General Description

The TLV743xxPDBVR series are hily accurate, low noise, CMOS LDO Voltage Regulators. Offering low iutput noise,high ripple rejection ratio, low dropout and very fast turn-on times, the TLV743xxPDBVR series is ideal for today's cutting edge mobile phone.Internally the TLV743xxPDBVR includes a reference voltage source,error amplifiers,driver transistors,current limiters and phase compensators.The TLV743xxPDBVR's output voltage is set by current trimming. Voltages are selectable in 100mV steps within a range of 0.9V to 5.0V.

When the CE input pin is low, the fast discharge channel can pass, a built-in pull-down resistor pulls the output voltage low. Fast discharge function.

The TLV743xxPDBVR series is also fully compatible with low ESR ceramic capacitors, reducing cost and improving output stability.This high level ofoutput stability is maintained even during frequent load fluctuations, due to the excellent transient response performance and high PSRR achieved across a broad range of frequencies. The CE function allows the output of regulator to be turned off,resulting in greatly reduced power consumption.

Features

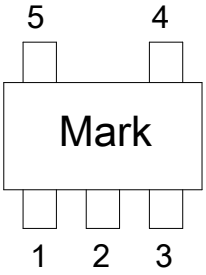
- Low power consumption:10uA (Typ.)
- Low voltage drop: 0.11V@100mA@VOUT=2.8V(Typ.)
- Standby Mode: 0.1uA
- Low temperature coefficient
- Good line Regulation:0.05%/V
- High Ripple Rejection: 75dB@100Hz(Typ.)
- High input voltage (up to 6.5V)
- Output voltage accuracy: tolerance ±2%
- SOT-23-5L package

Application

- Battery-powered equipment
- Communication equipment
- Mobile phones
- Portable games
- Cameras, Video cameras
- Reference voltage sources

Pin Configuration And Descriptions

SOT-23-5L
(TSOT-23-5)



PIN No. SOT-23-5L (TSOT-23-5)	Name	Functions Description
1	V_{IN}	Input
2	GND	Ground
3	CE	ON/OFF Control
4	NC	No Connect
5	V_{OUT}	Output

Order Information

Orderable Device	Package	Output Voltage	Packing Option
TLV743xxPDBVR	SOT-23-5L(TSOT-23-5)	1.2V 1.5V 1.8V 2.5V 2.8V 3.0V 3.3V	3000/Reel

xx:From 12-33

Absolute Maximum Ratings

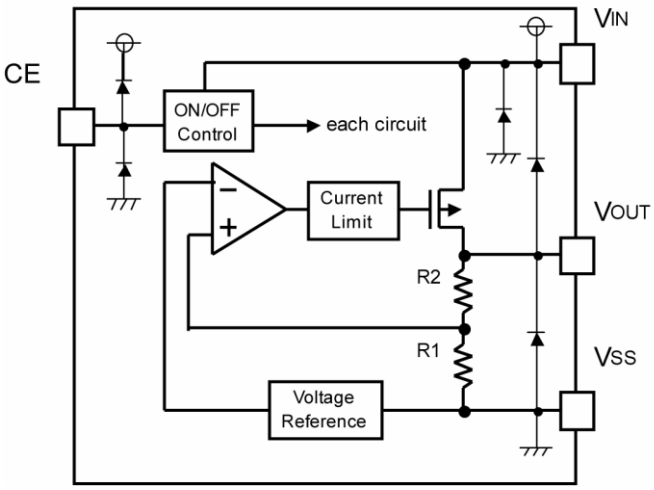
Description	Symbol	Value Range	Unit
Supply Voltage	V_{IN}	-0.3～+8	V
Storage Temperature Range	T_{STG}	-50～+125	°C
Operating Temperature	T_A	-40～+85	°C

Note:Stresses greater than those listed under “Absolute Maximum Ratingsmay” cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditionsis” not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Heat Dissipation

Description	Symbol	Package	Value Range	Unit
Thermal resistance	$è_{JA}$	SOT-23-5L	260	°C/W
Power dissipation	P_W	SOT-23-5L	0.4	W

Block Diagram

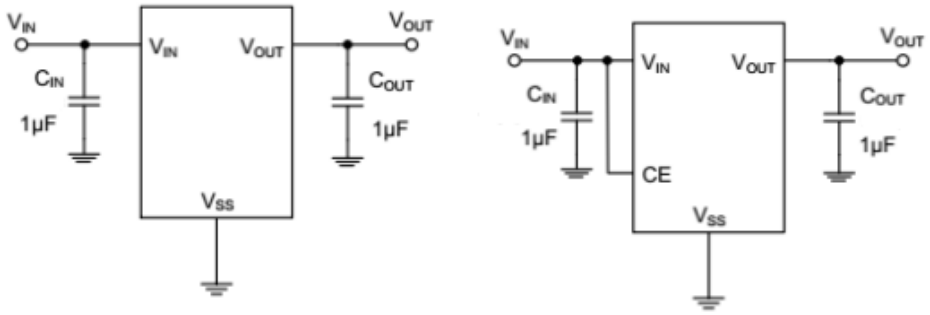


DC Characteristics (unless otherwise noted T_A= 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout≤2.5V	Vin=Vout+1V 1.0mA≤Iout≤100mA	Vout -0.05		Vout +0.05	V
	2.5V≤Vout≤5V	Vin=Vout+1V 1.0mA≤Iout≤300mA	Vout×0.98	--	Vout×1.02	V
Output Current*1	Iout	Vin-Vout=1V	--	300	--	mA
Line Regulation	△Vout1/ (△Vin·Vout)	4.3V≤Vin≤8V Iout=10mA	--	0.05	0.2	%/V
Load Regulation	△Vout	Vin= 4.3V 1.0mA≤Iout≤100mA	--	15	40	mV
Dropout Voltage	V_{DROP}	Iout=100mA	--	0.11	--	V
Output voltage Temperature Coefficiency	△Vout/(Ta·Vout)	Iout=30mA 0℃≤Ta≤70℃	--	±100	--	Ppm/℃
Supply Current	Iss	--	--	10	15	uA
Input Voltage	Vin	--	--	--	6.5	V
EN ligic high voltage	V_{ENH}	VIN=5.0V	1.5	--	--	V
EN logic low voltage	V_{ENL}	VIN=5.0V	--	--	0.4	V
PSRR	PSRR	F=100Hz, Vin=（VOUT+1） dc+1Vpp	--	75	--	dB
		F=1000Hz, Vin=（VOUT+1） dc+1Vpp	--	65	--	dB

Application Circuit

Basic Circuits



Operational Explanation

<Low ESR Capacitors>

With the TLV743xxPDBVR series, a stable output voltage is achievable even if used with low ESR capacitors as a phase compensation circuit is built-in. In order to ensure the effectiveness of the phase compensation, we suggest that an output capacitor (C_L) is connected as close as possible to the output pin (V_{OUT}) and the V_{SS} pin. Please use an output capacitor with a capacitance value of at least 10uF. Also, please connect an input capacitor (C_{IN}) of 10uF between the V_{IN} pin and the V_{SS} pin in order to ensure a stable power input. Stable phase compensation may not be ensured if the capacitor runs out capacitance when depending on bias and temperature. In case the capacitor depends on the bias and temperature, please make sure the capacitor can ensure the actual capacitance.

<CE Pin>

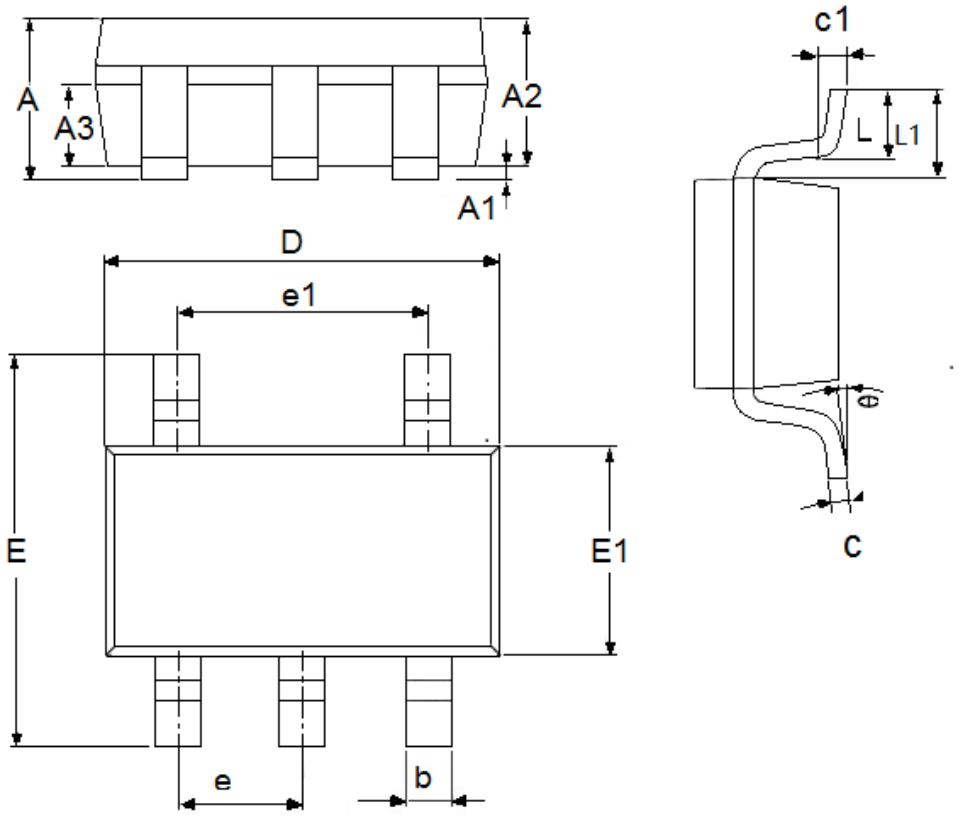
The IC's internal circuitry can be shutdown by the signal from the CE pin with the TLV743xxPDBVR series. In shutdown mode, output at the V_{OUT} pin will be pulled down to the V_{SS}. Although the CE pin is equal to an inverter input with CMOS hysteresis, with either the pull-up or pull-down options, the CE pin input current will increase when the IC is in operation. If you want add resistor before the CE pin，the resistor must be under 10K. We suggest that you use this IC with either a V_{IN} voltage or a V_{SS} voltage input at the CE pin. If this IC is used with the correct specifications for the CE pin, the operational logic is fixed and the IC will operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry.

Notes on Use

1. Please use this IC within the stated absolute maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please keep the resistance low between VIN and VSS wiring in particular.
3. Please wire the input capacitor (CIN) and the output capacitor (CL) as close to the IC as possible.

Package Outline Dimensions

SOT-23-5L(TSOT-23-5)



Symbol	Dimensions in Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.05	1.45	0.0413	0.0571
A1	0	0.15	0.0000	0.0059
A2	0.9	1.3	0.0354	0.0512
A3	0.6	0.7	0.0236	0.0276
b	0.25	0.5	0.0098	0.0197
c	0.1	0.23	0.0039	0.0091
D	2.82	3.05	0.1110	0.1201
e1	1.9(TYP)		0.0748(TYP)	
E	2.6	3.05	0.1024	0.1201
E1	1.5	1.75	0.0512	0.0689
e	0.95(TYP)		0.0374(TYP)	
L	0.25	0.6	0.0098	0.0236
L1	0.59(TYP)		0.0232(TYP)	
θ	0	8°	0.0000	8°
c1	0.2(TYP)		0.0079(TYP)	

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