

74AVC4T245-Q100

4-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 6 — 11 April 2024

Product data sheet

1. General description

The 74AVC4T245-Q100 is an 4-bit, dual supply transceiver that enables bidirectional level translation. The device can be used as two 2-bit transceivers or as a 4-bit transceiver. It features four 2-bit input-output ports (nAn and nBn), a direction control input (nDIR), an output enable input (nOE) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins nAn, $n\overline{OE}$ and nDIR are referenced to $V_{CC(A)}$ and pins nBn are referenced to $V_{CC(B)}$. A HIGH on nDIR allows transmission from nAn to nBn and a LOW on nDIR allows transmission from nBn to nAn. The output enable input ($n\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated. The device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both nAn and nBn are in the high-impedance OFF-state.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range: $V_{CC(A)}$: 0.8 V to 3.6 V; $V_{CC(B)}$: 0.8 V to 3.6 V
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-B (2.7 V to 3.6 V)
- Maximum data rates:
 - 380 Mbit/s (\geq 1.8 V to 3.3 V translation)
 - 200 Mbit/s (\geq 1.1 V to 3.3 V translation)
 - 200 Mbit/s (\geq 1.1 V to 2.5 V translation)
 - 200 Mbit/s (\geq 1.1 V to 1.8 V translation)
 - 150 Mbit/s (\geq 1.1 V to 1.5 V translation)
 - 100 Mbit/s (\geq 1.1 V to 1.2 V translation)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3B exceeds 8000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

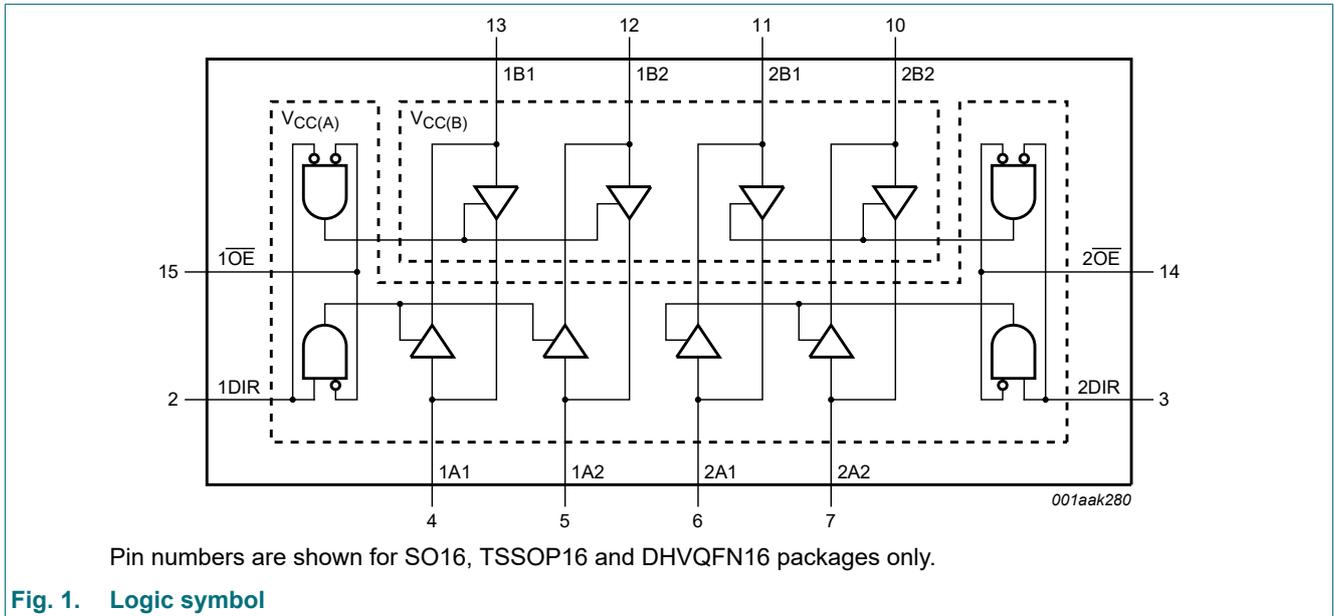
Type number	Package			Version
	Temperature range	Name	Description	
74AVC4T245D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AVC4T245PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AVC4T245BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74AVC4T245GU-Q100	-40 °C to +125 °C	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 × 2.60 × 0.50 mm	SOT1161-1

4. Marking

Table 2. Marking codes

Type number	Marking code
74AVC4T245D-Q100	74AVC4T245D
74AVC4T245PW-Q100	VC4T245
74AVC4T245BQ-Q100	C4T245
74AVC4T245GU-Q100	BT5

5. Functional diagram



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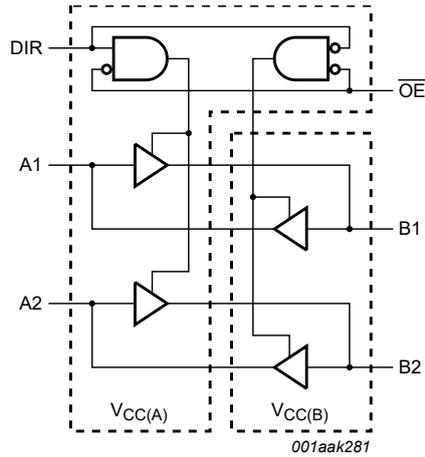


Fig. 2. Logic diagram (one 2-bit transceiver)

6. Pinning information

6.1. Pinning

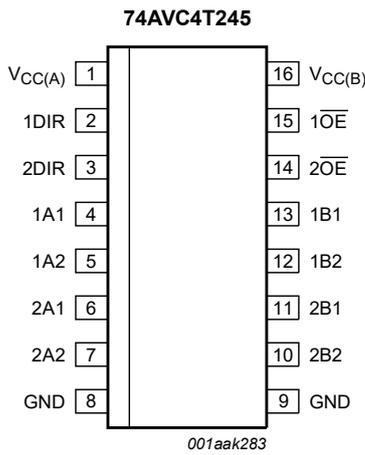


Fig. 3. Pin configuration SOT109-1 (SO16)

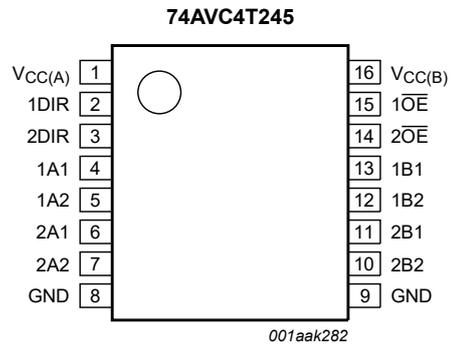
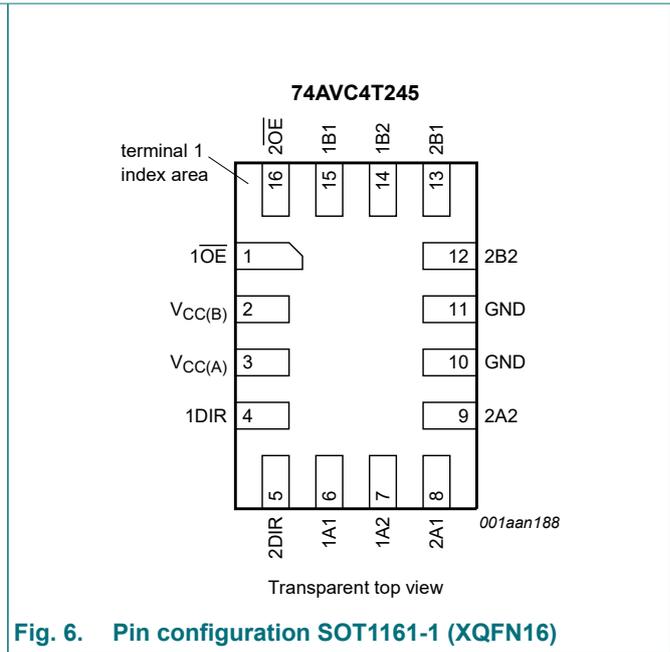
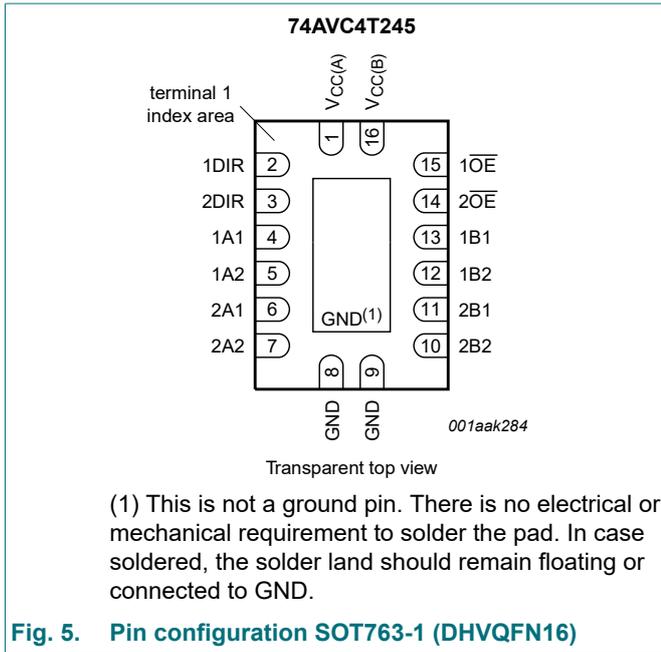


Fig. 4. Pin configuration SOT403-1 (TSSOP16)

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6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT109-1, SOT403-1 and SOT763-1	SOT1161-1	
V _{CC(A)}	1	3	supply voltage A (nAn, n \overline{OE} and nDIR inputs are referenced to V _{CC(A)})
1DIR, 2DIR	2, 3	4, 5	direction control
1A1, 1A2	4, 5	6, 7	data input or output
2A1, 2A2	6, 7	8, 9	data input or output
GND[1]	8, 9	10, 11	ground (0 V)
2B2, 2B1	10, 11	12, 13	data input or output
1B2, 1B1	12, 13	14, 15	data input or output
2 \overline{OE} , 1 \overline{OE}	14, 15	16, 1	output enable input (active LOW)
V _{CC(B)}	16	2	supply voltage B (nBn inputs are referenced to V _{CC(B)})

[1] All GND pins must be connected to ground (0 V).

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage	Input		Input/output[1]	
	nOE [2]	nDIR[2]	nAn[2]	nBn[2]
0.8 V to 3.6 V	L	L	nAn = nBn	input
0.8 V to 3.6 V	L	H	input	nBn = nAn
0.8 V to 3.6 V	H	X	Z	Z
GND[1]	X	X	Z	Z

[1] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

[2] The nAn, nDIR and nOE input circuit is referenced to $V_{CC(A)}$; The nBn input circuit is referenced to $V_{CC(B)}$.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode [1] [2] [3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode [1]	-0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CCO} [2]	-	± 50	mA
I_{CC}	supply current	per $V_{CC(A)}$ or $V_{CC(B)}$ pin	-	100	mA
I_{GND}	ground current	per GND pin	-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		SOT109-1; SOT403-1; SOT763-1 [4]	-	500	mW
		SOT1161-1	-	250	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] $V_{CCO} + 0.5$ V should not exceed 4.6 V.

[4] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
 For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
 For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		0.8	3.6	V
$V_{CC(B)}$	supply voltage B		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode [1]	0	V_{CCO}	V
		Suspend or 3-state mode	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8\text{ V to }3.6\text{ V}$ [2]	-	5	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

10. Static characteristics

Table 7. Typical static characteristics at $T_{amb} = 25\text{ °C}$

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -1.5\text{ mA}$; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.69	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 1.5\text{ mA}$; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.07	-	V
I_I	input leakage current	nDIR, \overline{nOE} input; $V_I = 0\text{ V or }3.6\text{ V}$; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V to }3.6\text{ V}$	-	± 0.025	± 0.25	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0\text{ V or }V_{CCO}$; $V_{CC(A)} = V_{CC(B)} = 3.6\text{ V}$ [2]	-	± 0.5	± 2.5	μA
		suspend mode A port; $V_O = 0\text{ V or }V_{CCO}$; $V_{CC(A)} = 3.6\text{ V}$; $V_{CC(B)} = 0\text{ V}$ [2]	-	± 0.5	± 2.5	μA
		suspend mode B port; $V_O = 0\text{ V or }V_{CCO}$; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 3.6\text{ V}$ [2]	-	± 0.5	± 2.5	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\text{ V to }3.6\text{ V}$; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 0.8\text{ V to }3.6\text{ V}$	-	± 0.1	± 1	μA
		B port; V_I or $V_O = 0\text{ V to }3.6\text{ V}$; $V_{CC(B)} = 0\text{ V}$; $V_{CC(A)} = 0.8\text{ V to }3.6\text{ V}$	-	± 0.1	± 1	μA
C_I	input capacitance	nDIR, \overline{nOE} input; $V_I = 0\text{ V or }3.3\text{ V}$; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	1.0	-	pF
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3\text{ V or }0\text{ V}$; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	4.0	-	pF

[1] V_{CCO} is the supply voltage associated with the output port; V_{CCI} is the supply voltage associated with the data input port.

[2] For I/O ports, the parameter I_{OZ} includes the input leakage current.

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Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	data input					
		V _{CCI} = 0.8 V	0.70V _{CCI}	-	0.70V _{CCI}	-	V
		V _{CCI} = 1.1 V to 1.95 V	0.65V _{CCI}	-	0.65V _{CCI}	-	V
		V _{CCI} = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V _{CCI} = 3.0 V to 3.6 V	2	-	2	-	V
		nDIR, nOE input					
		V _{CC(A)} = 0.8 V	0.70V _{CC(A)}	-	0.70V _{CC(A)}	-	V
		V _{CC(A)} = 1.1 V to 1.95 V	0.65V _{CC(A)}	-	0.65V _{CC(A)}	-	V
V _{IL}	LOW-level input voltage	data input					
		V _{CCI} = 0.8 V	-	0.30V _{CCI}	-	0.30V _{CCI}	V
		V _{CCI} = 1.1 V to 1.95 V	-	0.35V _{CCI}	-	0.35V _{CCI}	V
		V _{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V _{CCI} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		nDIR, nOE input					
		V _{CC(A)} = 0.8 V	-	0.30V _{CC(A)}	-	0.30V _{CC(A)}	V
		V _{CC(A)} = 1.1 V to 1.95 V	-	0.35V _{CC(A)}	-	0.35V _{CC(A)}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = -100 µA; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	V _{CCO} - 0.1	-	V _{CCO} - 0.1	-	V
		I _O = -3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	0.85	-	0.85	-	V
		I _O = -6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	1.05	-	1.05	-	V
		I _O = -8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	1.2	-	1.2	-	V
		I _O = -9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	1.75	-	1.75	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 100 µA; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I _O = 3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	-	0.25	-	0.25	V
		I _O = 6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	-	0.35	-	0.35	V
		I _O = 8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	-	0.45	-	0.45	V
		I _O = 9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	-	0.55	-	0.55	V
I _I	input leakage current	nDIR, nOE input; V _I = 0 V or 3.6 V; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	±1	-	±5	µA

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Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = V _{CC(B)} = 3.6 V [2]	-	±5	-	±30	μA
		suspend mode A port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V [2]	-	±5	-	±30	μA
		suspend mode B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V [2]	-	±5	-	±30	μA
I _{OFF}	power-off leakage current	A port; V _I or V _O = 0 V to 3.6 V; V _{CC(A)} = 0 V; V _{CC(B)} = 0.8 V to 3.6 V	-	±5	-	±30	μA
		B port; V _I or V _O = 0 V to 3.6 V; V _{CC(B)} = 0 V; V _{CC(A)} = 0.8 V to 3.6 V	-	±5	-	±30	μA
I _{CC}	supply current	A port; V _I = 0 V or V _{CCI} ; I _O = 0 A					
		V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	10	-	55	μA
		V _{CC(A)} = 1.1 V to 3.6 V; V _{CC(B)} = 1.1 V to 3.6 V	-	8	-	50	μA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-	8	-	50	μA
		V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V	-2	-	-12	-	μA
		B port; V _I = 0 V or V _{CCI} ; I _O = 0 A					
		V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	10	-	55	μA
		V _{CC(A)} = 1.1 V to 3.6 V; V _{CC(B)} = 1.1 V to 3.6 V	-	8	-	50	μA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-2	-	-12	-	μA
		V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V	-	8	-	50	μA
		A plus B port (I _{CC(A)} + I _{CC(B)}); I _O = 0 A; V _I = 0 V or V _{CCI} ; V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	20	-	70	μA
A plus B port (I _{CC(A)} + I _{CC(B)}); I _O = 0 A; V _I = 0 V or V _{CCI} ; V _{CC(A)} = 1.1 V to 3.6 V; V _{CC(B)} = 1.1 V to 3.6 V	-	16	-	65	μA		

[1] V_{CCO} is the supply voltage associated with the output port; V_{CCI} is the supply voltage associated with the data input port.
 [2] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 9. Typical total supply current (I_{CC(A)} + I_{CC(B)})

V _{CC(A)}	V _{CC(B)}							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA

11. Dynamic characteristics

Table 10. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C_{PD}	power dissipation capacitance	A port: (direction nAn to nBn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nAn to nBn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nBn to nAn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction nBn to nAn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction nAn to nBn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction nAn to nBn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction nBn to nAn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction nBn to nAn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] $f_i = 10\text{ MHz}$; $V_i = \text{GND to } V_{CC}$; $t_r = t_f = 1\text{ ns}$; $C_L = 0\text{ pF}$; $R_L = \infty\ \Omega$.

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Table 11. Typical dynamic characteristics at $V_{CC(A)} = 0.8\text{ V}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9; for waveforms see Fig. 7 and Fig. 8.[1]

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.5	7.3	6.5	6.2	5.9	6.0	ns
		nBn to nAn	14.5	12.7	12.4	12.3	12.1	12.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn	14.3	14.3	14.3	14.3	14.3	14.3	ns
		$n\overline{OE}$ to nBn	17.0	9.9	9.0	9.4	9.0	9.7	ns
t_{en}	enable time	$n\overline{OE}$ to nAn	18.2	18.2	18.2	18.2	18.2	18.2	ns
		$n\overline{OE}$ to nBn	19.2	10.7	9.8	9.6	9.7	10.2	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Table 12. Typical dynamic characteristics at $V_{CC(B)} = 0.8\text{ V}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9; for waveforms see Fig. 7 and Fig. 8.[1]

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.5	12.7	12.4	12.3	12.1	12.0	ns
		nBn to nAn	14.5	7.3	6.5	6.2	5.9	6.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn	14.3	5.5	4.1	4.0	3.0	3.5	ns
		$n\overline{OE}$ to nBn	17.0	13.8	13.4	13.1	12.9	12.7	ns
t_{en}	enable time	$n\overline{OE}$ to nAn	18.2	5.6	4.0	3.2	2.4	2.2	ns
		$n\overline{OE}$ to nBn	19.2	14.6	14.1	13.9	13.7	13.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

4-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 13. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9; for waveforms see Fig. 7 and Fig. 8.[1]

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 1.1 V to 1.3 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.4	0.5	7.1	0.5	6.2	0.5	5.2	0.5	5.1	ns
		nBn to nAn	0.5	9.4	0.5	8.9	0.5	8.7	0.5	8.4	0.5	8.2	ns
t _{dis}	disable time	n \overline{OE} to nAn	1.8	10.9	1.8	10.9	1.8	10.9	1.8	10.9	1.8	10.9	ns
		n \overline{OE} to nBn	1.9	12.4	1.9	9.6	1.9	9.5	1.4	8.1	1.2	9.1	ns
t _{en}	enable time	n \overline{OE} to nAn	1.4	12.8	1.4	12.8	1.4	12.8	1.4	12.8	1.4	12.8	ns
		n \overline{OE} to nBn	1.1	13.3	1.1	10.0	1.1	8.9	1.0	7.9	1.0	7.7	ns
V_{CC(A)} = 1.4 V to 1.6 V													
t _{pd}	propagation delay	nAn to nBn	0.3	8.9	0.3	6.3	0.3	5.2	0.3	4.2	0.3	4.2	ns
		nBn to nAn	0.7	7.1	0.7	6.3	0.5	6.0	0.4	5.7	0.3	5.6	ns
t _{dis}	disable time	n \overline{OE} to nAn	1.8	10.2	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns
		n \overline{OE} to nBn	1.9	11.3	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns
t _{en}	enable time	n \overline{OE} to nAn	1.1	9.4	1.4	9.4	1.1	9.4	0.7	9.4	0.4	9.4	ns
		n \overline{OE} to nBn	1.4	12.1	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns
V_{CC(A)} = 1.65 V to 1.95 V													
t _{pd}	propagation delay	nAn to nBn	0.1	8.7	0.1	6.0	0.1	4.9	0.1	3.9	0.3	3.9	ns
		nBn to nAn	0.6	6.2	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	ns
t _{dis}	disable time	n \overline{OE} to nAn	1.8	8.6	1.6	8.6	1.8	8.6	1.3	8.6	1.6	8.6	ns
		n \overline{OE} to nBn	1.7	10.9	1.7	9.9	1.6	8.7	1.2	6.9	1.0	6.9	ns
t _{en}	enable time	n \overline{OE} to nAn	1.0	7.2	1.0	7.2	1.0	7.2	0.6	7.2	0.4	7.2	ns
		n \overline{OE} to nBn	1.2	11.7	1.2	9.2	1.0	7.4	0.8	5.3	0.8	4.6	ns
V_{CC(A)} = 2.3 V to 2.7 V													
t _{pd}	propagation delay	nAn to nBn	0.1	8.4	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns
		nBn to nAn	0.6	5.2	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns
t _{dis}	disable time	n \overline{OE} to nAn	1.0	6.2	1.0	6.2	1.0	6.2	1.0	6.2	1.0	6.2	ns
		n \overline{OE} to nBn	1.5	10.4	1.5	8.8	1.3	8.2	1.1	6.2	0.9	5.2	ns
t _{en}	enable time	n \overline{OE} to nAn	0.7	4.8	0.7	4.8	0.7	4.8	0.6	4.8	0.4	4.8	ns
		n \overline{OE} to nBn	0.9	11.3	0.9	8.8	0.8	7.0	0.6	4.8	0.6	4.0	ns
V_{CC(A)} = 3.0 V to 3.6 V													
t _{pd}	propagation delay	nAn to nBn	0.1	8.2	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns
		nBn to nAn	0.6	5.1	0.6	4.2	0.4	3.4	0.2	3.0	0.1	2.8	ns
t _{dis}	disable time	n \overline{OE} to nAn	0.7	5.6	0.7	5.6	0.7	5.6	0.7	5.6	0.7	5.6	ns
		n \overline{OE} to nBn	1.4	10.2	1.4	9.3	1.2	8.1	1.0	6.4	0.8	6.2	ns
t _{en}	enable time	n \overline{OE} to nAn	0.6	3.8	0.6	3.8	0.6	3.8	0.6	3.8	0.4	3.8	ns
		n \overline{OE} to nBn	0.8	11.3	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PZH}; t_{en} is the same as t_{PZL} and t_{PZH}.

4-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 14. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9; for waveforms see Fig. 7 and Fig. 8.[1]

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 1.1 V to 1.3 V													
t _{pd}	propagation delay	nAn to nBn	0.5	10.4	0.5	7.9	0.5	6.9	0.5	5.8	0.5	5.7	ns
		nBn to nAn	0.5	10.4	0.5	9.8	0.5	9.6	0.5	9.3	0.5	9.1	ns
t _{dis}	disable time	n \overline{OE} to nAn	1.8	12.0	1.8	12.0	1.8	12.0	1.8	12.0	1.8	12.0	ns
		n \overline{OE} to nBn	1.9	13.7	1.9	10.6	1.9	10.5	1.4	9.0	1.2	10.1	ns
t _{en}	enable time	n \overline{OE} to nAn	1.4	14.1	1.4	14.1	1.4	14.1	1.4	14.1	1.4	14.1	ns
		n \overline{OE} to nBn	1.1	14.7	1.1	11.0	1.1	9.8	1.0	8.7	1.0	8.5	ns
V_{CC(A)} = 1.4 V to 1.6 V													
t _{pd}	propagation delay	nAn to nBn	0.3	9.8	0.3	7.0	0.3	5.8	0.3	4.7	0.3	4.7	ns
		nBn to nAn	0.7	7.9	0.7	7.0	0.5	6.6	0.4	6.3	0.3	6.2	ns
t _{dis}	disable time	n \overline{OE} to nAn	1.8	11.3	1.8	11.3	1.5	11.3	1.3	11.3	1.6	11.3	ns
		n \overline{OE} to nBn	1.9	12.5	1.9	11.4	1.9	10.1	1.4	8.2	1.2	8.4	ns
t _{en}	enable time	n \overline{OE} to nAn	1.1	10.4	1.4	10.4	1.1	10.4	0.7	10.4	0.4	10.4	ns
		n \overline{OE} to nBn	1.4	13.3	1.4	10.6	1.1	8.5	0.9	6.4	0.9	6.2	ns
V_{CC(A)} = 1.65 V to 1.95 V													
t _{pd}	propagation delay	nAn to nBn	0.1	9.6	0.1	6.6	0.1	5.4	0.1	4.3	0.3	4.3	ns
		nBn to nAn	0.6	6.9	0.6	5.9	0.5	5.4	0.3	5.1	0.3	5.0	ns
t _{dis}	disable time	n \overline{OE} to nAn	1.8	9.5	1.6	9.5	1.8	9.5	1.3	9.5	1.6	9.5	ns
		n \overline{OE} to nBn	1.7	12.0	1.7	10.9	1.6	9.6	1.2	7.6	1.0	7.6	ns
t _{en}	enable time	n \overline{OE} to nAn	1.0	8.0	1.0	8.0	1.0	8.0	0.6	8.0	0.4	8.0	ns
		n \overline{OE} to nBn	1.2	12.9	1.2	10.2	1.0	8.2	0.8	5.9	0.8	5.1	ns
V_{CC(A)} = 2.3 V to 2.7 V													
t _{pd}	propagation delay	nAn to nBn	0.1	9.3	0.1	6.3	0.1	5.1	0.2	4.0	0.1	4.0	ns
		nBn to nAn	0.6	5.8	0.6	4.7	0.4	4.3	0.2	3.9	0.2	3.8	ns
t _{dis}	disable time	n \overline{OE} to nAn	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	ns
		n \overline{OE} to nBn	1.5	11.5	1.5	10.4	1.3	9.1	1.1	6.9	0.9	5.8	ns
t _{en}	enable time	n \overline{OE} to nAn	0.7	5.3	0.7	5.3	0.7	5.3	0.6	5.3	0.4	5.3	ns
		n \overline{OE} to nBn	0.9	12.4	0.9	9.7	0.8	7.7	0.6	5.3	0.6	4.4	ns
V_{CC(A)} = 3.0 V to 3.6 V													
t _{pd}	propagation delay	nAn to nBn	0.1	9.1	0.1	6.2	0.1	5.0	0.1	3.8	0.1	3.3	ns
		nBn to nAn	0.6	5.7	0.6	4.7	0.4	3.9	0.2	3.4	0.1	3.3	ns
t _{dis}	disable time	n \overline{OE} to nAn	0.7	6.2	0.7	6.2	0.7	6.2	0.7	6.2	0.7	6.2	ns
		n \overline{OE} to nBn	1.4	11.3	1.4	10.3	1.2	9.0	1.0	7.1	0.8	6.9	ns
t _{en}	enable time	n \overline{OE} to nAn	0.6	4.2	0.6	4.2	0.6	4.2	0.6	4.2	0.4	4.2	ns
		n \overline{OE} to nBn	0.8	12.4	0.8	9.6	0.6	7.5	0.5	5.2	0.5	4.2	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

11.1. Waveforms and test circuit

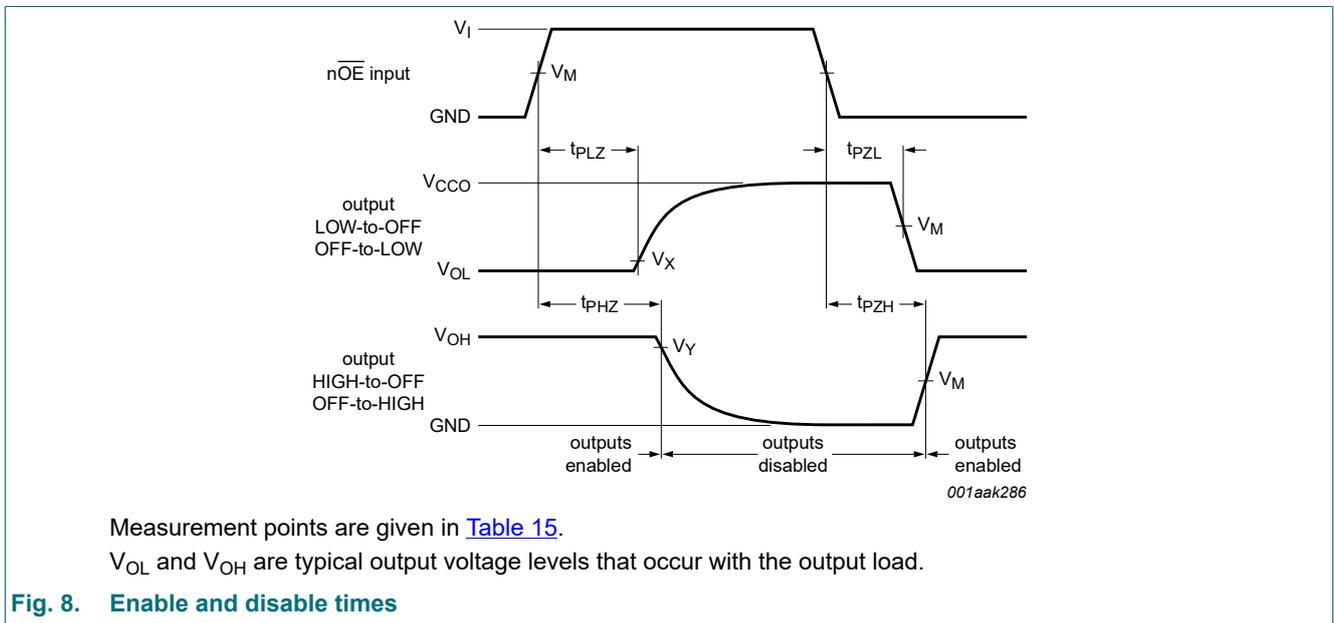
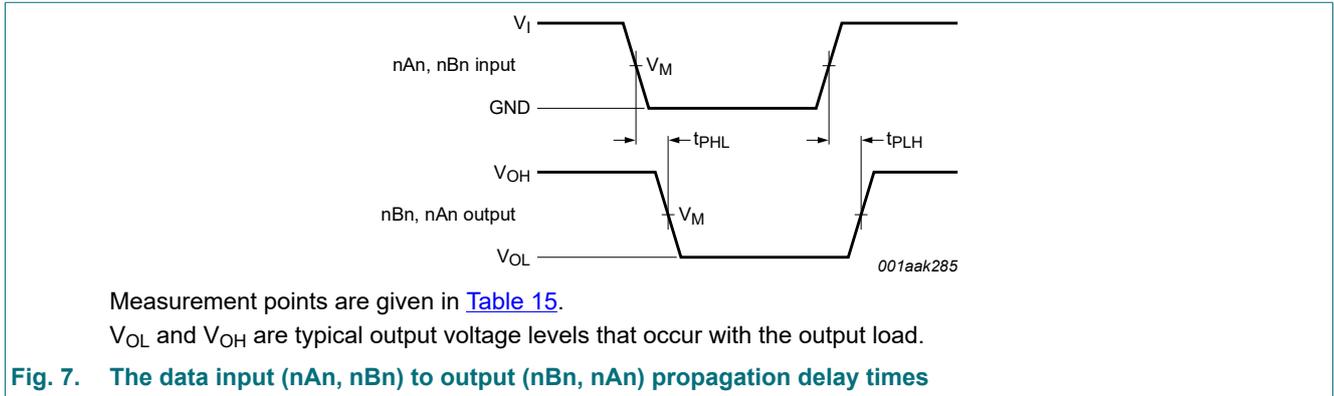


Table 15. Measurement points

Supply voltage	Input[1]	Output[2]		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1\text{ V}$	$V_{OH} - 0.1\text{ V}$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1] V_{CCI} is the supply voltage associated with the data input port.
 [2] V_{CCO} is the supply voltage associated with the output port.

4-bit dual supply translating transceiver with configurable voltage translation; 3-state

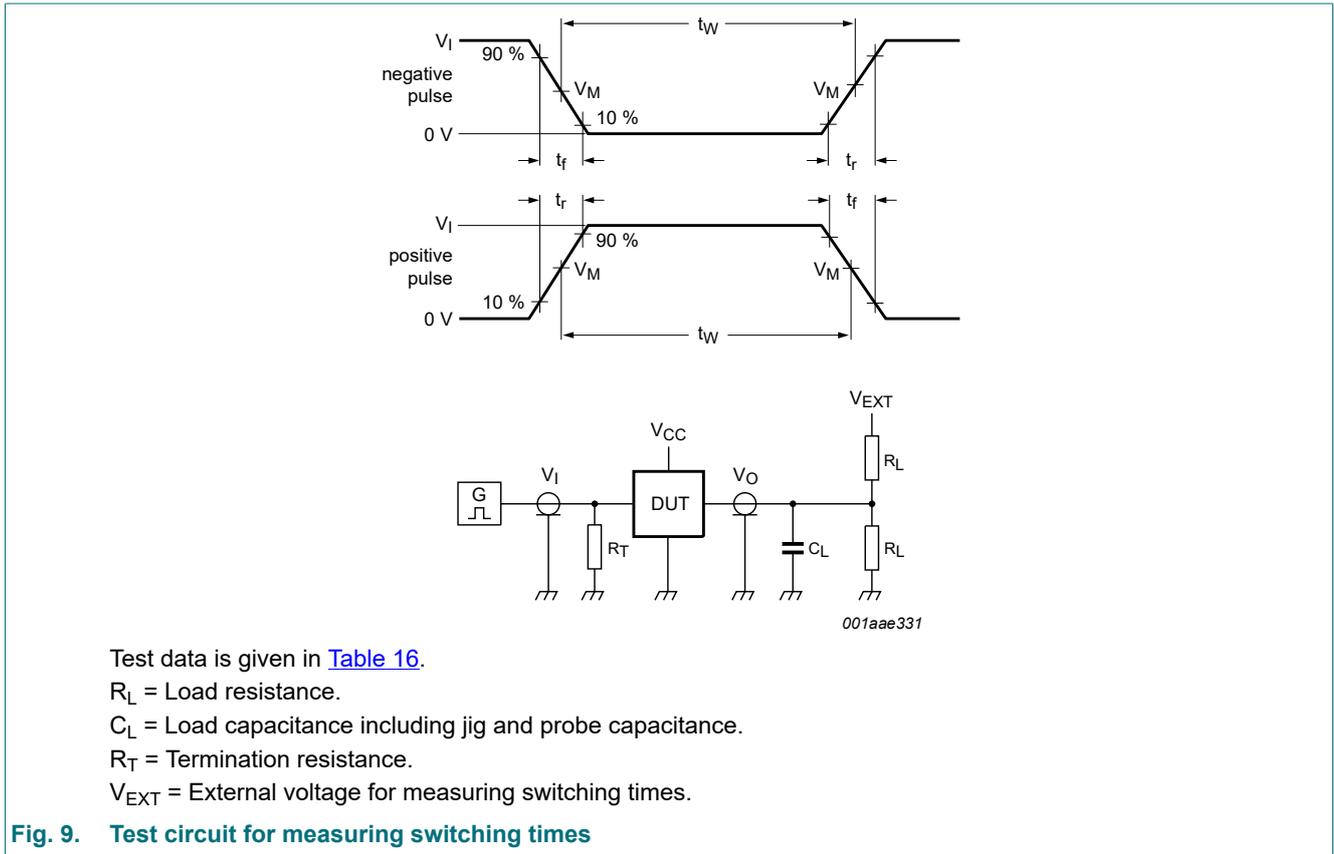
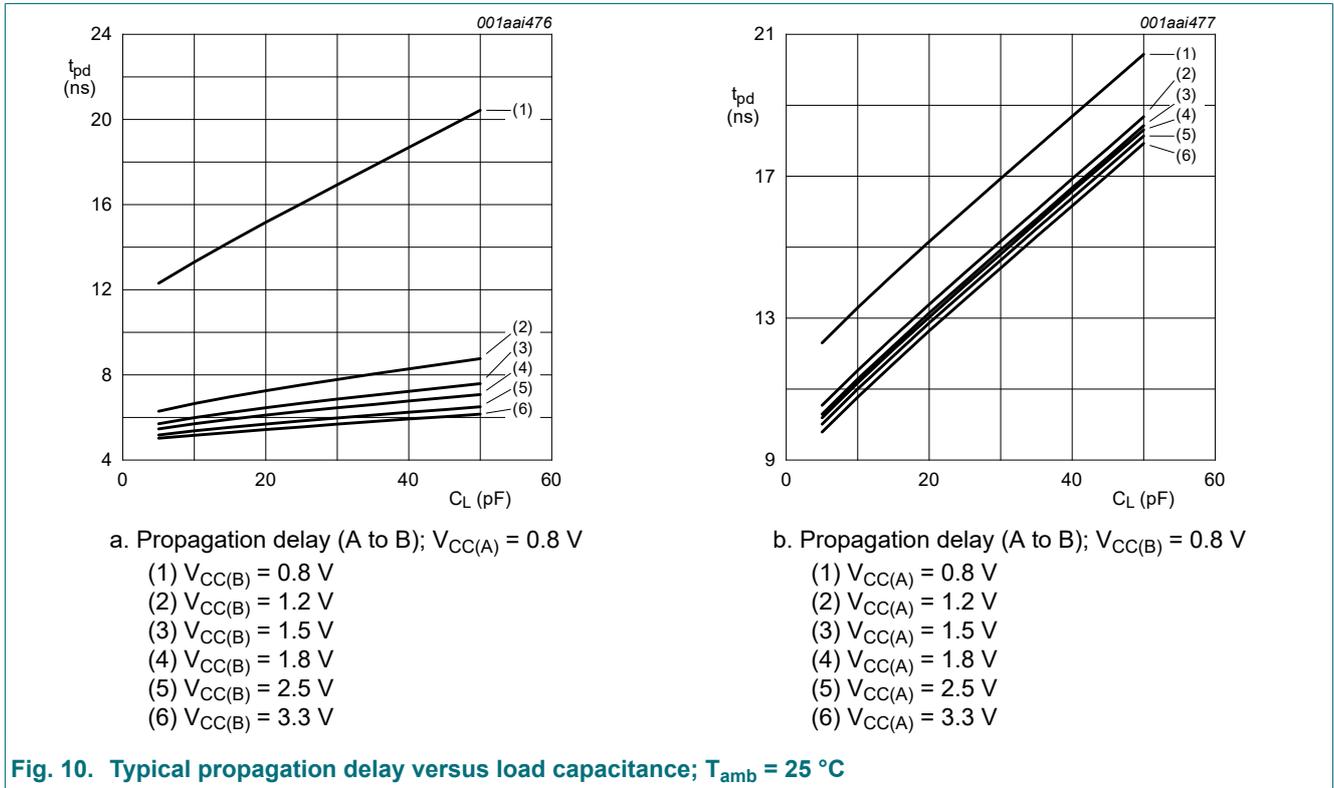


Table 16. Test data

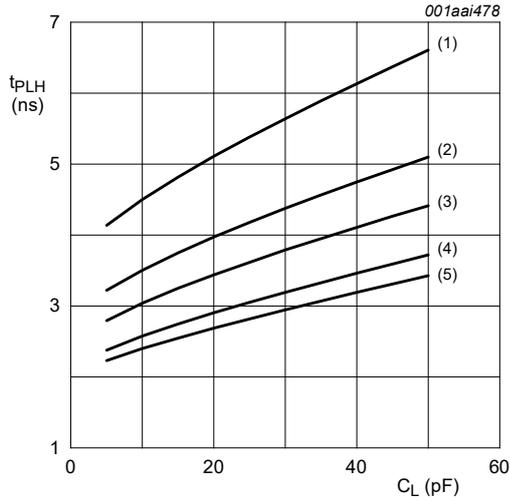
Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	V_I [1]	$\Delta t/\Delta V$ [2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [3]
0.8 V to 1.6 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the data input port.
 [2] $dV/dt \geq 1.0 \text{ V/ns}$
 [3] V_{CCO} is the supply voltage associated with the output port.

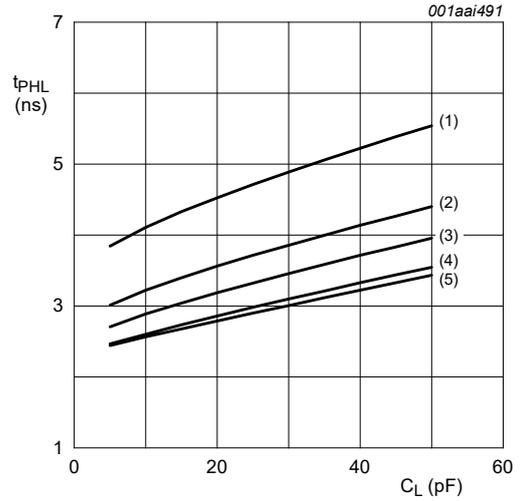
12. Typical propagation delay characteristics



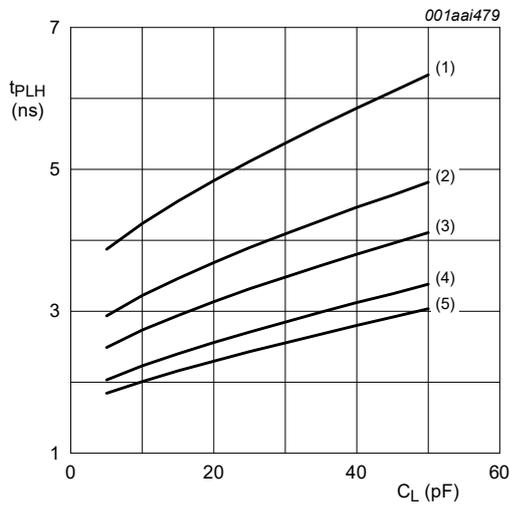
4-bit dual supply translating transceiver with configurable voltage translation; 3-state



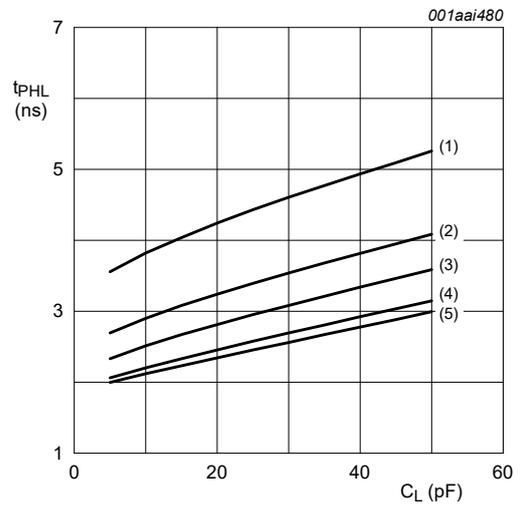
a. LOW to HIGH propagation delay (A to B); $V_{CC(A)} = 1.2\text{ V}$



b. HIGH to LOW propagation delay (A to B); $V_{CC(A)} = 1.2\text{ V}$



c. LOW to HIGH propagation delay (A to B); $V_{CC(A)} = 1.5\text{ V}$

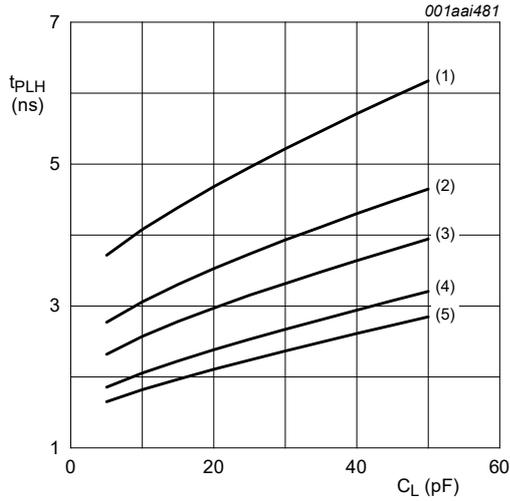


d. HIGH to LOW propagation delay (A to B); $V_{CC(A)} = 1.5\text{ V}$

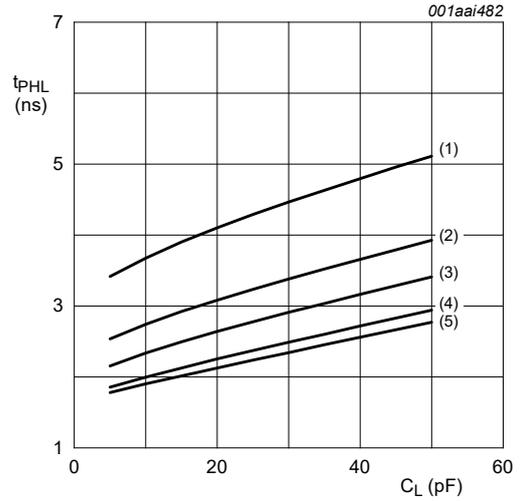
- (1) $V_{CC(B)} = 1.2\text{ V}$
- (2) $V_{CC(B)} = 1.5\text{ V}$
- (3) $V_{CC(B)} = 1.8\text{ V}$
- (4) $V_{CC(B)} = 2.5\text{ V}$
- (5) $V_{CC(B)} = 3.3\text{ V}$

Fig. 11. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ °C}$

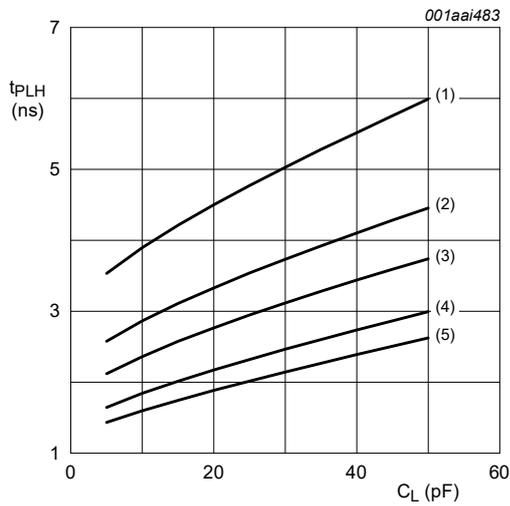
4-bit dual supply translating transceiver with configurable voltage translation; 3-state



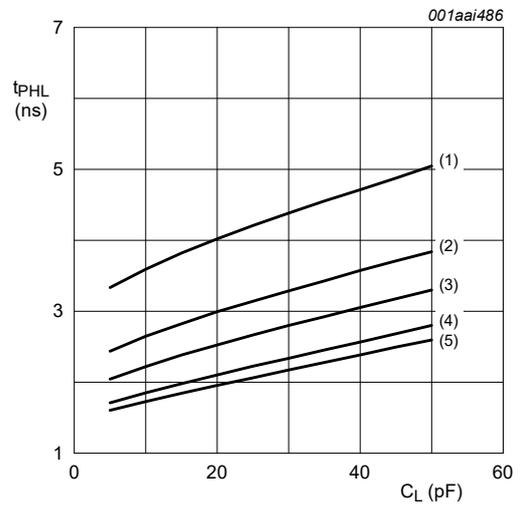
a. LOW to HIGH propagation delay (A to B); $V_{CC(A)} = 1.8\text{ V}$



b. HIGH to LOW propagation delay (A to B); $V_{CC(A)} = 1.8\text{ V}$



c. LOW to HIGH propagation delay (A to B); $V_{CC(A)} = 2.5\text{ V}$

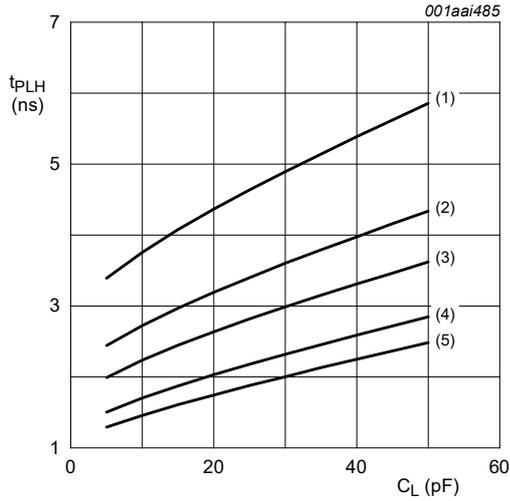


d. HIGH to LOW propagation delay (A to B); $V_{CC(A)} = 2.5\text{ V}$

- (1) $V_{CC(B)} = 1.2\text{ V}$
- (2) $V_{CC(B)} = 1.5\text{ V}$
- (3) $V_{CC(B)} = 1.8\text{ V}$
- (4) $V_{CC(B)} = 2.5\text{ V}$
- (5) $V_{CC(B)} = 3.3\text{ V}$

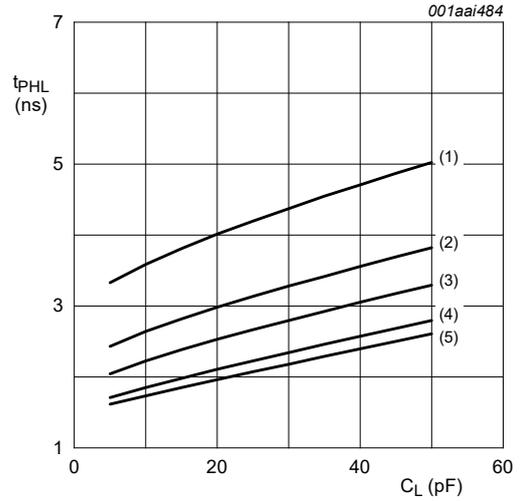
Fig. 12. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ °C}$

4-bit dual supply translating transceiver with configurable voltage translation; 3-state



a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 3.3\text{ V}$

- (1) $V_{CC(B)} = 1.2\text{ V}$
- (2) $V_{CC(B)} = 1.5\text{ V}$
- (3) $V_{CC(B)} = 1.8\text{ V}$
- (4) $V_{CC(B)} = 2.5\text{ V}$
- (5) $V_{CC(B)} = 3.3\text{ V}$



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 3.3\text{ V}$

Fig. 13. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ °C}$

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

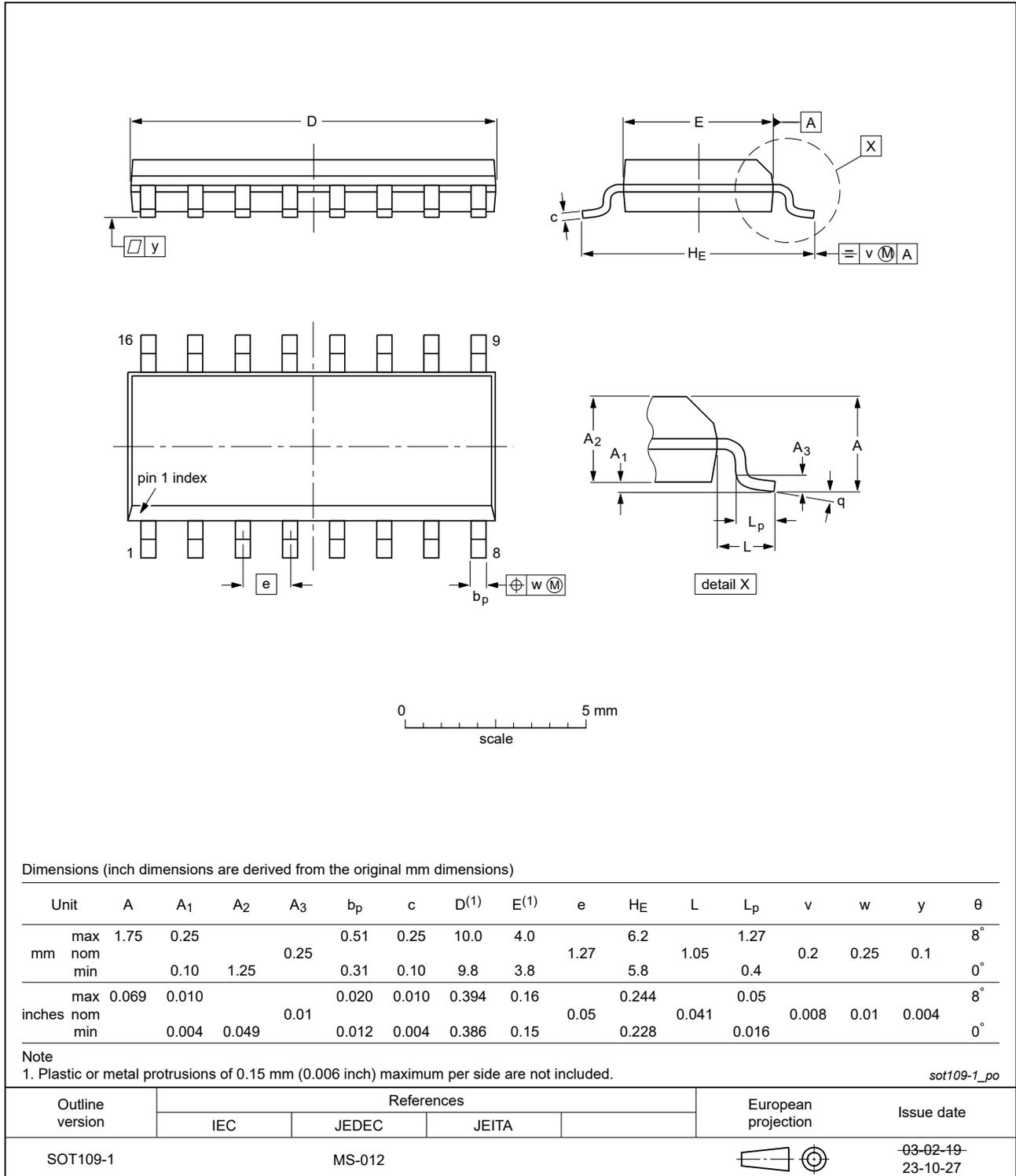


Fig. 14. Package outline SOT109-1 (SO16)

4-bit dual supply translating transceiver with configurable voltage translation; 3-state

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

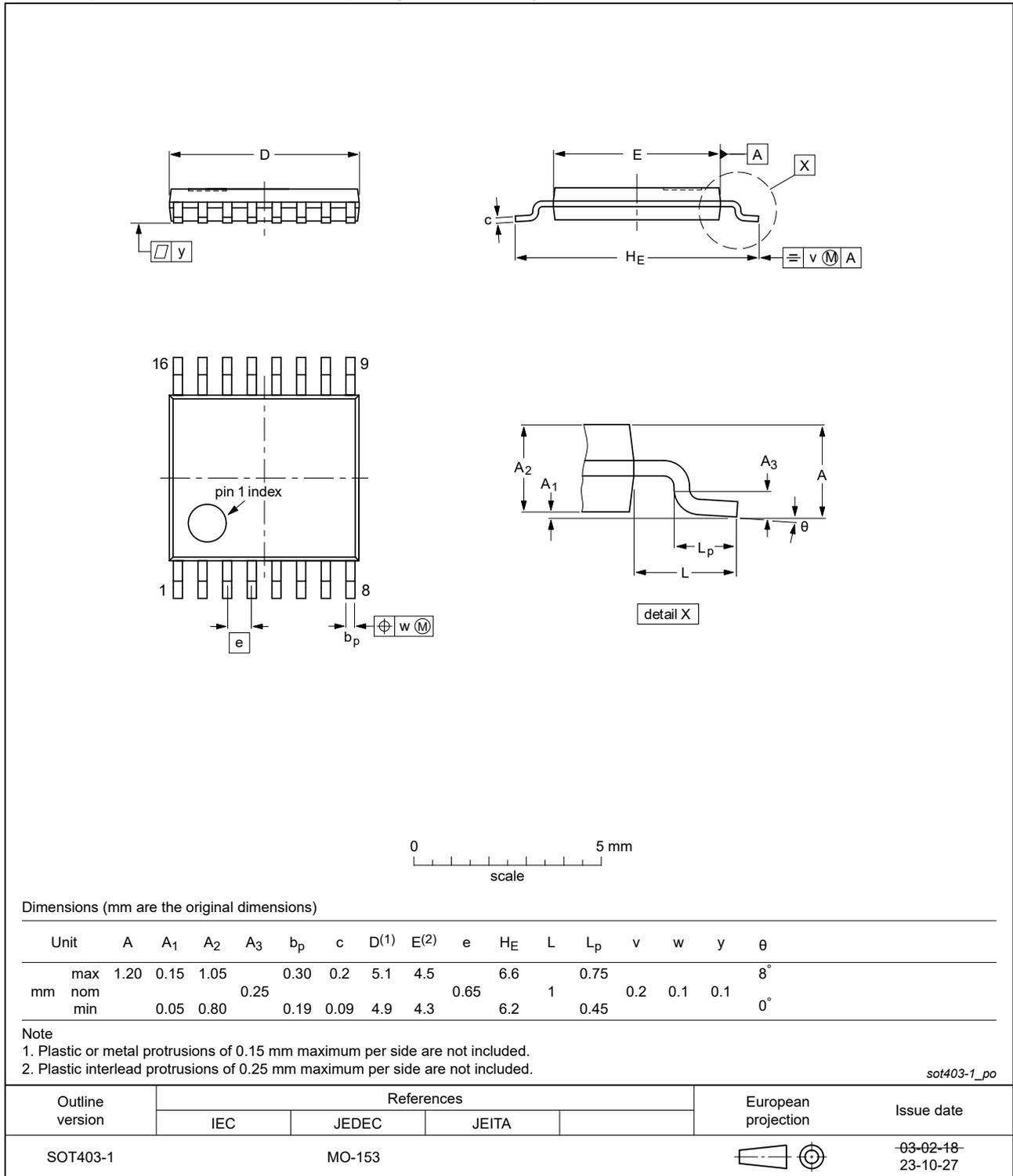


Fig. 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

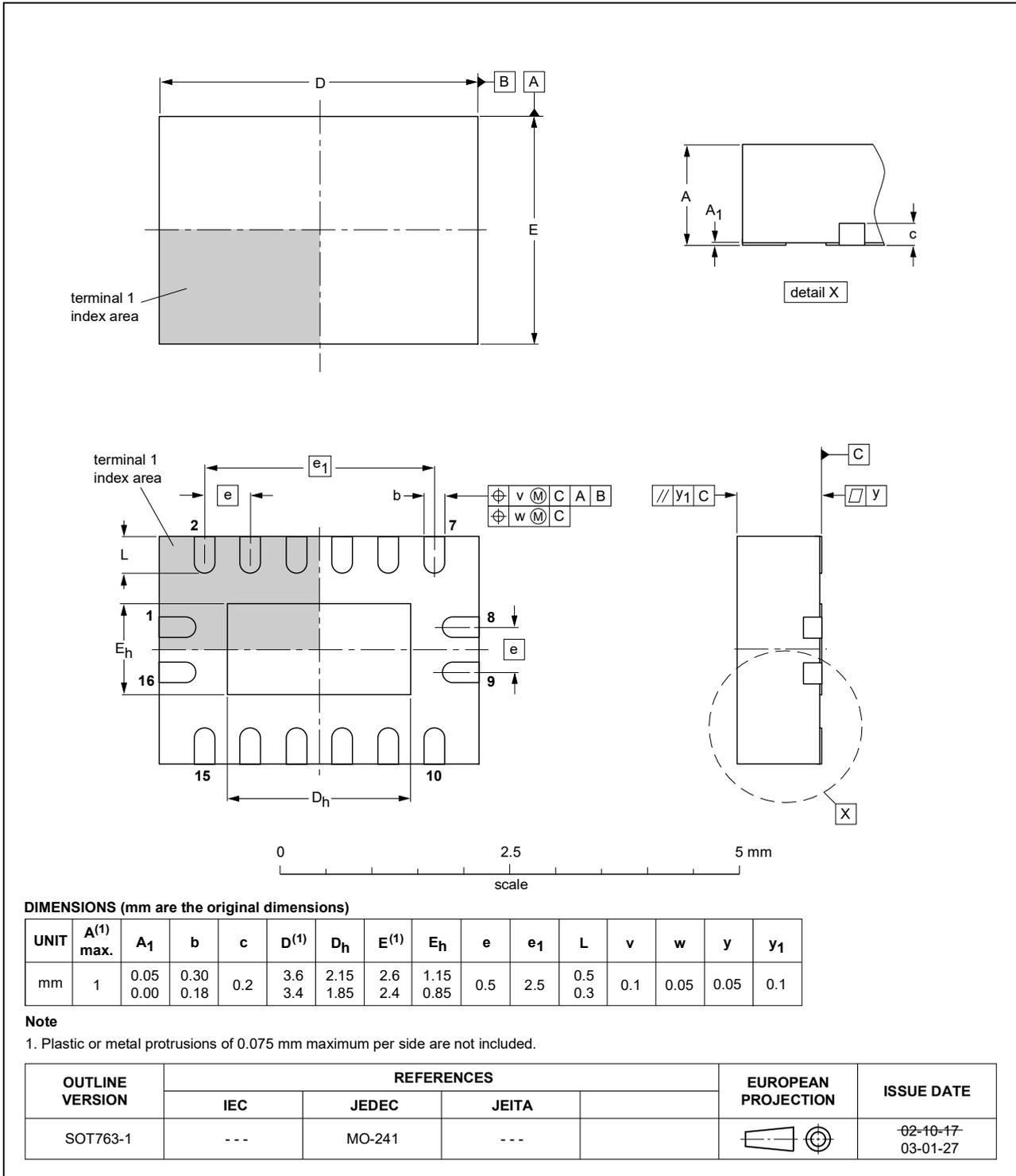


Fig. 16. Package outline SOT763-1 (DHVQFN16)

4-bit dual supply translating transceiver with configurable voltage translation; 3-state

XQFN16: plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm

SOT1161-1

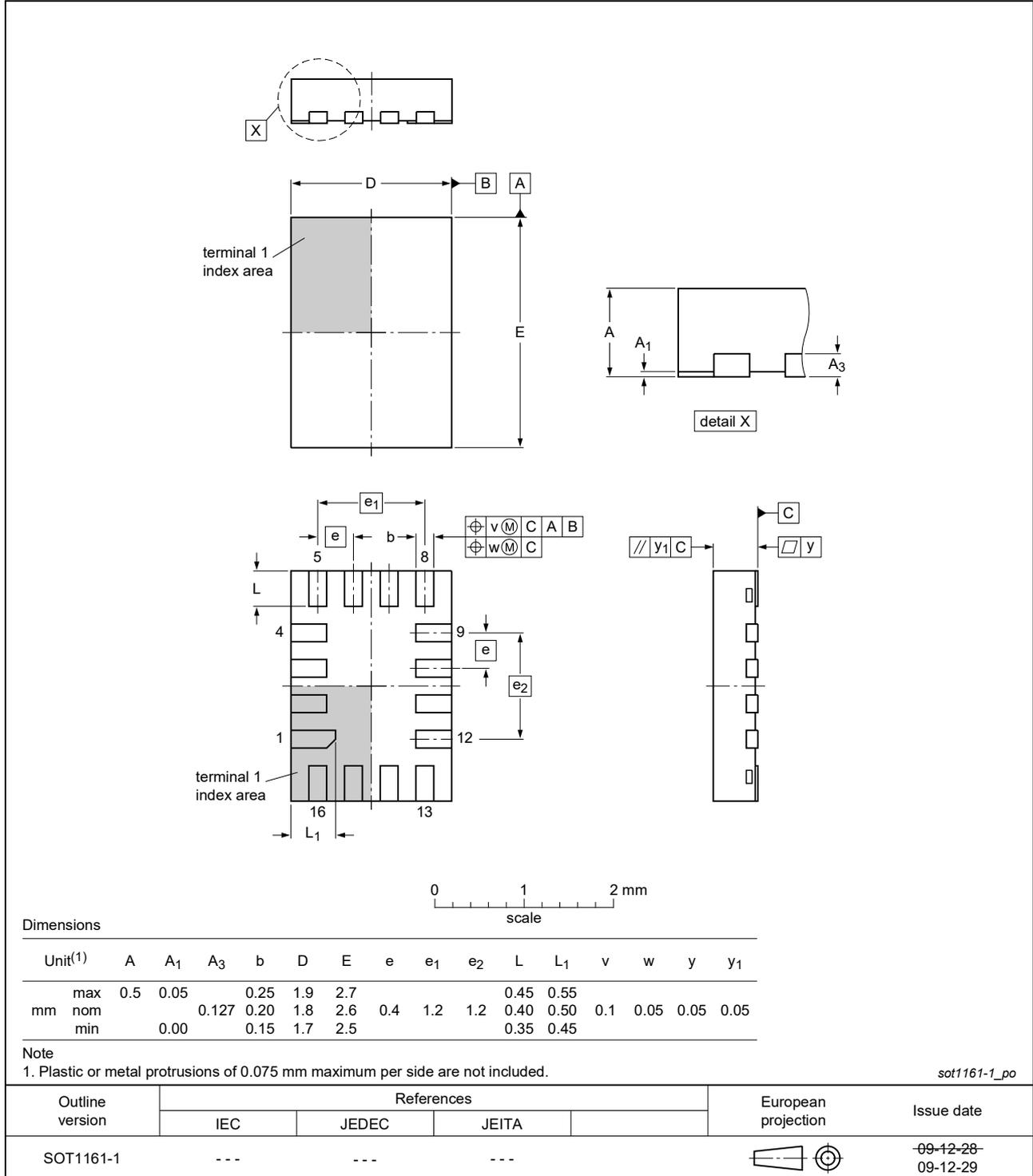


Fig. 17. Package outline SOT1161-1 (XQFN16)

14. Abbreviations

Table 17. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

15. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC4T245_Q100 v.6	20240411	Product data sheet	-	74AVC4T245_Q100 v.5
Modifications:	<ul style="list-style-type: none"> • Fig. 14, Fig. 15: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74AVC4T245_Q100 v.5	20200317	Product data sheet	-	74AVC4T245_Q100 v.4
Modifications:	<ul style="list-style-type: none"> • Section 2 updated. 			
74AVC4T245_Q100 v.4	20190613	Product data sheet	-	74AVC4T245_Q100 v.3
Modifications:	<ul style="list-style-type: none"> • Type number 74AVC4T245GU-Q100 (SOT1161-1/XQFN16) added. • Table 5: Derating values for total power dissipation (P_{tot}) have changed. 			
74AVC4T245_Q100 v.3	20190320	Product data sheet	-	74AVC4T245_Q100 v.2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. 			
74AVC4T245_Q100 v.2	20151207	Product data sheet	-	74AVC4T245_Q100 v.1
Modifications:	<ul style="list-style-type: none"> • Table 5: conditions I_{CC} and I_{GND} changed (errata). 			
74AVC4T245_Q100 v.1	20130402	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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