PD69104

Datasheet

4-Port PSE PoE Manager

March 2018

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 was published in March 2018. The format of this document was updated to the latest template.

Part marking is updated. For more information, see Ordering Information (see page 22).

Figures, punctuation, and stylistic conventions were applied to match Microsemi standards.

1.2 Revision 1.7

Revision 1.7 was published in July 2015. In revision 1.7 of this document, a NOTE was added specifying "Fuses per port are not required for use in circuits with total power level of up to 3 kW". Also, removed the "PD69104F" instances.

1.3 Revision 1.6

Revision 1.6 was published in June 2013. In revision 1.6 of this document, a full temperature range P/N was added.

1.4 Revision 1.5

Revision 1.5 was published in December 2012. In revision 1.5 of this document, Tape and Reel Data was added.

1.5 Revision 1.4

Revision 1.4 was published in February 2012. In revision 1.4 of this document, I lim was updated according to UL and IEEE standards.

1.6 Revision 1.3

Revision 1.3 was published in January 2012. In revision 1.3 of this document, the Footer address was updated.

1.7 Revision 1.2

Revision 1.2 was published in October 2011. In revision 1.2 of this document, Theta JC was added.

1.8 Revision 0.6

Revision 0.6 was published in August 2011. In revision 0.6 of this document, SPI Timing data was added.

1.9 Revision 0.5

Revision 0.5 was published in April 2011. In revision 0.5 of this document, minor corrections were made.

1.10 Revision 0.4

Revision 0.4 was published in July 2010. In revision 0.4 of this document, the catalog numbers metrology and Ordering information was updated.

1.11 Revision 0.3

Revision 0.3 was published in April 2010. In revision 0.3 of this document, minor corrections were made.

1.12 Revision 0.2

Revision 0.2 was published in January 2010. In revision 0.2 of this document, the Power Dissipation was updated.

1.13 Revision 0.1

Revision 0.1 was published in November 2009. It was the initial release of this document.

2 Product Overview

Microsemi's PD69104 Power over Ethernet (PoE) manager integrates power, analog, and state of the art logic into a single 48-pin, plastic QFN package. The device is used in Ethernet switches and midspans, enabling network devices to share power and data over the same cable. The PD69104 device is a four port, mixed-signal, high-voltage PoE driver.

The PD69104 enables detection of IEEE802.3at-2009 compliant Type 1 and Type 2 powered devices (PDs). This ensures the safe power feeding and disconnection of ports with full digital control and a minimum of external components.

The PD69104 device executes all real time functions as specified in the IEEE802.3af-2003 (AF) and IEEE802.3at-2009 high power (AT) standards, including load detection, AF, and AT classification. In addition, the PD69104 device features multiple classification attempts (MCA) port status monitoring and provides system level activities such as power management and MIB support for system management.

The PD69104 device is designed to detect and disable disconnected ports. This utilizes the DC disconnection methods as specified in the IEEE 802.3af-2003 and IEEE802.3at-2009 standards.

The PD69104 device provides PD protection such as over-load, under-load, over-voltage, and short-circuiting. It supports supply voltages ranging from 44 to 57 voltage DC (V_{DC}) with no additional power supply sources. The chip includes built-in internal thermal protection. Optionally, the PD69104 can detect legacy/pre-standard PD devices.

The PD69104 is a low power device using an internal MOSFET and an external 0.36 Ω sense resistor.

2.1 Features

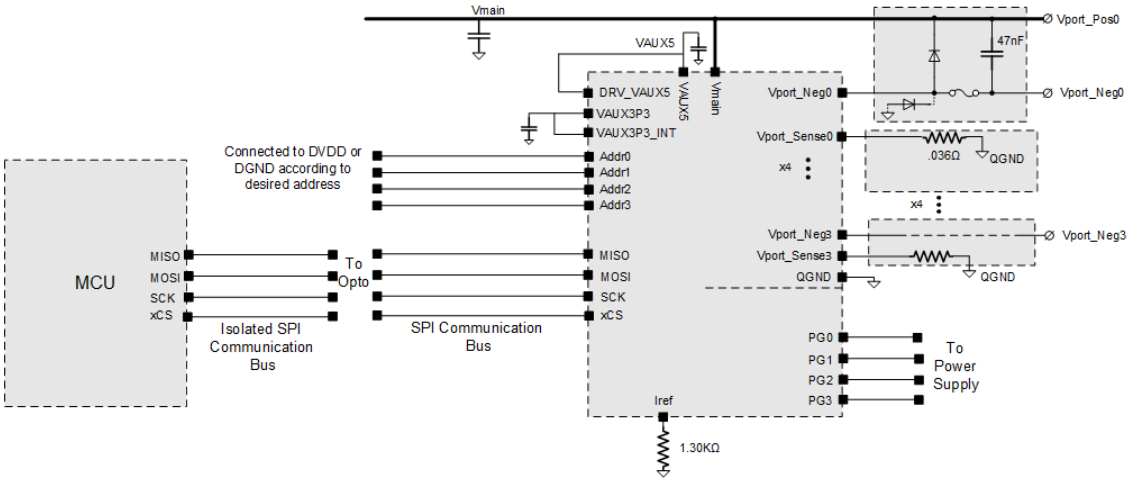
- IEEE802.3af-2003 compliant
- IEEE802.3at-2009 compliant, including two-event classification
- Supports pre-standard PD detection
- Supports Cisco devices detection
- Single DC voltage input (44 V_{DC} to 57 V_{DC})
- Input voltage out of range protection
- Wide temperature range: –10 °C to 85 °C
- Over-temperature protection
- Low power dissipation (0.36 Ω sense resistor and 0.3 Ω MOSFET Rdson)
- Includes reset command pin
- 4 × direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- Configurable AT/AF modes
- Configurable standard and legacy detection mode
- Power soft start mechanism
- On-chip thermal protection
- Voltage monitoring/protection
- Built-in 3.3 V_{DC} and 5 V_{DC} regulators
- Internal power on reset
- RoHS compliant
- MSL3
- Emergency power management supporting four configurable power bank I/Os
- Can be cascaded to up to 12 PoE devices (48 ports)

2.2 Typical Application

This typical application illustrates a simple PoE system solution for eight Ethernet ports switch or hub.

Positive (POS) and Negative (NEG) signals should be connected to the switch RJ45 jack.

Figure 1 • Typical Application



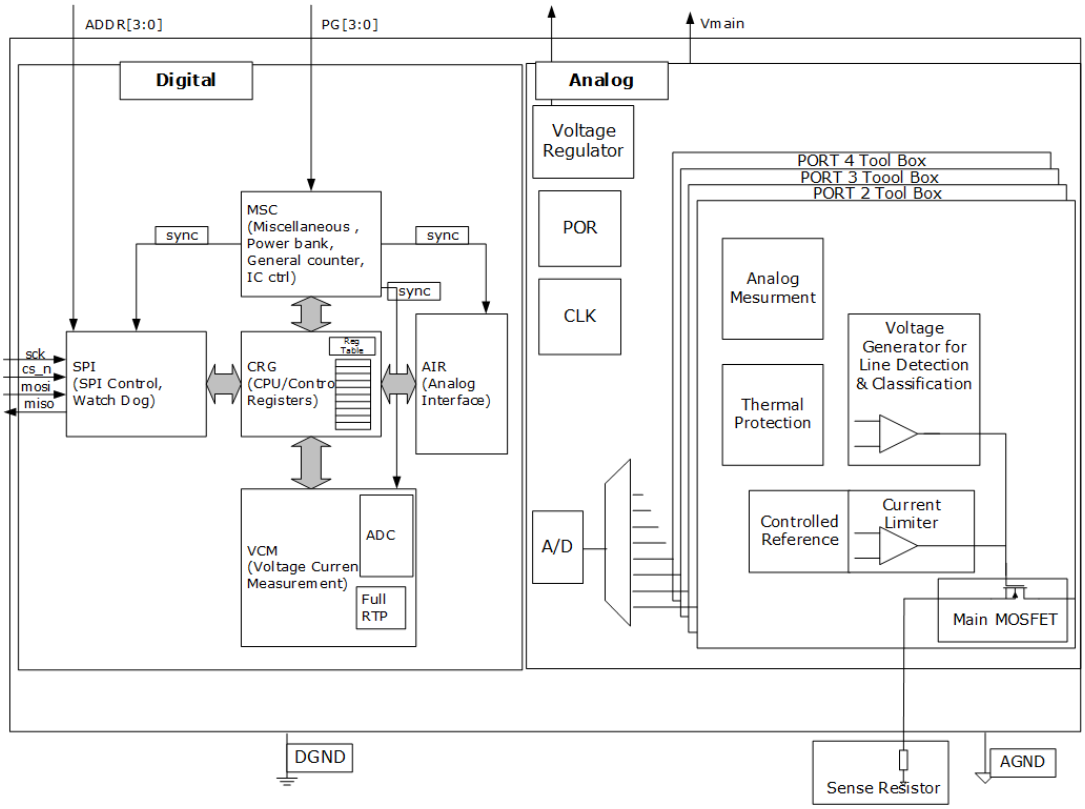
Note: Fuses per port are not required for use in circuits with total power level of up to 3 kW as the PD69104 is designed to fulfill limited power source (LPS) requirements per the latest editions of IEC60950-1 and EN60950-1.

3 Functional Descriptions

The PD69104 has two major sections: a digital section that controls and monitors the logical PoE functions (like state machines and timings) and an analog section that performs the front-end analog PoE functionality.

The following illustration shows the internal functional blocks of the PD69104 device.

Figure 2 • PD69104 Internal Block Diagram



3.1 Logic Main Control Module

The logic main control module includes the digital timing mechanisms and state machines. It synchronizes and activates the PoE functions according to the following MCU control commands:

- Real-time protection (RTP)
- Start-up macro (DVDT)
- Load signature detection (RES DET)
- Classification macro (CLASS)
- Voltage and current monitoring registers (VMC)
- ADC interfacing
- Direct digital signals with analog block

3.1.1 Line Detection Generator

Upon request from the MCU to the main control module, four different voltage levels are generated by the line detection generator. This ensures the robust AF/AT line detection functionality.

3.1.2 Classification Generator

Upon request from the MCU to the main control module, the state machine applies a regulated class event and marks event voltage to the ports. This is required by the IEEE standard.

3.1.3 Current Limiter

This circuit continuously monitors the current of powered ports and limits the current to a specific value, according to pre-defined limits as set by AF/AT and current_set pins. In cases where the current exceeds this specific level, the system starts to measure the elapsed time. If this time period is greater than a preset threshold, the port is disconnected.

3.1.4 Main MOSFET

This is the main power switching FET, used to control PoE current into the load.

3.1.5 Analog-to-Digital Converter (ADC)

A 10-bit analog-to-digital converter, used to convert analog signals into digital registers for the logic control module.

3.1.6 Power on Reset (PoR)

This circuit monitors the internal 3.3 V_{DC} levels. If this voltage drops below specific thresholds, a reset signal is generated and the PD69104 is reset.

3.1.7 Voltage Regulator

The voltage regulator generates 3.3 V_{DC} and 5 V_{DC} for the internal circuitry. These voltages are derived from the Vmain supply. To use the internal voltage regulator, connect:

- VAUX5 to DRV_VAUX5
- VAUX3P3 to VAUX3P3_INT
- REG_EN_N to AGND

There are two options to reduce the PD69104 power dissipation by regulating the voltage outside the chip:

- Use an external NPN transistor to regulate the 5 V_{DC}. In this setup, the configuration of the regulator's pins should be:
  - DRV_VAUX5 is connected to the NPN BASE
  - VAUX5 is connected to the NPN EMITTER

  (Connect the **Collector** to VMAIN)
  - VAUX3P3 is connected to VAUX3P3_INT
  - REG_EN_N is connected to AGND
- Supply the PD69104 with an external 3.3 V voltage regulator. In this setup, the configuration of the regulators pins should be:
  - VAUX5 is connected to DRV_VAUX5
  - VAUX3P3_INT is connected to VAUX5
  - VAUX3P3 is connected to the external 3.3 V
  - REG_EN_N is connected to VAUX3P3

The two options above can be implemented simultaneously.

3.1.8 CLK

CLK is an internal 8 MHz clock oscillator.

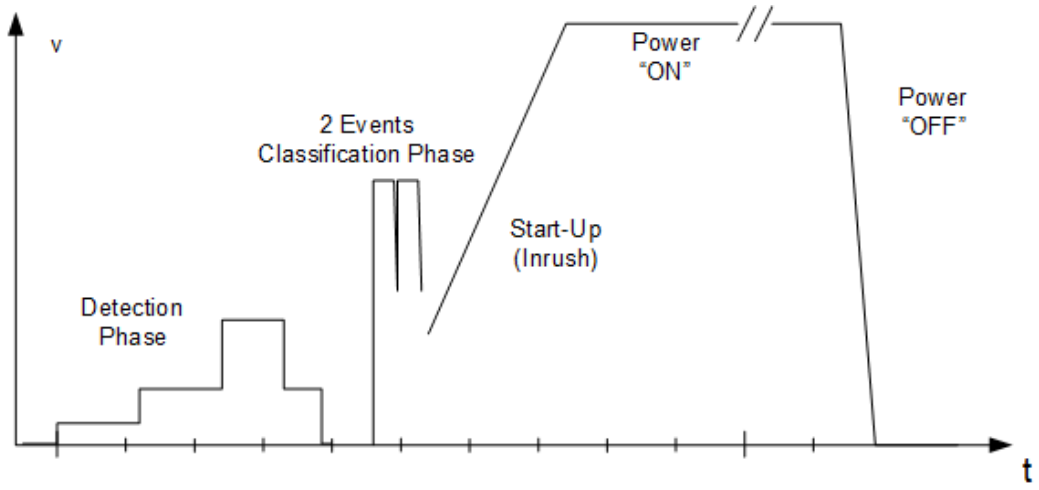
3.2 Application Information

The PD69104 performs IEEE 802.3af and IEEE 802.3at functionality, as well as legacy (capacitor) and Cisco PD detection, in addition to protections such as short circuit and dV/dT protection upon startup.

3.2.1 Line Detection

The line detection feature detects a valid AF or AT load, as specified in the AF/AT standard. The resistor value should range from 19K Ω to 26.5K Ω. Line detection is based on four different voltage levels generated over the PD (the load), as shown in the following illustration.

Figure 3 • Typical PoE Voltage Timing Diagram



3.2.2 Legacy (Capacitor) Detection

In cases where legacy is set, the PD69104's detection mechanism is configured to detect and power up legacy PDs, as well as AF/AT-compliant. This mechanism also detects and powers up Cisco legacy PDs.

3.2.3 Classification

The classification process takes place right after the resistor detection, when the resistor detection has completed successfully. The main goal of the classification process is to detect the PD class, as specified in the IEEE 802.3AF and AT standards. In AF mode, the classification mechanism is based on a single voltage level (single finger). In AT mode, the classification mechanism is based on two voltage levels (dual finger), as defined in IEEE 802.3at-2009.

3.2.4 Port Start Up

Upon a successful detection and classification process, power is applied to the load through a controlled start-up mechanism. During this period, current is limited to 425 mA for a typical duration of 65 mS, which enables the PD load to charge and to enter a steady state power condition.

3.2.5 Over-Load Detection and Port Shut Down

After power up, the PD69104 automatically initializes its internal protection mechanisms to monitor and disconnect power from the load in cases where extreme conditions (such as over-current or short port terminal scenarios) occur, as specified in the IEEE 802.3AF/AT standard.

3.2.6 Disconnect Detection

The PD69104 supports the DC disconnect function as per the IEEE 802.3AF/AT standard. This mechanism continuously monitors the load current and disconnects power in cases where the load current is below 7.5 mA (typical) for more than 322 mS.

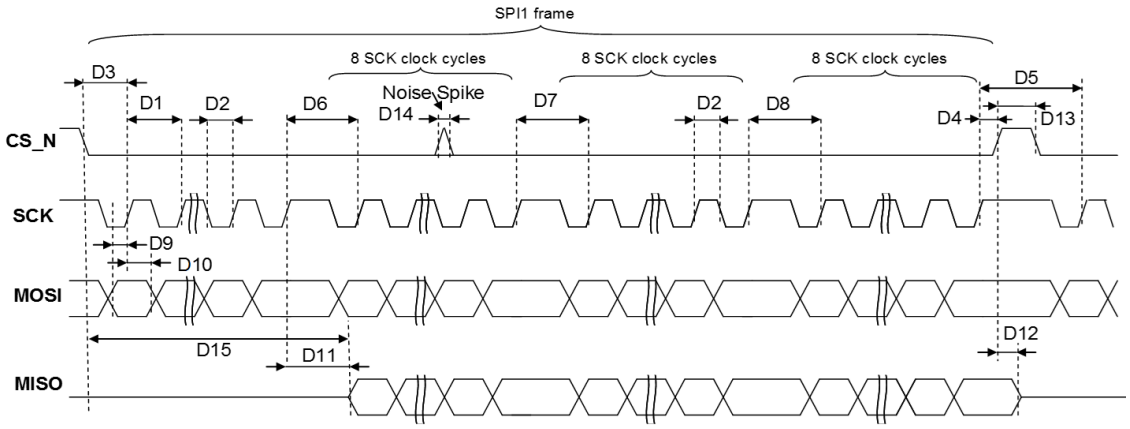
3.2.7 Over-Temperature Protection

The PD69104 has internal temperature sensors that continuously monitor the main MOSFET junction temperature and disconnect load power when the junction temperature exceeds 200 °C. This mechanism protects the device from extreme events such as high ambient temperature or other thermo-mechanical failures that may damage the PD69104.

3.2.8 V MAIN Out-of-Range Protection

The PD69104 automatically disconnects port power when Vmain exceeds 60 V_{DC}. This is an extremely valuable feature that protects the load if the main power source is faulty or damaged. The following image shows the SPI detailed timing information.

Figure 4 • SPI Detailed Timing Information



The following table shows the SPI Timing details.

Table 1 • SPI Timing Details

Name	Min Delay	Max Delay	Description
D1		714 ns	SPI clock period
D2	45 ns	55 ns	SPI duty cycle
D3	340 ns		SPI_CS setup to SPI clock positive edge (delay after SPI_CS active signal)
D4	340 ns		SPI_CS hold to SPI clock positive edge (delay before SPI_CS inactive signal)
D5	2 SPI clock cycles		Delay between last SCK in eSPI1 frame and first SCK at adjacent eSPI1 frame.
D6	1 SPI clock cycles		Between byte 0 (IC addr) and byte 1 (addr).
D7	1 SPI clock cycles		Between byte 1 (addr) and byte 2 (data).
D8	1 SPI clock cycles		Between byte 2 (MS data byte) and byte 3 (LS data byte).
D9	340 ns		MOSI setup time
D10	210 ns		MOSI hold time
D11		140 ns	MISO tri-state to valid data from clock positive edge.
D12		300 ns	MISO valid data to tri-state from SPI_CS positive edge.
D13	1 SPI clock cycles		SPI_CS width (Delay eSPI1 frame to adjacent eSPI1 frame).
D14		60 ns	Filtered glitch width
D15	D3 + 15.5 SPI clock cycles	D3 + 23.75 SPI clock cycles	MISO tri-state from SPI_CS negative edge to valid data.

4 Electrical Specifications

The following specifications apply to the operating ambient temperature.

Table 2 • PD69104 Power Supply

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Input voltage	V_{MAIN}	Supports full IEEE 802.3 functionality	44	55	57	V
Power supply current at operating mode		V_{MAIN} = 55 V			20	mA
5 V output voltage	V_{AUX5}		4.5	5	5.5	V_{DC}
3.3 V output voltage	V_{AUX3P3}		2.97	3.3	3.63	V_{DC}
3.3 V output current		Without external NPN			5	mA
		With external NPN transistor on V_{AUX5}			30	mA
3.3 V input voltage	V_{AUX3P3}	REG_EN_N pin = 3.3 V (internal reg. is disabled) VAUX3P3_INT = 5 V	3	3.3	3.6	V_{DC}

Table 3 • Digital I/O

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Input logic, high threshold	V_{IH}		2.2			V
Input logic, low threshold	V_{IL}				0.8	V
Input hysteresis voltage			0.4	0.6	0.8	V
Input high current	I_{IH}		–10		10	µA
Input low current	I_{IL}		–10		10	µA
Output high voltage	V_{OH}	For I_{OH} = –1 mA	2.4			V
Output low voltage	V_{OL}	I_{OH} = 1 mA			0.4	V

Table 4 • PoE Load Currents

Parameter	Symbol	Test Conditions/Comment	Min.	Typ.	Max.	Unit
AF, limit mode	AF_LIM		400	425	450	mA
AT limit	AT_LIM		775	850	925	mA
AT limit dynamic range	Configurable by communication	R_{SENSE} = 0.36 Ω 1% connected at Port_Sense pin	540		1200	mA

Table 5 • Main Power Switching FET

Parameter	Symbol	Typ.	Unit
On resistance	R_{DSON}	0.3	Ω
Internal thermal protection threshold		200	°C

4.1 Dynamic Characteristics

The PD69104 utilizes three current level thresholds (I_{MIN}, I_{CUT}, I_{LIM}) and three timers (T_{MIN}, T_{CUT}, T_{LIM}).

- Loads that consume I_{LIM} current for more than T_{LIM} are labeled as "short circuit state" and shut down.
- Loads that dissipate more than I_{CUT} for longer than T_{CUT} are labeled as overloads and are automatically shut down.
- If output power is below I_{MIN} for more than T_{MIN}, the PD is labeled as "no load" and is shut down.

Automatic recovery from overload and no load condition is attempted every T_{OVLREC} periods (typically, 1 second). The output power is limited to $I_{LIM,}$ which is a maximum peak current allowed at the port.

Table 6 • IEEE 802.3 AF Mode Parameters

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Automatic recovery from no load shutdown		T_{UDLREC} value, measured from port shutdown point (can be modified through control port)		1		Sec
Cutoff timer accuracy		Typical accuracy of T_{cut}		2		ms
Inrush current	I_{Inrsh}	For t = 50 ms, C_{load} =180 µF (max)	400		450	mA
Output current operating range	I_{PORT}	Continuous operation after startup period	10		350	mA
Output power available operating range	P_{PORT}	Continuous operation after startup period, at port output	0.57		15.4	W
Off-mode current	I_{MIN1}	Must disconnect for T greater than T_{UVL}	0		5	mA
	I_{MIN2}	May or may not disconnect when T is greater than T_{UVL}	5	7.5	10	mA
PD power maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Overload current detection range	I_{CUT}	Time limited to T_{OVL}	350		400	mA
Overload time limit	T_{OVL}		50		75	ms
Turn-on rise time	T_{RISE}	From 10% to 90% of V_{port} (specified for PD load consisting of 100 µF capacitor in parallel to 200 Ω)	15			µs
Turn-off time	T_{OFF}	From V_{port} to 2.8 V_{DC}			500	ms
Time maintain power signature	T_{MPS}	DC modulation time for DC disconnect		49		ms

Table 7 • IEEE 802.3 AT Mode Parameters

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Automatic recovery from no load shutdown		T_{UDLREC} value, measured from port shutdown point (can be modified through control port)		1		Sec
Cutoff timer accuracy		Typical accuracy of T_{cut}		2		ms
Inrush current	I_{Inrsh}	For t = 50 ms, C_{load} = 180 µF (max)	400		450	mA
Output current operating range	I_{PORT}	Continuous operation after startup period	10		600	mA
Output power available operating range	P_{PORT}	Continuous operation after startup period, at port output	0.57		36	W
Off-mode current	I_{MIN1}	Must disconnect when T is greater than T_{UVL}	0		5	mA
	I_{MIN2}	May or may not disconnect when T is greater than T_{UVL}	5	7.5	10	mA
PD power maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Overload current detection range	I_{CUT}	Time limited to T_{OVL}	600		775	mA
Overload time limit	T_{OVL}		50		75	ms
Turn-on rise time	T_{RISE}	From 10% to 90% of V_{port} (specified for PD load consisting of 100 µF capacitor in parallel to 200 Ω).	15			µs
Turn-off time	T_{OFF}	From V_{port} to 2.8 V_{DC}			500	ms
Time maintain power signature	T_{MPS}	DC modulation time for DC disconnect		49		ms

4.2 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the PD69104 device.

Exceeding these ratings can cause damage to the device. All voltages are with respect to ground. Currents are marked positive when flowing into a specified terminal and marked negative when flowing out of a specified terminal.

Table 8 • Absolute Maximum Ratings

Parameter	Rating
Supply input voltage (V_{MAIN})	–0.3 V_{DC} to 74 V_{DC}
Port_Neg [0..7] pins	–0.3 V_{DC} to 74 V_{DC}
Port_Sense [0..7] pins	–0.3 V_{DC} to 3.6 V_{DC}
QGND, GND pins	–0.3 V_{DC} to 0.3 V_{DC}
All other pins	–0.3 V_{DC} to 3.6 V_{DC}
Operating ambient temperature range	–10 °C to 85 °C
Maximum operating junction temperature	150 °C
Storage temperature range	–65 °C to 150 °C
ESD protection at all I/O pins	±2 KV (HBM)

4.3 Power Dissipation Information

The following table shows the power dissipation values of the respective parameters.

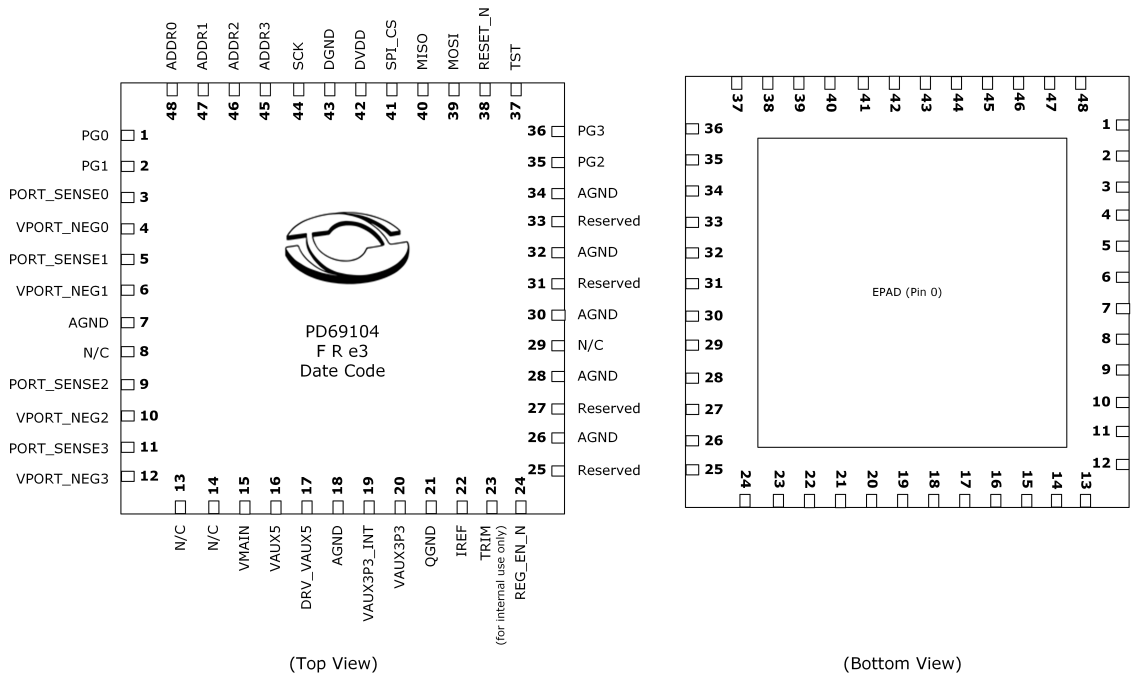
Table 9 • Power Dissipation

Parameter	Value
Rsense power dissipation	0.36 Ω × I_{PORT}^2
Rds_ON power dissipation	0.3 Ω × I_{PORT}^2
Pport_AF= 15.4 W	PRsense = 28.2 mW
	PRds_ON = 23.4 mW
Pport_AT= 30 W	PRsense = 107 mW
	PRds_ON = 88.5 mW
PD69104 self power dissipation (including internal 3.3 V regulator)	1.1 W
PD69104 8 ports AF application power dissipation	1.1 W + [4 × (28.2 mW + 23.4 mW)] = 1.31 W
PD69104 8 ports AT application power dissipation	1.1 W + [4 × (107 mW + 88.5 mW)] = 1.88 W
PD69104 self power dissipation (including external 3.3 V regulator)	0.5 W
PD69104 AF 8 ports application power dissipation	0.5 W + [4 × (28.2 mW + 23.4 mW)] = 0.55 W
PD69104 8 ports AT application power dissipation	0.5 W + [4 × (107 mW + 88.5 mW)] = 1.28 W

5 PD69104 Pin Description

The following illustrations shows the top an bottom views of the pin diagram for the PD69104 device.

Figure 5 • PD69104 Pinout



- PD69104 for –10 °C to 85 °C operating ambient temperature range

The following table shows the pin details for the PD69104 device.

Table 10 • Pin Descriptions

Number	Name	Type	Description
0	Exposed PAD	Analog ground	Exposed pad; metal plate on the IC bottom side connected to analog ground. A high-quality ground plane (about 500 mil. inch over 500 mil. inch) should be deployed around this pin whenever possible.
1	PG0	Digital input	Power supply monitoring
2	PG1		
3	PORT_SENSE0	Analog input	Sense resistor port input (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
4	VPORT_NEG0	Analog I/O	Negative port output
5	PORT_SENSE1	Analog input	Sense resistor port input (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
6	VPORT_NEG1	Analog I/O	Negative port output
7	AGND	Power	Analog ground
8	N/C	Power	Not connected

Number	Name	Type	Description
9	PORT_SENSE2	Analog input	Sense resistor port input (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
10	VPORT_NEG2	Analog I/O	Negative port output
11	PORT_SENSE3	Analog input	Sense resistor port input (Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
12	VPORT_NEG3	Analog I/O	Negative port output
13	N/C	Analog I/O	Test pin (for production use only); keep open (not connected).
14	N/C		
15	VMAIN	Power	Supplies voltage for the internal analog circuitry. A low ESR 1 uF (or higher) bypass capacitor, connected to AGND, should be placed as close as possible to this pin through low resistance traces.
16	VAUX5	Power	Regulated 5 V_{DC} output voltage source; it needs to be connected to a filtering capacitor of 4.7 uF or higher. If an external NPN is used to regulate the voltage, connect this pin to the "Emitter" (the "collector" should be connected to Vmain).
17	DRV_VAUX5	Power	Zapping input for IC production trimming. Should be connected to DVDD.
18	AGND	Power	Analog ground.
19	VAUX3P3_INT	Power	Connected to VAX3P3 (pin 20) if internal 3.3 V_{DC} regulator is used. Connect to VAUX5 (pin 16) if external 3.3 V_{DC} regulator is used.
20	RESET_N	Power	Regulated 3.3 V output voltage source. A 4.7 µF or higher filtering capacitor should be connected between this pin and AGND. When an external 3.3 V_{DC} regulator is used, connect it to this pin to supply the chip.
21	QGND	Power	Quiet analog ground.
22	IREF	Analog input	Reference resistor pin. Connect a 30.1 kΩ 1% resistor to QGND.
23	TRIM	Analog input	Trimming input for IC production. It should be connected to VAUX3P3.
24	REG_EN_N	REG_EN_N	Enable/Disable the internal 3.3 V_{DC} regulator in case an external 3.3 V_{DC} is used to supply the chip. • GND: Internal regulator enabled • 3.3 V_{DC}: Internal regulator disabled
25	Reserved	Analog I/O	Keep this pin open (disconnected)
26	AGND		Connect to analog ground
27	Reserved		Keep this pin open (disconnected)
28	AGND		Connect to analog ground
29	N/C		Not connected
30	AGND	Power	Analog ground
31	Reserved		Keep this pin open (disconnected)
32	AGND		Connect to analog ground
33	Reserved		Keep this pin open (disconnected)
34	AGND		Connect to analog ground
35	PG2	Digital input	Power supply monitoring

Number	Name	Type	Description
36	PG3		
37	TST	Digital I/O	Test pin for production use only. Keep connected to DGND.
38	RESET_N	Digital input	Reset input; active low ('0' = reset) An external 10K pull-up resistor should be connected between this pin and DVDD.
39	MOSI	Digital input	SPI bus, master data out/slave in
40	MISO	Digital output	SPI bus, master data in/slave out
41	SPI_CS	Digital input	SPI bus, chip select
42	DVDD	Power	Digital 3.3 V input. It needs to be connected to filtering capacitor of 1 uF.
43	DGND	Digital I/O	Digital GND
44	SCK	Digital input	SPI bus, Serial clock input
45	ADDR3	Digital input	SPI address bit 3 to set chip address.
46	ADDR2	Digital input	SPI address bit 2 to set chip address.
47	ADDR1	Digital input	SPI address bit 1 to set chip address.
48	ADDR0	Digital input	SPI address bit 0 to set chip address.

5.1 Address Pin Description (ADDR<3:0>)

Note: 0= Connect to DGND (digital ground), 1= connect to DVDD (3.3 V).

The following table represents the address details:

Table 11 • Address Pin Description

ADDR3	ADDR2	ADDR1	ADDR0	SPI ADDRESS [HEX]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E - **Broadcast** [1]
1	1	1	1	F

Note:

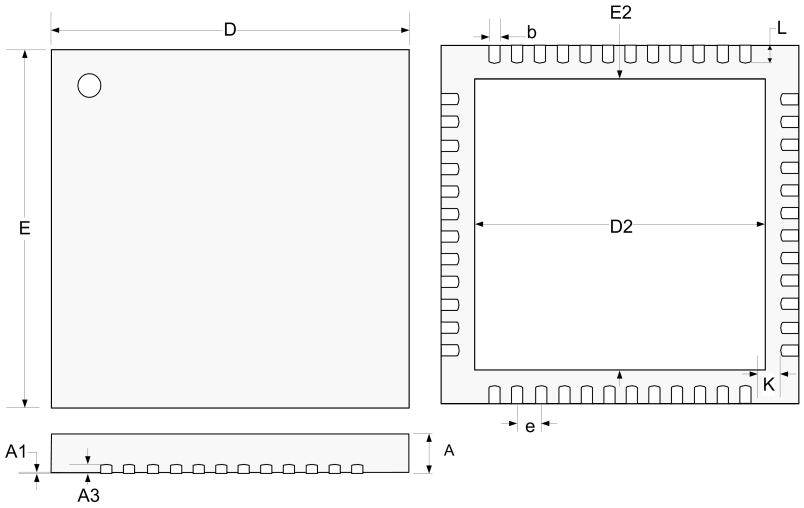
1. This address is used for Broadcast. Do not set any PD69104s in the system to this address.

6 Package Specification

This section provides the package drawing, RoHS and solder reflow information, and thermal specifications for the PD69104 device.

The PD69104 package is a 8 mm × 8 mm, 48-pin QFN, as shown in the following illustration.

Figure 6 • QFN Package



The dimensions do not include protrusions; these shall not exceed 0.155 mm (.006”) on any side. Lead dimension shall not include solder coverage.

The following table lists the dimensions for the QFN package.

Table 12 • Package Dimensions

Dimension	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.35	6.60	0.250	0.260
E2	6.35	6.60	0.250	0.260
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

6.1 RoHS and Solder Reflow Information

The PD69104 device is rated RoHS 6/6. The package is lead(Pb)-free with a 100% matte tin finish. The package peak temperature for solder reflow (40 seconds maximum exposure) is 260 °C (0 °C, –5 °C).

Note: Exceeding these ratings can cause damage to the device.

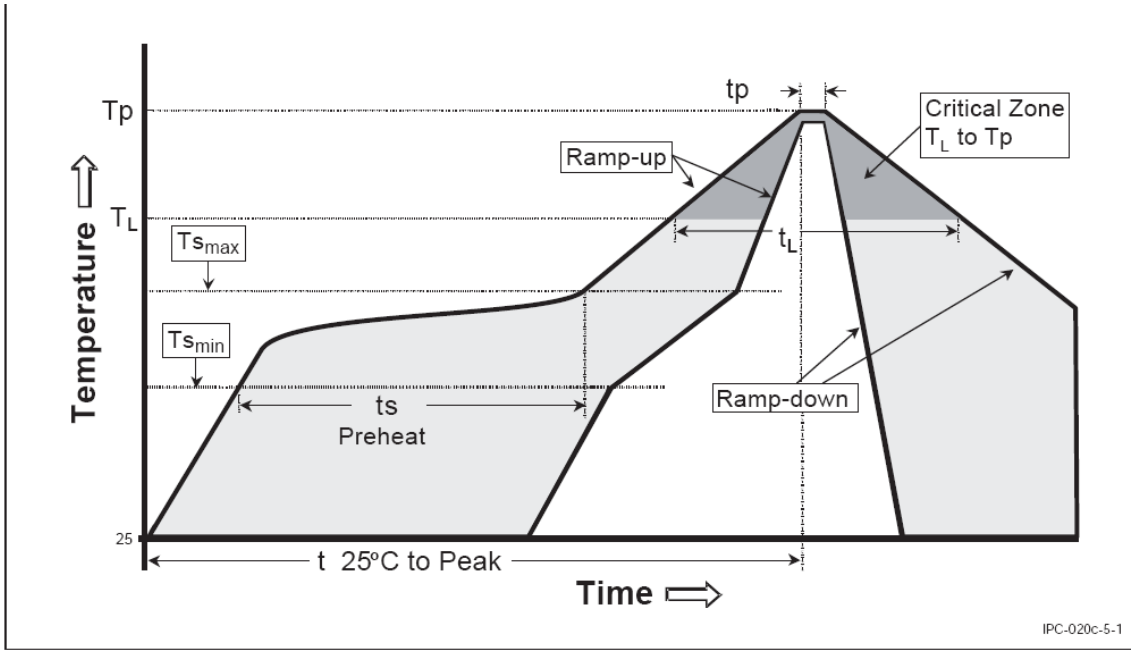
The following table shows the classification reflow profile information.

Table 13 • Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Average ramp-up rate (TS_{max} to Tp)	3 °C/s max
Preheat Temperature min (TS_{min}) Temperature max (TS_{max}) Time (ts_{min} to ts_{max})	150 °C 200 °C 60–180 s
Time maintained Temperature (T_L) Time (t_L)	217 °C 60–150 s
Peak classification temperature (T_P)	240 - 255 °C
Time within 5 °C of actual peak temperature (tp)	20–40 s
Ramp-down rate	6 °C/s max
Time 25 °C to peak temperature	8 minutes max

Note: All temperatures refer to topside of the package, measured on the package body surface.

Figure 7 • Classification Reflow Profile Diagram



6.2 Thermal Specifications

The following table lists the thermal specifications for the PD69104 device.

Table 14 • Thermal Specifications

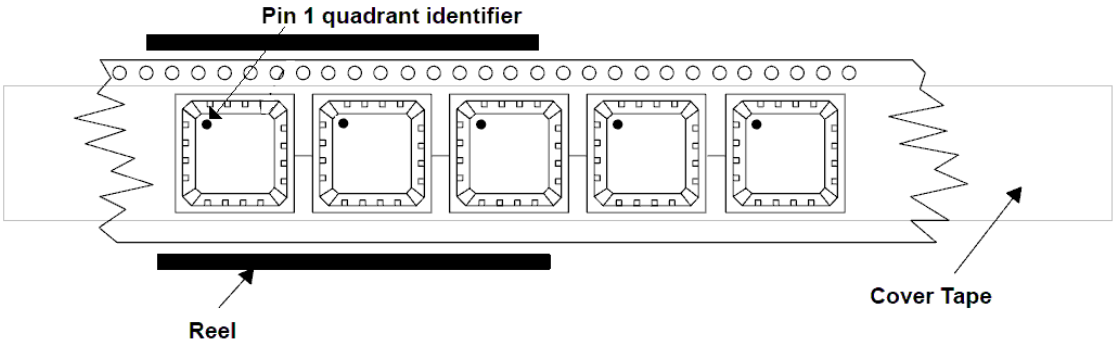
Parameter	Value
Typical thermal resistance: junction to ambient	25 °C/W
Typical thermal resistance: junction to case	4 °C/W

The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All specifications assume no ambient airflow.

6.3 Tape and Reel Packaging Information

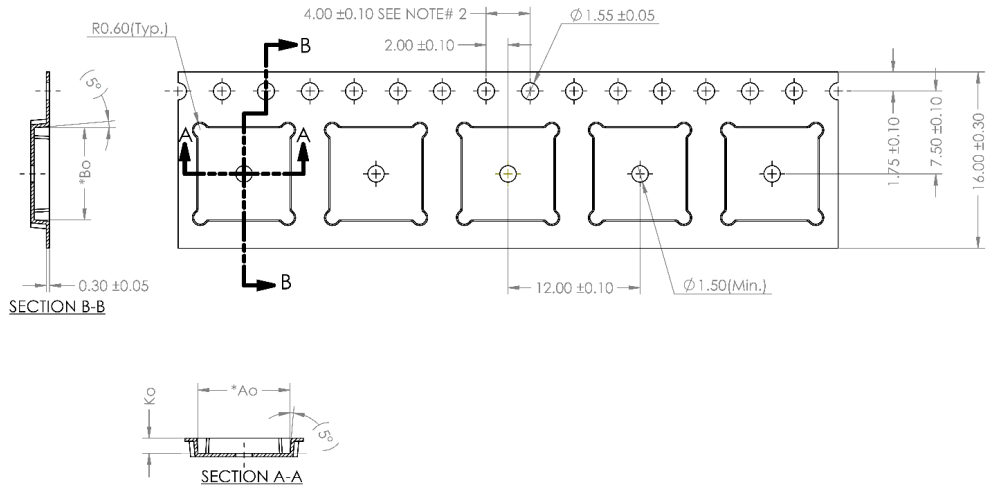
The following figure shows the Pin-1 orientation of QFN packages:

Figure 8 • Pin-1 Orientation of QFN Packages Diagram



The following figures represents the tape and reel shipment specifications.

Figure 9 • Tape Shipment Specifications



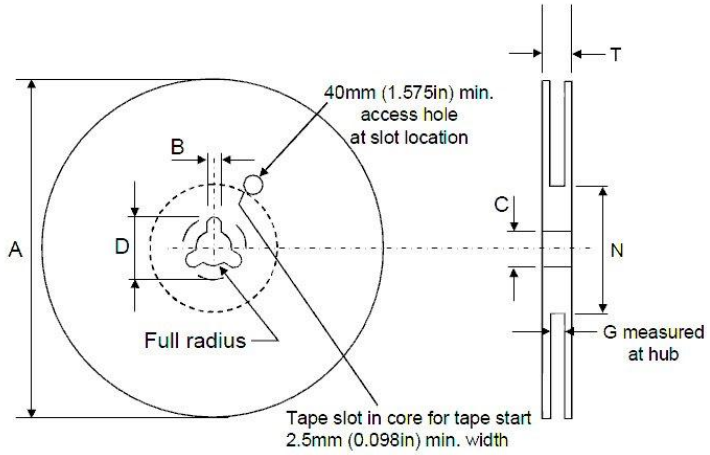
The following table shows the tape mechanical data:

Table 15 • Tape Mechanical Data

Dimensions	(mm)
Ao	8.35 ±0.10
Bo	8.35 ±0.10
Ko	1.40 ±0.10
K1	N/A
Pitch	12.00 ±0.10
Width	16.00 ±0.30

The following image shows the reel shipment specifications for the PD69104 device.

Figure 10 • Reel Shipment Specifications



The following table lists the reel specification details:

Table 16 • Reel Mechanical Data

	mm	inch
Tape size	16.00 ± 0.3	0.630 ± 0.012
A max	330	13”
B max	1.5	0.059
C	13.0 ± 0.20	0.512 ± 0.008
D min	20.2	0.795
N min	50	1.968
G	16.4 + 2.0/–0.0	0.645 + 0.079/–0.0
T max	29	1.142
Base quantity	2000 pcs	

7 Ordering Information

The following table lists the ordering information for the PD69104 device.

Table 17 • Ordering Information

Part Number	Package	Packaging Type	Temperature	Part Marking
PD69104ILQ	Plastic 48-pin QFN: 8 mm × 8 mm	Tray	–10 °C to 85 °C	Microsemi Logo PD69104 FR e3 YYWWAZZ

Note: Available in tape and reel. Append the letters “TR” to the part number.

1. FR e3: F = FAB Code, R = Product Revision Code, and e3 = 2nd Level Interconnect.
2. YY = Year, WW = Week, A = Assembly Location, ZZ = Assembly Lot Sequence Code.

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