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NE555DR

GENERAL PURPOSE TIMER

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Features

- Static current is small, with a typical 2.7mA.
- The chip's input pin can cause the IC to power down when disabled.
- The static current is small during power failure, with a typical value of 65uA.
- Output power exceeds 250mW when using a 32Ω load.
- Distortion small 0.5% TYP.
- In the audio frequency band, gain can be adjusted from 0dB to 46dB.
- Peripheral components are few.
- Compact package: SOP8

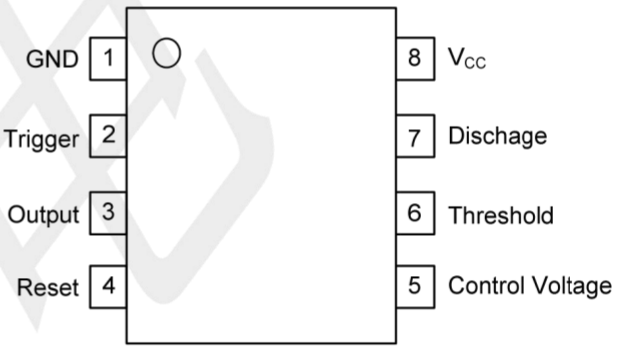
Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing Pulse detector

General Description

The NE555 is a highly stable timer integrated circuit. It can be operated in both Astable and Monostable mode. With monostable operation, the time delay is precisely controlled by one external and one capacitor. With a stable operation as an oscillator the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor.

Pinout (top view)



SOP8

Pin Configurations

Pin Number	Pin Name	Pin Function
1	GND	Supply ground
2	TRIGGER	Start timer input; (Active LOW)
3	OUTPUT	Timer logic level output
4	RESET	Timer inhibit input; (Active LOW)
5	CONTROL VOLTAGE	Timing capacitor upper voltage sense input
6	THRESHOLD	Timing capacitor lower voltage sense input
7	DISCHARGE	Timing capacitor discharge output
8	VCC	Supply voltage

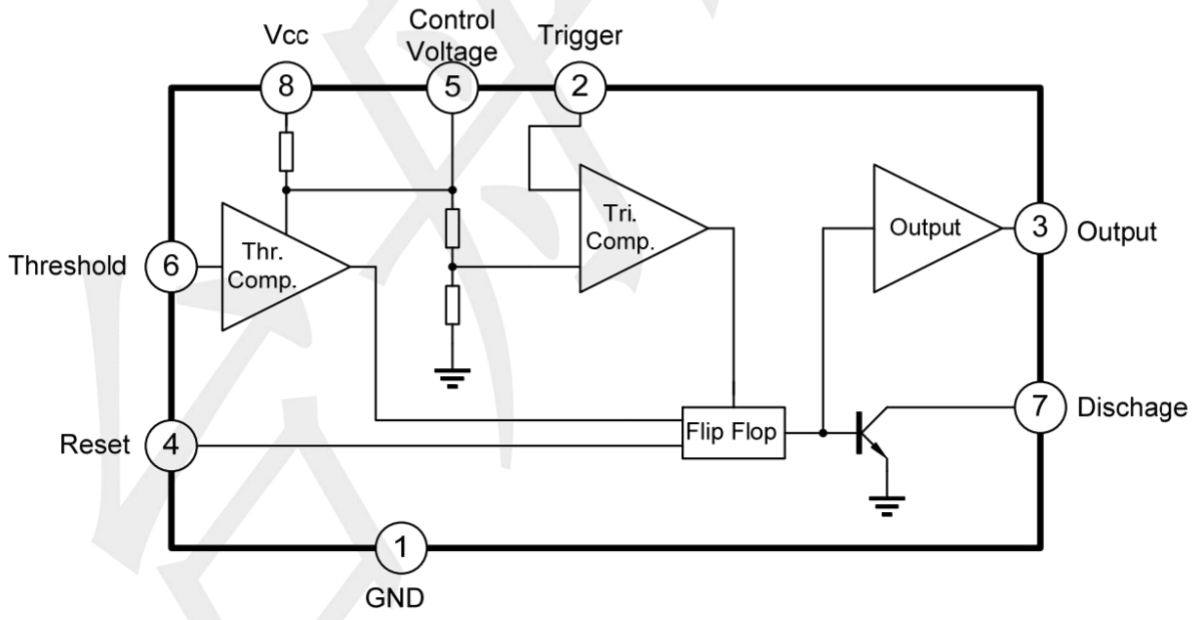
Absolute Maximum Ratings

At 25°C free-air temperature (unless otherwise noted)

Symbol	Parameter	MIN	MAX	UNIT
Vcc	Collector to emitter voltage	--	18	V
PD	Power Dissipation	--	600	mW
Tamb	Operating Temperature	0	+70	℃
TJ	Operating virtual junction temperature	--	+150	℃
TSTG	Storage temperature range	-65	+150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

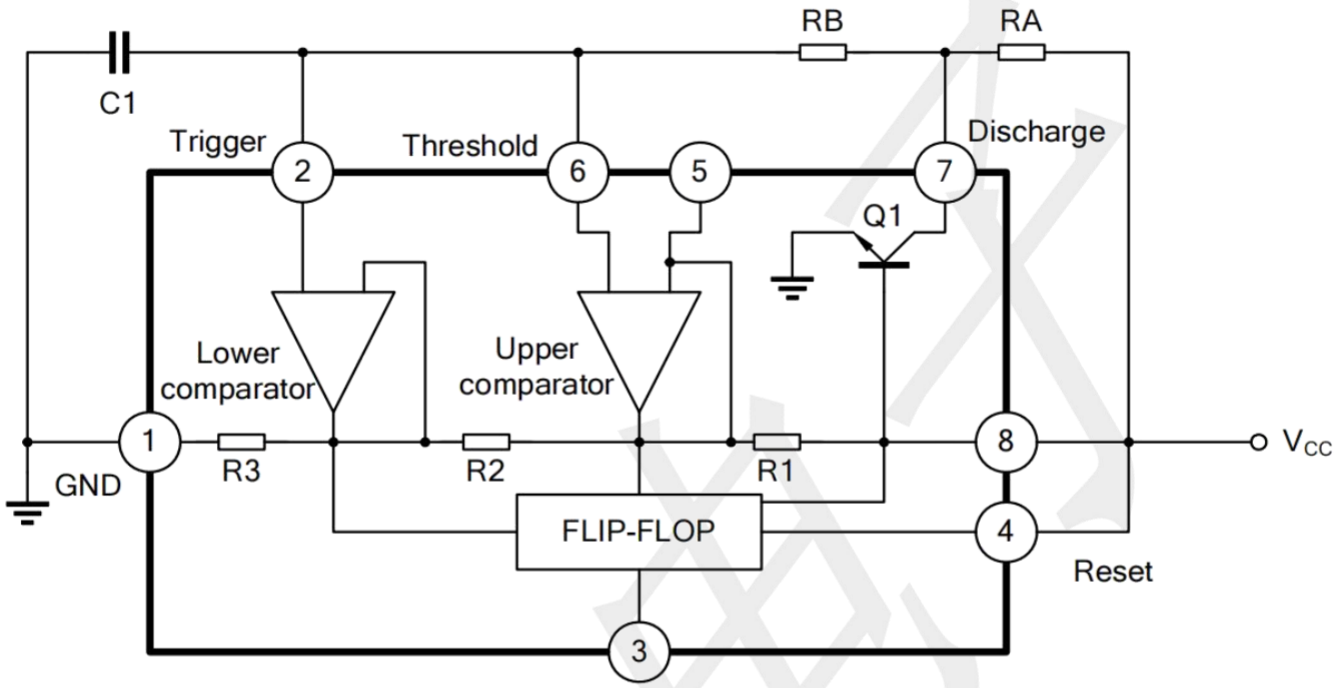
BLOCK DIAGRAM



Electrical Characteristics(TA=+25℃, unless otherwise specified)

SYMBOL	PARAMETER	Test Conditions	MIN	TYP	MAX	UNIT
VCC	Collector to Emitter voltage		4.5	--	16	V
ICCQ	Supply Current	VCC=5V, RL=∞	--	3.0	6.0	mA
		VCC=15V, RL=∞	--	10	15	mA
VTH	Threshold Voltage		--	0.667	--	V
ITH	Threshold Current		--	0.1	0.25	uA
VTR	Trigger Voltage	VCC=15V	--	5.0	--	V
		VCC=5V	--	1.67	--	V
ITR	Trigger Current		--	0.5	0.9	uA
VR	Reset Voltage		0.4	0.5	1.0	V
IR	Reset Current		--	0.1	0.4	mA
VCON	control voltage	VCC=15V	9.0	10	11	V
		VCC=5V	2.6	3.33	4.0	V
I7(IEAK)	7-terminal leakage current	Output High Level	--	1.0	100	nA
I7(SAT)	7-end saturation pressure drop	Output low level VCC=15V, I7=15mA	--	180	--	mV
		Output low level VCC=4.5V, I7=4.5mA	--	80	200	mV
VOH	Output Voltage (High)	VCC=15V,I7=200mA	--	12.5	--	V
		VCC=15V,I7=100mA	12.75	13.3	--	V
		VCC=5V,I7=100mA	2.75	3.3	--	V
VOL	Output Voltage (Low)	VCC=15V,ISINK=10mA	--	0.1	0.25	V
		VCC=15V,ISINK=50mA	--	0.4	0.75	V
		VCC=15V,ISINK=100mA	--	2.0	2.5	V
		VCC=15V,ISINK=200mA	--	2.5	--	V
		VCC=5V,ISINK=5mA	--	0.25	0.35	V
tR	Rise Time of Output		--	100	--	nS
tF	Fall Time of Output		--	100	--	nS
tE	Initial Precision	Monostable state RA.RB = 1~100K C = 0.1μF VCC = 5V (15V)	--	1.0	--	%
tT	Rate of change with temperature drift		--	50	--	ppm/°C
tV	Voltage drift rate change		--	0.1	--	%/V
tOPr	Accuracy within the operating temperature range		--	1.5	--	%
tE1	Initial Precision	Oscillatory state RA.RB = 1~100K C = 0.1μF VCC = 5V (15V)	--	2.25	--	%
tT1	Rate of change with temperature drift		--	150	--	ppm/°C
tV1	Voltage drift rate change		--	0.3	--	%/V
tOPr1	Accuracy within the operating temperature range		--	3.0	--	%

TYPICAL APPLICATION CIRCUIT



TYPICAL APPLICATION NOTES

The application circuit shows astable mode configuration.

Pin 6 (Threshold) is tied to Pin 2 (Trigger) and Pin 4 (reset) is tied to V_{CC} (Pin 8). The external capacitor C1 of Pin 6 and Pin 2 charges through R_A, R_B and dischages through R_B only. In the internal circuit of **NE555**, one input of the upper comparator is at voltage of 2/3V_{CC} (R1=R2=R3),another input is connected to Pin 6.As soon as C1 is charging to higher than 2/3V_{CC}, transistor Q1 is turned ON and discharge C1 to collector voltage of transistor Q1. Therefore, the flip-flop circuit is reset and output is low. One input of lower comparator is at voltage of 1/3Vcc, discharge transistor Q1 turn off and C1 charges through RA and RB. Therefore, the flip-flop circuit is set output high. That is, when C1 charges through R_A and R_B, output is high and when C1 discharge through R_B ,output is low. The charge time(output is high) t1 is 0.693(R_A+R_B) C1 and the discharge time (output is low) T2 is 0.693 R_B×C1.

$$\ln\frac{V_{CC}-\frac{1}{3}V_{CC}}{V_{CC}-\frac{2}{3}V_{CC}}=0.693$$

$T1=0.693\times(R_A+R_B)\times C1$

$T2=0.693\times R_B\times C1$

Thus the total period time T is given by
$T=T1+T2=0.693(R_A+2R_B)\times C1$.

Then the frequency of astable mode is given by

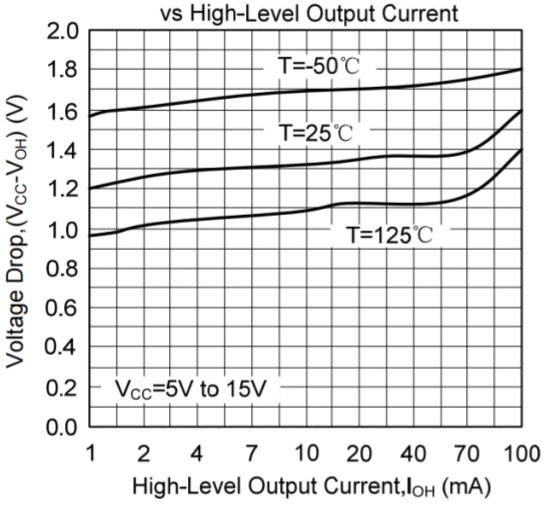
$$f=\frac{1}{T}=\frac{1.44}{(R_A+2R_B)\times C1}$$

The duty cycle is given by

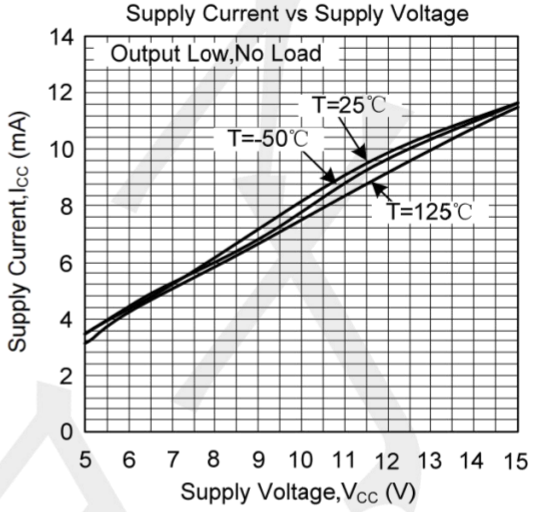
$$D.C.=\frac{T2}{T}=\frac{R_B}{R_A+2R_B}.$$

TYPICAL CHARACTERISTICS

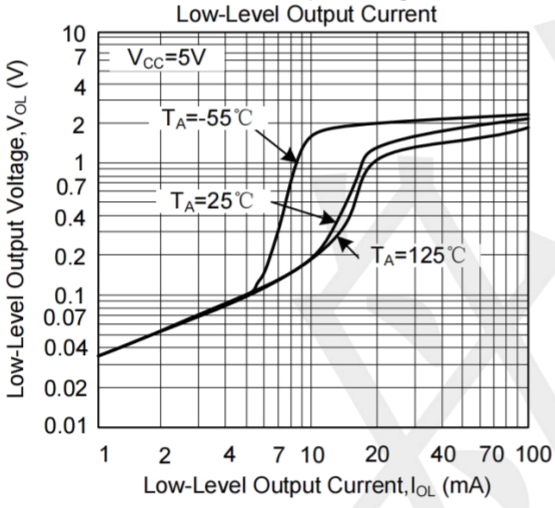
Drop Between Supply Voltage and Output vs High-Level Output Current



Supply Current vs Supply Voltage



Low-Level Output Voltage vs Low-Level Output Current



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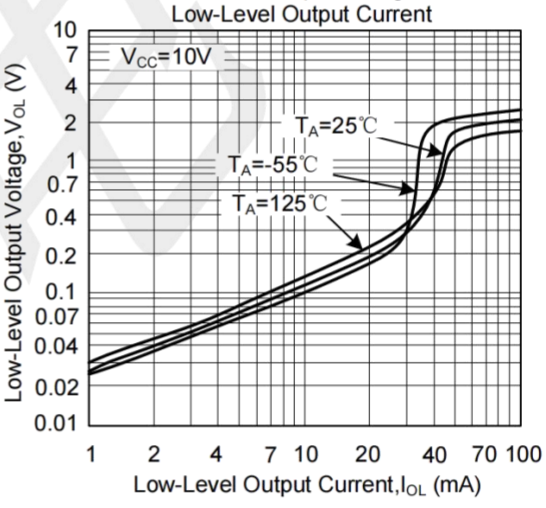

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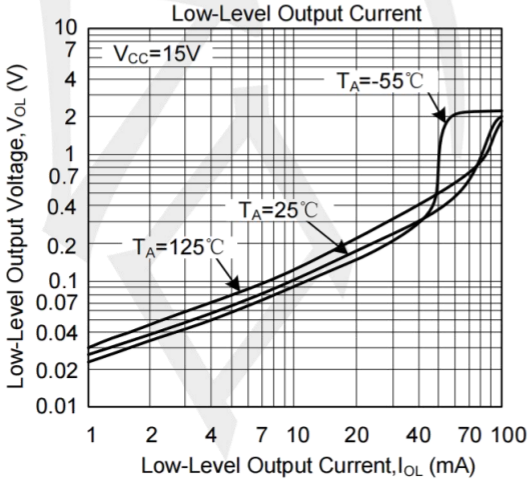
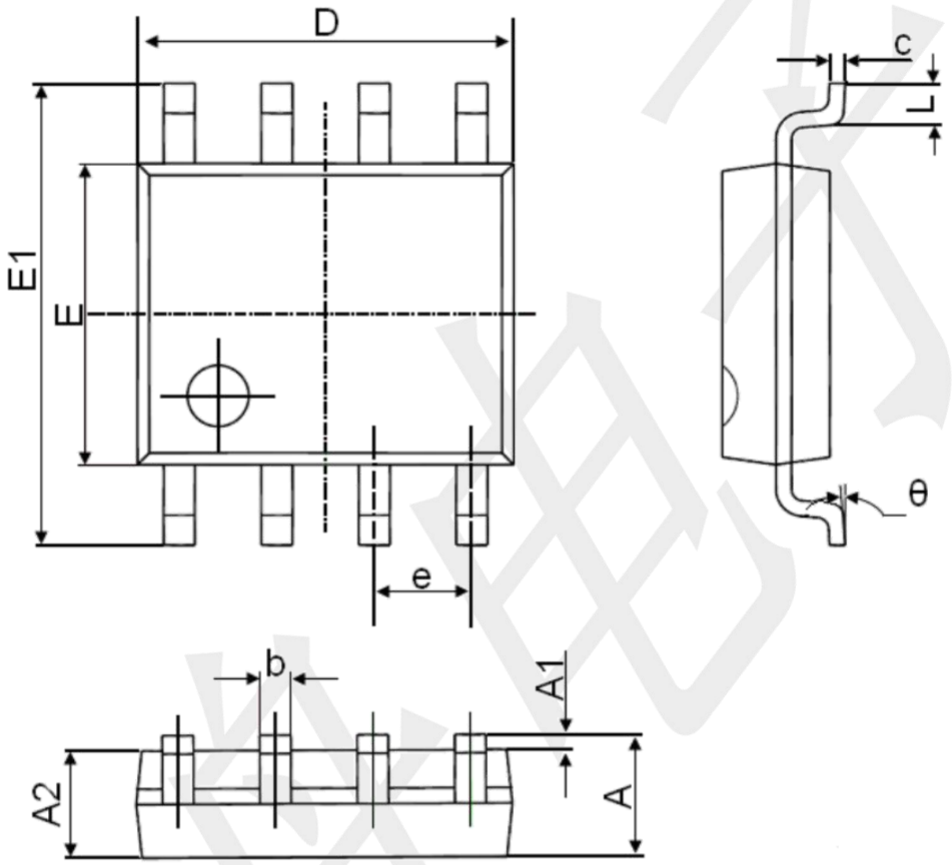


Package Outline Dimensions

SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°