WS3203

High Power/High Efficiency PoE Interface and DC/DC Controller

FEATURES

- Powers up to 15 W (input) PDs
- DC/DC Control Optimized for Isolated Converters
- Supports High-efficiency Topologies
- Complete PoE Interface
- Enhanced Classification per IEEE 802.3af with Status Flag
- Adapter ORing Support
- Programmable Frequency with Synchronization
- Robust 85V, 0.4 Ω Hotswap MOSFET
- –40°C to 125°C Junction Temperature Range
- Industry Standard HTSSOP-14

APPLICATIONS

- IEEE 802.3at Compliant Devices
- Video and VoIP Telephones
- RFID Readers
- Multiband Access Points
- Security Cameras

DESCRIPTION

The WS3203 is a combined Power over Ethernet(PoE) powered device (PD) interface and current-mode dc/dc controller optimized specifically for isolated converters. The PoE interface supports the IEEE 802.3at standard as a 13W, type1 PD.The requirements for an IEEE 802.3at type1 device are a superset of IEEE 802.3-2008(originally 802.3af) requirements.

The WS3203 supports a number of input voltage ORing options including highest voltage, external adapter preference, and PoE preference. These features allow the designer to determine which power source will carry the load under all conditions.

The PoE interface features the new extended hardware classification necessary for compatibility with high-power midspan power sourcing equipment (PSE) per IEEE 802.3at. The detection signature pin can also be used to force power from the PoE source off. Classification can be programmed to any of thedefined types with a single resistor.

The dc/dc controller features internal softstart, bootstrap startup source, current-mode compensation, and a 78% maximum duty cycle. A programmable and synchronizable oscillator allows design optimization for efficiency and eases use of the controller to upgrade existing power supply designs. Accurate programmable blank, with a default period, simplifies the usual current sense filter design trade-offs.

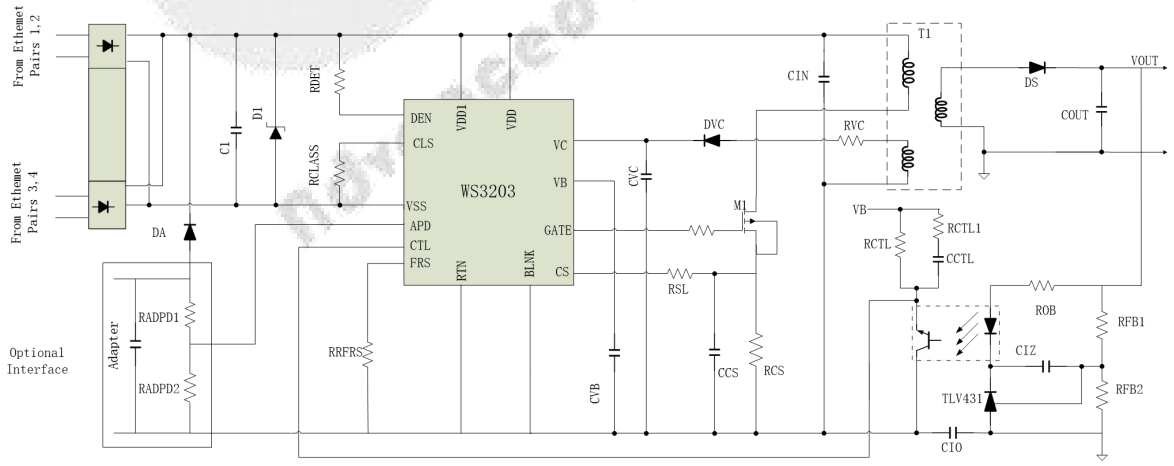


Figure 1. High Efficiency Converter Using WS3203

PRODUCT INFORMATION

DEVICE	STATUS	DUTY CYCLE	POE UVLO ON / HYST.	CONVERTER UVLO ON / HYST.	PACKAGE	MARKING
WS3203	Active	0–78%	35/4.5	9 / 3.5	TSSOP-14	WS3203

ABSOLUTE MAXIMUM RATINGS(1) (2)

Voltage with respect to V_{SS} unless otherwise noted.

	VALUE	UNIT
Input voltage range DEN, RTN , V_{DD}, V_{DD1}	–0.3 to 85	V
Input voltage range CLS(2)	-0.3 to 6.5	V
Input voltage range [APD, BLNK(2) , CTL, FRS(2) , VB(2)] to [RTN]	–0.3 to 6.5	V
Input voltage rangeCS to [RTN]	–0.3 to V_B	V
Voltage range V_C to [RTN]	–0.3 to 15	V
Voltage range GATE(2) to [RTN]	–0.3 to V_C+0.3	V
Sinking current RTN	Internal limited	mA
Sourcing current V_B	Internal limited	mA
Average Sourcing or sinking current GATE	25	mArms
ESD rating HBM	2	kV
ESD rating CDM	500	V
ESD –system level (contact/air) at RJ-45(3)	8/15	kV
Operating junction temperature range, T_J	–40 to Internal limited	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Do not apply voltage to these pins

(3) ESD per EN61000-4-2. A power supply containing the WS3203 was subjected to the highest test levels in the standard. See the ESD section.

RECOMMENDED OPERATING CONDITIONS(1)

Voltage with respect to V_{SS} (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage range RTN,, VDD, VDD1	0		57	V
Input voltage range T2P, VC to [RTN]	0	12	15	V
Input voltage range APD, CTL to [RTN]	0		VB	V
Input voltage range CS to [RTN]	0		2	V
Continuous RTN current (TJ ≤ 125°C)			350	mA
Sourcing current, VB	0	2.5	5	mA
VB capacitance	0.08			μF
RRBLNK	0		350	kΩ
Synchronization pulse width input (when used)	25			ns
Operating junction temperature range TJ	-40		125	°C

DISSIPATION RATINGS

PACKAGE	Ψ_{JT} °C/W(1)	θ_{JP} °C/W	θ_{JB} °C/W	θ_{JA} °C/W	MAXIMUM POWER RATING (W)
TSSOP-14	1.9	1.4	49.1	106.6	1.2

(1) $T_J = T_{TOP} + (\Psi_{JT} \times P_J)$

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: CS=APD=CTL=RTN, GATE float, R_{RFRS}=68 kΩ, R_{RBLNK}=249kΩ, C_{VB}=C_{VC}=0.1μF, R_{DET}=24.9 kΩ, R_{CLS} open, 0 V≤(V_{DD}, V_{DD1}) ≤57 V, 0V≤V_C≤12 V, –40°C≤T_J≤125°C. Typical specifications are at 25°C.

CONTROLLER SECTION ONLY

[V_{SS} = RTN and V_{DD}=V_{DD1}] or [V_{SS}=RTN=V_{DD}], all voltages referred to [RTN].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C						
V_{CUV}	UVLO	V_C rising	8.4	9	9.6	V
V_{CUVH}		Hysteresis(1)	3.7	4	4.3	V
Operating current		V_C=12V, CTRL=V_B, R_{RDT}=68.1kΩ	0.7	1.2	1.4	mA
t_{ST}	Bootstrap startup time, C_{VC}=22uF	V_{DD1}=13.2V, V_C(0)=0V	50	85	175	ms
		V_{DD1}=35V, V_C(0)=0V	27	45	92	
Startup current source I_{VC}		V_{DD1}=13.2V, V_C=8.6V	0.44	1.06	1.80	mA
		V_{DD1}=48V, V_C=0V	2.7	4.8	6.8	mA
V_B						
Voltage		6.5V≤V_C≤12V, 0≤I_{VB}≤5mA	4.8	5.1	5.25	V
FRS						
Switching frequency		CTRL=V_B, measure GATE, R_{RFRS}=68.1K	203	253	293	kHz
D_{MAX}	Duty cycle	CTRL=V_B, measure GATE	76	78	80	%
V_{SYNC}	Synchronization	Input threshold	2	2.2	2.4	V
CTRL						
V_{ZDC}	0% duty cycle threshold	V_{CTRL}↓until GATE stops	1.3	1.5	1.7	V
	Softstart period	Interval from switching start to V_{CSMAX}	0.4	2		ms
	Input resistance		70	100	145	kΩ
BLNK						

	Blanking delay	RBLNK=RTN	35	55	78	ns
	(in addition to t_1)	R_{RBLNK}=49.9 kΩ	38	55	70	
CS						
V_{CSMAX}	Maximum threshold voltage	V_{CTL}=VB, V_{CS} rising until GATE duty cycles drops	0.5	0.55	0.6	V
t_1	Turnoff delay	V_{CS}=0.65V	24	40	70	ns
V_{SLOPE}	Internal slope compensation voltage	Peak voltage at maximum duty cycle, referenced to CS	90	118	142	mV
I_{SL_EX}	Peak slope compensation current	V_{CTL}=V_B, I_{CS} at maximum duty cycle	30	42	54	uA
Bias current (sourcing)		DC component of I_{CS}	1	2.5	4.3	uA
GATE						
Source current		V_{CTRL}=V_B, V_C=12V, GATE high, pulsed measurement	0.37	0.6	0.95	A
Sink current		V_{CTRL}=V_B, V_C=12V, GATE low, pulsed measurement	0.7	1	1.4	A
APD						
V_{APDEN}	APD threshold voltage	V_{APD} rising	1.43	1.5	1.57	V
V_{APDH}		Hysteresis(1)	0.29	0.31	0.33	
APD leakage current (source or sink)		V_C=12V, V_{APD}=VB			1	uA
THERMAL SHUTDOWN						
Turnoff temperature		TJ rising	135	145	155	℃
Hysteresis(2)				20		℃

(1) The hysteresis tolerance tracks the rising threshold for a given device.

(2) These parameters are provided for reference only, and do not constitute part of WST's published specifications for purposes of WST's product warranty.

ELECTRICAL CHARACTERISTICS – PoE AND CONTROL

[V_{DD}=V_{DD1}] or [V_{DD1}=RTN], V_C = RTN, all voltages referred to V_{SS} unless otherwise noted。

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DETECTION（DEN）		V_{DD}=V_{DD1}=RTN=V_{SUPPLY} positive				
Detection current		Measure I_{SUPPLY}				
		V_{DD}=1.6V	62	64.3	66.5	uA
		V_{DD}=10V	399	406	414	
Detection bias current		V_{DD}=10V, float DET, measure I_{SUPPLY}		5.6	10	uA
		Note: not during Mark state				
V_{PD_DIS}	Hotswap disable threshold		3	4	5	V
DET leakage current		V_{DET}=V_{DD}=57V, float VDD1 and RTN, measure I_{DET}		0.1	5	uA
CLASSIFICATION (CLS)		(V_{DD} = V_{DD1} = RTN = V_{SUPPLY} positive)				
I_{CLASS}		13V≤VDD≤21V, measure I_{SUPPLY}				mA
		R_{CLASS}=1270Ω	1.8	2.1	2.4	
	Classification current,	R_{CLASS}=243Ω	9.9	10.4	10.9	
	applies to both cycles	R_{CLASS}=137Ω	17.6	18.5	19.4	
		R_{CLASS}=90.9Ω	26.5	27.7	29.3	
		R_{CLASS}=63.4Ω	38	39.7	42	
Classification mark resistance		5.6V≤V_{DD}≤9.4V	7.5	9.7	12	kΩ
V_{CL_ON}	Classification regulator lower	Regulator turns on, V_{DD} rising	11.2	11.9	12.6	V
V_{CL_H}	threshold	Hysteresis(1)	1.55	1.65	1.75	
V_{CU_OFF}	Classification regulator upper	Regulator turns off, V_{DD} rising	21	22	23	V
V_{CU_H}	threshold	Hysteresis(1)	0.5	0.75	1.0	
V_{MSR}	Mark state reset	V_{DD} falling	3	4	5	V
Leakage current		V_{DD}=57V, V_{CLASS}=0V, DET=V_{SS}, measure I_{CLASS}			1	uA
PASS DEVICE (RTN)		V_{DD1}=RTN				
On resistance				0.45	0.75	Ω
Current limit		V_{RTN}=1.5V, V_{DD}=48V, pulsed measurement	405	450	535	mA
Inrush limit		V_{RTN}=2V, V_{DD}:0V->48V, pulsed measurement	100	140	180	mA
Fold-back voltage threshold		V_{DD} rising	11	12.3	13.6	V
UVLO						
V_{UVLO_R}	UVLO threshold	V_{DD} rising	33.9	35	36.1	V
V_{UVLO_H}		Hysteresis(1)	4.4	4.55	4.76	
THERMAL SHUTDOWN						
Turnoff temperature		T_J rising	135	145	155	℃
Hysteresis(2)				20		℃

(1) The hysteresis tolerance tracks the rising threshold for a given device.

(2) These parameters are provided for reference only, and do not constitute part of WST's published specifications for purposes of WST's product warranty.

FUNCTIONAL BLOCK DIAGRAM

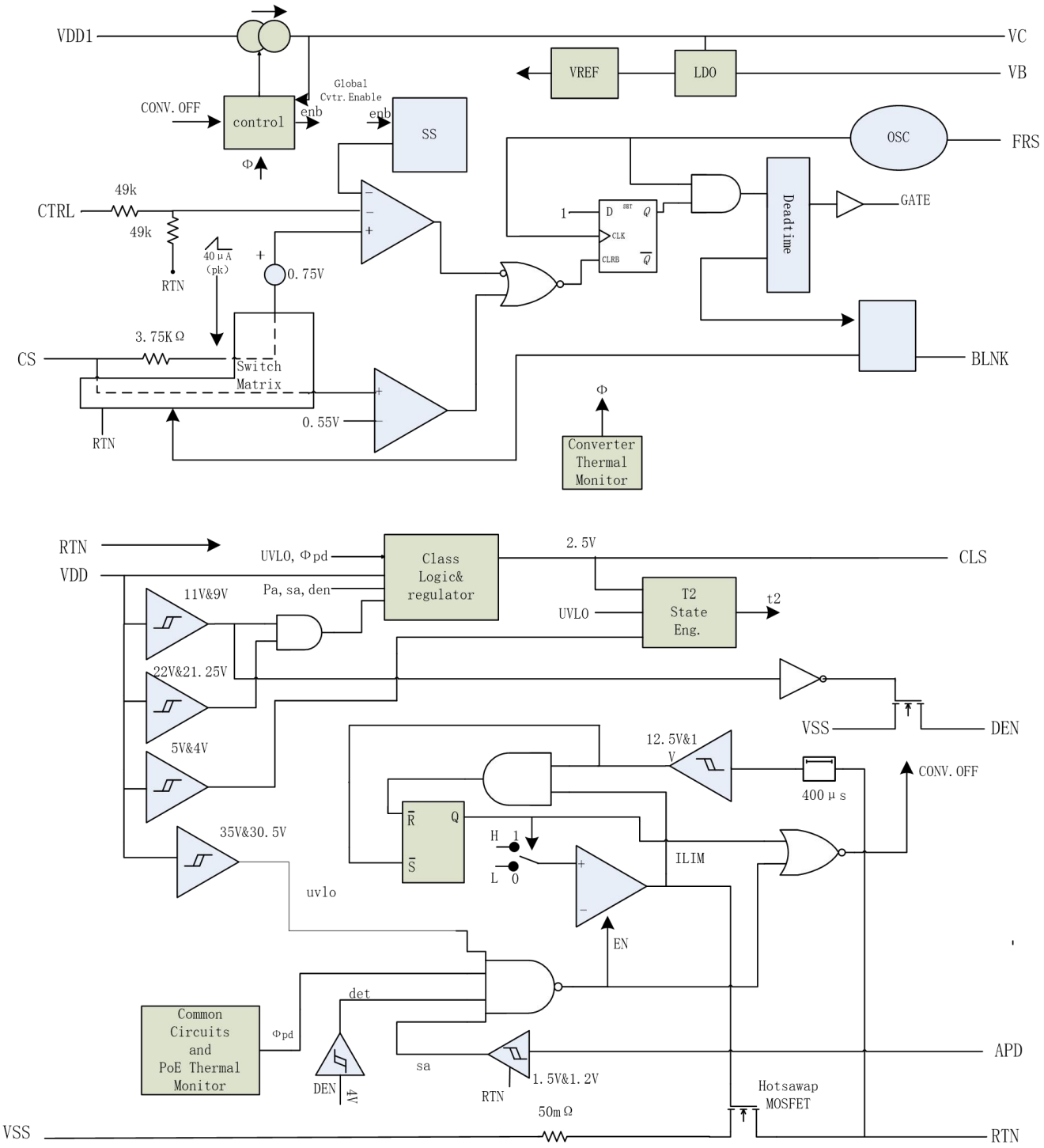
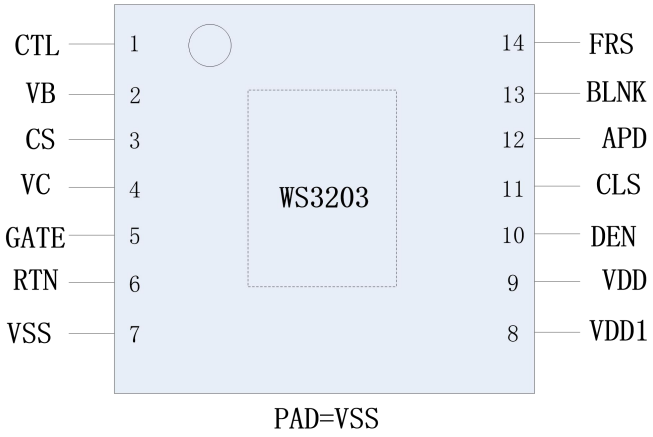


Figure 2

(TOP VIEW)



PIN FUNCTIONS

Name	Pin	Type	Description
CTL	1	I	The control loop input to the PWM (pulse width modulator), typically driven by output regulation feedback (e.g. optocoupler). Use V_B as a pullup for CTRL.
VB	2	O	5.1 V bias rail for dc/dc control circuits and the feedback optocoupler. Typically bypass with a 0.1 μF to ARTN.
CS	3	I/O	DC/DC converter switching MOSFET current sense input. See R_{CS} in Figure 1.
VC	4	I/O	DC/DC converter bias voltage. Connect a 0.47 μF (minimum) ceramic capacitor to ARTN at the pin, and a larger capacitor to power startup.
GATE	5	O	Gate drive output for the main dc/dc converter switching MOSFET
RTN	6		RTN is the output of the PoE hotswap MOSFET.
VSS	7		Connect to the negative power rail derived from the PoE source.
VDD1	8	I	Source of dc/dc converter startup current. Connect to VDD for many applications.
VDD	9	I	Connect to the positive PoE input power rail. VDD powers the PoE interface circuits. Bypass with a 0.1 μF capacitor and protect with a TVS.
DEN	10	I/O	Connect a 24.9 kΩ resistor from DET to VDD to provide the PoE detection signature. Pulling this pin to VSS during powered operation causes the internal hotswap MOSFET to turn off.
CLS	11	I	Connect a resistor from CLASS to VSS to program classification current. 2.5 V is applied to the program resistor during classification to set class current.
APD	12	I	Raising VADPD-VARTN above 1.5 V disables the internal hotswap switch, turns class off, and forces T2P active. This forces power to come from a external VDD1-RTN adapter. Tie ADPD to ARTN when not used.
BLNK	13	I	Connect to ARTN to utilize the internally set current-sense blanking period, or connect a resistor from RBLNK to ARTN to program a more accurate period.
FRS	14	I	Connect a resistor from RFRS to ARTN to program the converter switching frequency. RFRS may be used to synchronize the converter to an external timing source.

PIN DESCRIPTION

Refer to Figure 1 for component reference designators (RCS for example), and the Electrical Characteristics table for values denoted by reference (VCSMAX for example). Electrical Characteristic values take precedence over any numerical values used in the following sections.

APD

ADPD forces power to come from an external adapter connected from V_{DD1} to RTN by opening the hotswap switch, disabling the CLASS output,A resistor divider is recommended on APD when it is connected to an external adapter. The divider provides ESD protection, leakage discharge for the adapter ORing diode, and input voltage qualification. Voltage qualification assures the adapter output voltage is high enough that it can support the PD before the PoE current is cut off. Select the APD divider resistors per Equation 1 where $V_{ADPTR-ON}$ is the desired adapter voltage that enables the APD function as adapter voltage rises.

$$R_{APD1} = R_{APD2} \times (V_{ADPTR\ ON} - V_{APDEN})/V_{APDEN}$$

$$V_{ADPTR\_OFF} = \frac{R_{APD1}+R_{APD2}}{R_{APD2}} \times (V_{APDEN} - V_{APDH}) \quad (1)$$

Place the APD pull-down resistor adjacent to the ADPD pin.

APD should be tied to ARTN when not used.

BLNK

Blanking provides an interval between GATE going high and the current-control comparators on CS actively monitoring the input. This delay allows the normal turn-on current transient (spike) to subside before the comparators are active, preventing undesired short duty cycles and premature current limiting. Connect RBLNK to RTN to obtain the internally set blanking period and the programming resistor is defined by Equation 2.

$$R_{BLNK}(k\Omega) = t_{BLNK}(ns) \quad (2)$$

Place the resistor adjacent to the BLNK pin when it is used.

CLS

A resistor from CLS to V_{SS} programs the classification current per the IEEE standard. The PD power ranges and corresponding resistor values are listed in Table 1. The power assigned should correspond to the maximum average power drawn by the PD during operation. High-power PSEs may perform two classification cycles if Class 4 is presented on the first cycle. The WS3203 presents the same (resistor programmed) class each cycle per the standard.

Table 1. Class Resistor Selection

CLASS	POWER AT PD		RESISTOR (Ω)	NOTES
	MINIMUM (W)	MAXIMUM (W)		
0	0.44	12.95	1270	Minimum may be reduced by pulsed loading. Serves as a catch-all default class.
1	0.44	3.84	243	
2	3.84	6.49	137	
3	6.49	12.95	90.9	

CS

The CS (current sense) input for the dc/dc converter should be connected to the high side of the switching MOSFET's current sense resistor (R_{CS}). The current-limit threshold, V_{CSMAX}, defines the voltage on CS above which the GATE ON time will be terminated regardless of the voltage on CTL.
The WS3203 provides internal slope compensation (150 mV, V_{SLOPE}), an output current for additional slope compensation, a peak current limiter, and an off-time pull-down to this pin.
Routing between the current-sense resistor and the CS pin should be short to minimize cross-talk from noisy traces such as the gate drive signal.

CTL

CTL (control) is the voltage-control loop input to the PWM (pulse width modulator). Pulling V_{CTL} below V_{ZDC} causes GATE to stop switching. Increasing V_{CTL} above V_{ZDC} (zero duty cycle voltage) raises the switching MOSFET programmed peak current. The maximum (peak) current is requested at approximately V_{ZDC} + (2 × V_{CSMAX}). The ac gain from CTL to the PWM comparator is 0.5. The internal divider from CTL to ARTN is approximately 100 kΩ.
Use V_B as a pull up source for CTL.

DEN

DEN (detection and enable) is a multifunction pin for PoE detection and inhibiting operation from PoE power. Connect a 24.9 kΩ resistor from DEN to V_{DD} to provide the PoE detection signature. DEN goes to a high-impedance state when $V_{VDD-VSS}$ is outside of the detection range. Pulling DEN to V_{SS} during powered operation causes the internal hotswap MOSFET and class regulator to turn off, while the reduced detection resistance prevents the PD from properly re-detecting.

FRS

Connect a resistor from RFRS (frequency and synchronization) to ARTN to program the converter switching frequency. Select the resistor per the following relationship.

The converter may be synchronized to a frequency above its maximum free-running frequency by applying short ac-coupled pulses into the RFRS pin per figure 19.

The RFRS pin is high impedance. Keep the connections short and apart from potential noise sources. Special care should be taken to avoid crosstalk when synchronizing circuits are used.

$$R_{RFRS}(k\Omega) = \frac{17250}{f_{SW}(kHz)} \quad (4)$$

GATE

Gate drive output for the dc/dc converter's main switching MOSFET. GATE's phase turns the main switch on when it transitions high, and off when it transitions low. GATE is held low when the converter is disabled.

RTN

RTN is internally connected to the drain of the PoE hotswap MOSFET, while ARTN is the quiet analog reference for the dc/dc controller return.

VB

V_B is an internal 5.1V regulated dc/dc controller supply rail that is typically bypassed by a 0.1uF capacitor to RTN. V_B should be used to bias the feedback optocoupler.

VC

V_C is the bias supply for the dc/dc controller. The MOSFET gate drivers run directly from V_C. V_B is regulated down from V_C, and is the bias voltage for the rest of the converter control. A startup current source from V_{DD1} to V_C is controlled by a comparator with hysteresis to implement the converter bootstrap startup. V_C must be connected to a bias source,

such as a converter auxiliary output, during normal operation. A minimum 0.47uF capacitor, located adjacent to the V_C pin, should be connected from V_C to RTN to bypass the gate driver. A larger total capacitance is required for startup to provide control power between the time the converter starts switching and the availability of the converter auxiliary output voltage.

VDD

V_{DD} is the positive input power rail that is derived from the PoE source (PSE). V_{DD} should be bypassed to V_{SS} with a 0.1 uF capacitor as required by the IEEE standard. A transient suppressor diode (TVS), a special type of Zener diode, such as SMAJ54A should be connected from V_{DD} to V_{SS} to protect against over-voltage transients.

VDD1

V_{DD1} is the dc/dc converter startup supply. Connect to V_{DD} for many applications. V_{DD1} may be isolated by a diode from V_{DD} to support PoE priority operation.

VSS

V_{SS} is the PoE input-power return side. It is the reference for the PoE interface circuits, and has a current-limited hotswap switch that connects it to RTN. V_{SS} is clamped to a diode drop above RTN by the hotswap switch.
A local V_{SS} reference plane should be used to connect the input bypass capacitor, TVS, R_{CLASS}, and the Thermal Pad. This plane becomes the main heatsink for the WS3203.

TYPICAL CHARACTERISTICS

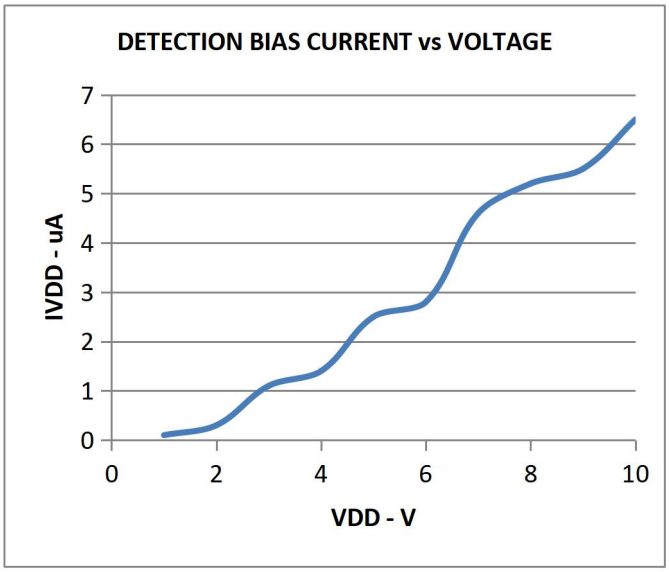


Figure 3.

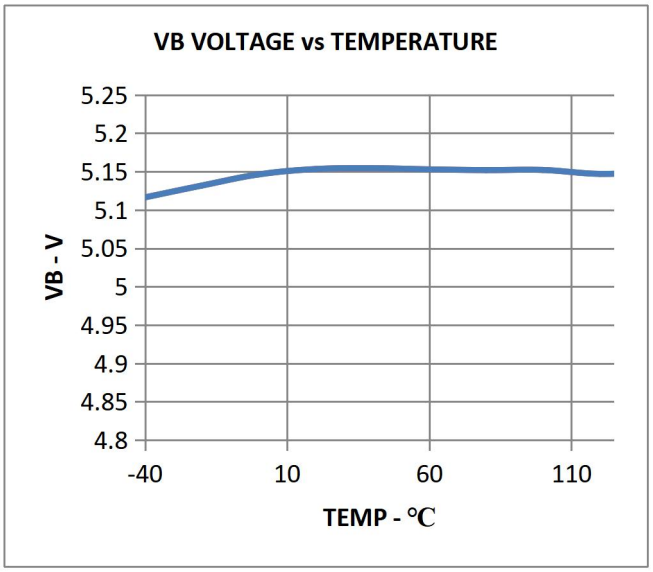


Figure 4.

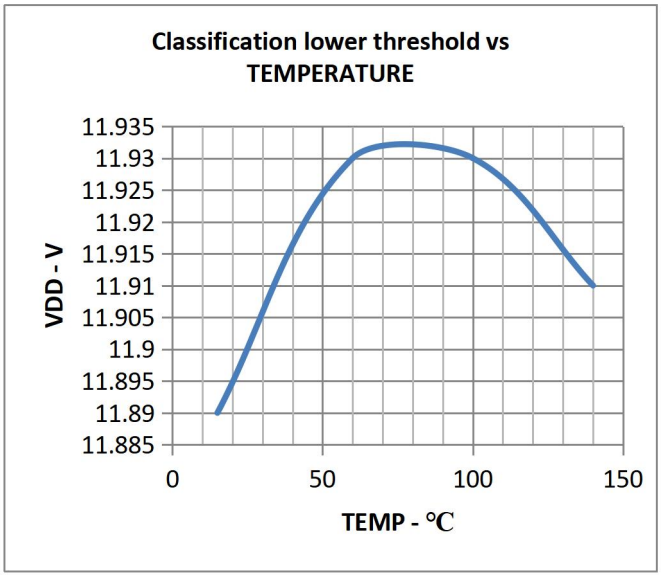


Figure 5.

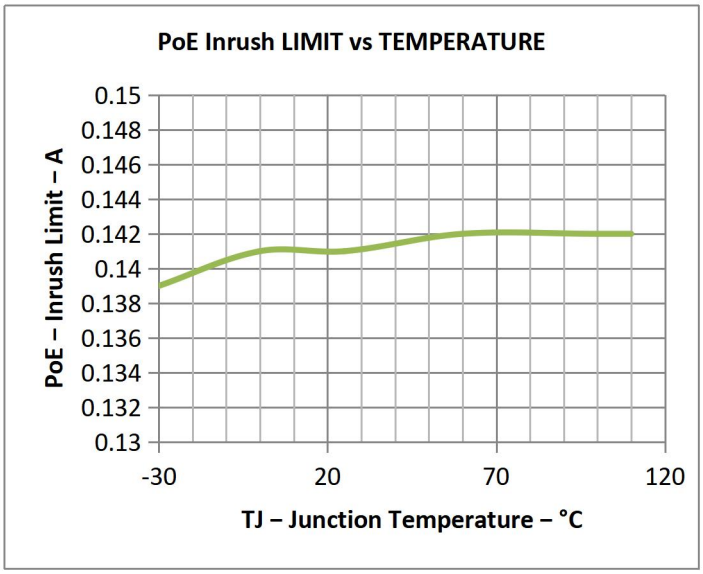


Figure 6.

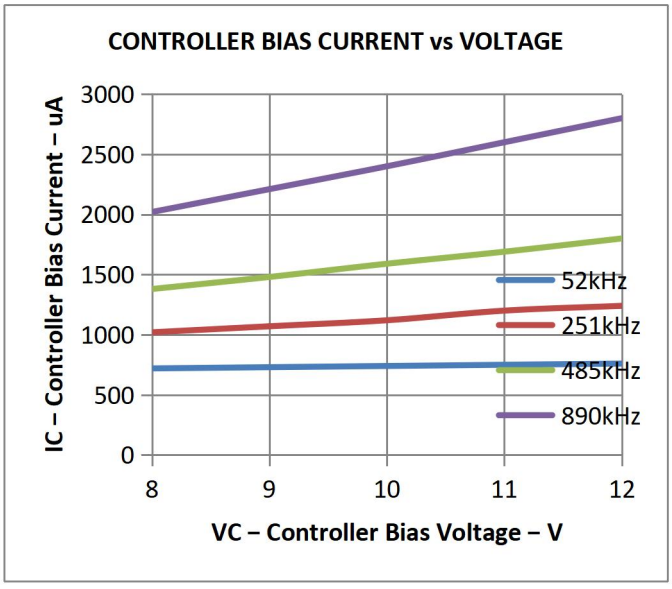


Figure 7.

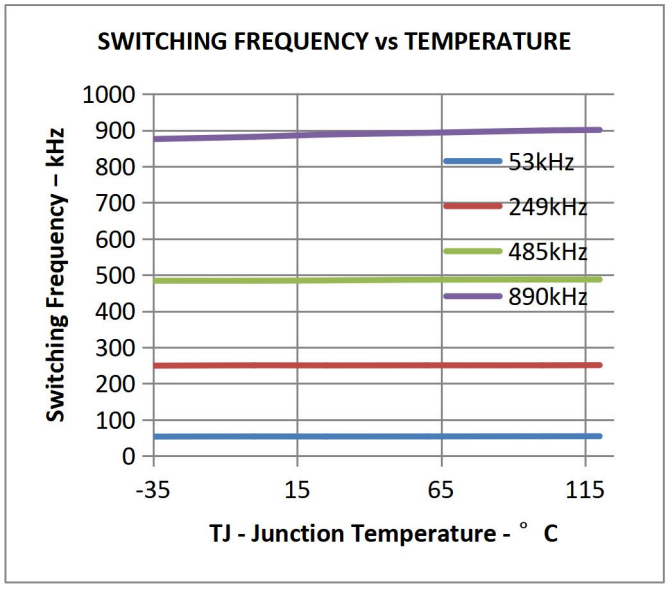


Figure 8

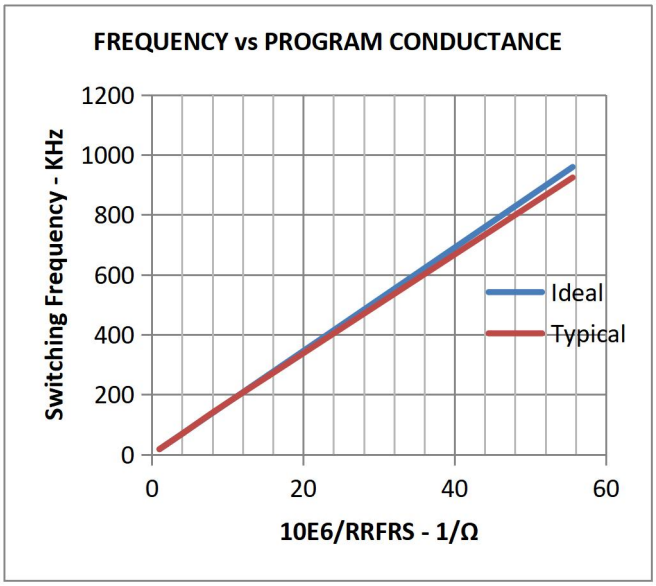


Figure 9.

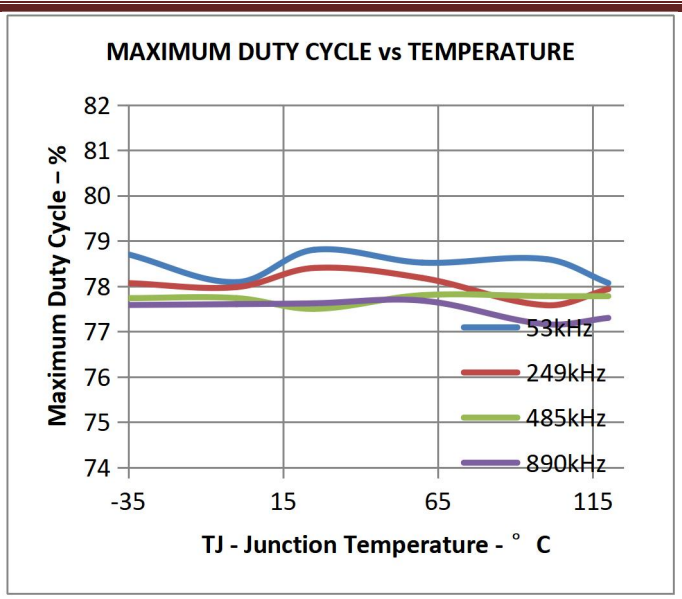


Figure 10.

PoE OVERVIEW

The following text is intended as an aid in understanding the operation of the WS3203 but not as a substitute for the IEEE 802.3at standard. The IEEE 802.3at standard is an update to IEEE 802.3-2008 clause 33 (PoE), adding high-power options and enhanced classification. Generally speaking, a device compliant to IEEE 802.3-2008 is referred to as a type 1 device, and devices with high power and enhanced classification will be referred to as type 2 devices. Standards change and should always be referenced when making designdecisions.

The IEEE 802.3at standard defines a method of safely powering a PD (powered device) over a cable by power sourcing equipment (PSE), and then removing power if a PD is disconnected. The process proceeds through an idle state and three operational states of detection, classification, and operation. The PSE leaves the cable unpowered (idle state) while it periodically looks to see if something has been plugged in; this is referred to as detection. The low power levels used during detection are unlikely to damage devices not designed for PoE. If a valid PD signature is present, the PSE my inquire how much power the PD requires; this is referred to as classification. The PSE may then power the PD if it has adequate capacity.

Type 2 PSEs are required to do type 1 hardware classification plus a (new) data-layer classification, or an enhanced type 2 hardware classification. Type 1 PSEs are not required to do hardware or data link layer (DLL) classification. A type 2 PD must do type 2 hardware classification as well as DLL classification. The PD may return the default, 13W current-encoded class, or one of four other choices. DLL classification occurs after power-on and the ethernet data link has been established.

Once started, the PD must present the maintain power signature (MPS) to assure the PSE that it is still present.The PSE monitors its output for a valid MPS, and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the idle state. Figure 11 shows the operational states as a function of PD input voltage. The upper half is for IEEE 802.3-2008, and the lower half shows specific differences for IEEE 802.3at. The dashed lines in the lower half indicate these are the same (e.g., Detect and Class) for both.

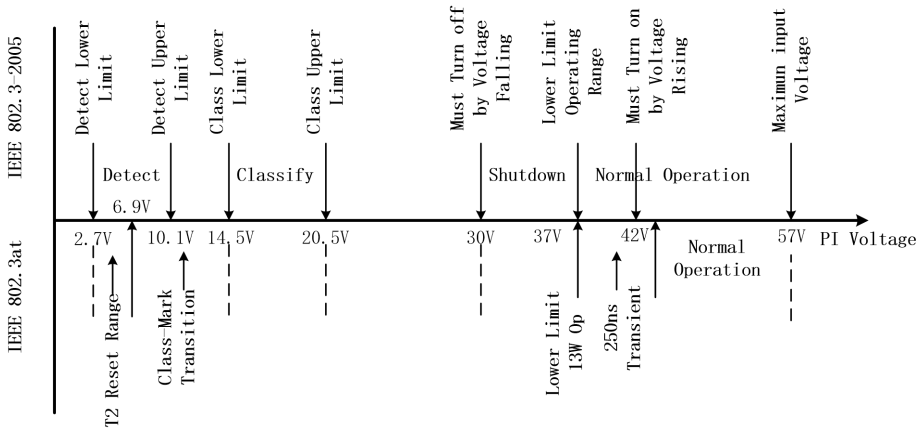


Figure 11. Operational States for PD

The PD input, typically an RJ-45 eight-lead connector, is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops and operating margin. The standard allots the maximum loss to the cable regardless of the actual installation to simplify implementation. IEEE 802.3-2008 was designed to run over infrastructure including ISO/IEC 11801 class C (CAT3 per TIA/EIA-568) that may have had AWG 26 conductors. IEEE 802.3at type 2 cabling power loss allotments and voltage drops have been adjusted for 12.5 Ω power loops per ISO/IEC11801 class D (CAT5 or higher per TIA/EIA-568, typically AWG #24 conductors). Table 2 shows key operational limits broken out for the two revisions of the standard.

Table 2. Comparison of Operational Limits

STANDARD	POWER LOOP RESISTANCE (max)	PSE OUTPUT POWER (min)	PSE STATIC OUTPUT VOLTAGE (min)	PD INPUT POWER (max)	STATIC PD INPUT VOLTAGE	
					POWER ≤ 12.95 W	POWER > 12.95 W
IEEE 802.3-2008 802.3af (Type 1)	20 Ω	15.4 W	44 V	12.95 W	37 V–57 V	N/A
802.3at (Type 2)	12.5 Ω	36 W	50 V	25.5 W	37 V–57 V	42.5 V–57 V

The PSE can apply voltage either between the RX and TX pairs (pins 1 - 2 and 3 - 6 for 10baseT or 100baseT), or between the two spare pairs (4 - 5 and 7 - 8). Power application to the same pin combinations in 1000baseT systems is recognized in IEEE 802.3at. 1000baseT systems can handle data on all pairs, eliminating the spare pair terminology. The PSE may only apply voltage to one set of pairs at a time. The PD uses input diode bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the standard limits at the POE and the WS3203 specifications.

The PSE is permitted to disconnect a PD if it draws more than its maximum class power over a one second interval. A Type 1 PSE compliant to IEEE 802.3at is required to limit current to between 400 mA and 450 Ma during powered operation, and it must disconnect the PD if it draws this current for more than 75 ms. Class 0 and 3 PDs may draw up to 400-mA peak currents for up to 50 ms. The PSE may set lower output current limits based on the declared power requirements of the PD.

Threshold Voltages

The WS3203 has a number of internal comparators with hysteresis for stable switching between the various states. Figure 12 relates the parameters in the Electrical Characteristics section to the PoE states. The mode labeled idle between classification and operation implies that the DEN, CLS, and RTN pins are all high impedance. The state labeled Mark, which is drawn in dashed lines, is part of the new type 2 hardware class state machine.

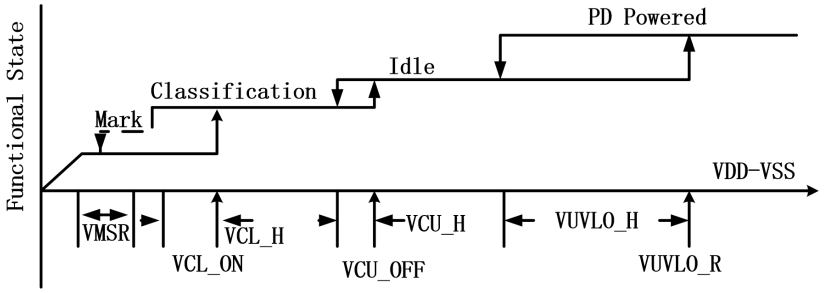


Figure 12. Threshold Voltages

PoE Startup Sequence

The waveforms of Figure 13 demonstrate detection, classification, and startup from a PSE with type 2 hardware classification. The key waveforms shown are V_{VDD}-V_{VSS}, V_{RTN}-V_{VSS}, and I_{PI}. IEEE 802.3at requires a minimum of two detection levels, two class and mark cycles, and startup from the second mark event. V_{RTN} to V_{SS} falls as the WS3203 charges C_{IN} following application of full voltage. Subsequently, the converter starts up, drawingcurrent as seen in the I_{PI} waveform.

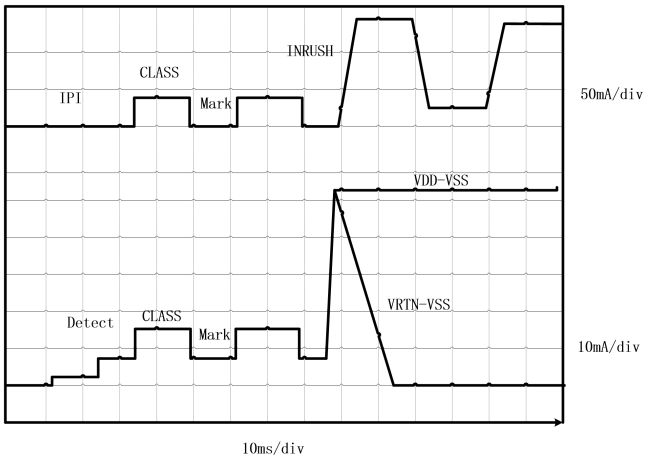


Figure 13. Startup

Detection

The WS3203 drives DET to V_{SS} whenever V_{VDD}-V_{VSS} is below the lower classification threshold. When the input voltage rises above V_{CL-ON}, the DET pin goes to an open-drain condition to conserve power. While in detection, RTN is high impedance, and almost all the internal circuits are disabled. An R_{DET} of 24.9 kΩ (1%), presents the correct signature. It may be a small, low-power resistor since it only sees a stress of about 5 mW. A valid PD detection signature is an incremental resistance (ΔV / ΔI) between 23.75 kΩ and 26.25 kΩ at the PI.

The detection resistance seen by the PSE at the PI is the result of the input bridge resistance in series with the parallel combination of R_{DET} and internal V_{DD} loading. The input diode bridge's incremental resistance may be hundreds of ohms at the very low currents drawn when 2.7 V is applied to the PI. The input bridge resistance is partially cancelled by the WS3203's effective resistance during detection.

The type 2 hardware classification protocol of IEEE 802.3at specifies that a type 2 PSE drops its output voltage into the

detection range during the classification sequence. The PD is required to have an incorrect detection signature in this condition, which is referred to as the mark event (see Figure 13). After the first mark event, the WS3203 will present a signature less than 12 kΩ until it has experienced a V_{VDD}-V_{VSS} voltage below the mark reset (V_{MSR}). This is explained more fully under Hardware Classification.

Hardware Classification

Hardware classification allows a PSE to determine a PD's power requirements before powering, and helps with power management once power is applied. Type 2 hardware classification permits high power PSEs and PDs to determine whether the connected device can support high-power operation. A type 2 PD presents class 4 in hardware to indicate it is a high-power device. A type 1 PSE will treat a class 4 device like a class 0 device, allotting 13 W if it chooses to power the PD. A PD that receives a 2 event class understands that it is powered from a high-power PSE and it may draw up to 25.5 W immediately after the 80 ms startup period completes. A type 2 PD that does not receive a 2-event hardware classification may choose to not start, or must start in a 13 W condition and request more power through the DLL after startup. The standard requires a type 2 PD to indicate that it is underpowered if this occurs. Startup of a high-power PD under 13 W implicitly requires some form of powering down sections of the application circuits.

The maximum power entries in Table 1 determine the class the PD must advertise. The PSE may disconnect a PD if it draws more than its stated Class power, which may be the hardware class or a lower DLL-derived power level. The standard permits the PD to draw limited current peaks that increase the instantaneous power above the Table 1 limit, however the average power requirement always applies.

The WS3203 implements two-event classification. Selecting an R_{CLASS} of 63.4 Ω provides a valid type 2 signature. WS3203 may be used as a compatible type 1 device simply by programming class 0–3 per Table 1. DLL communication is implemented by the ethernet communication system in the PD and is not implemented by the WS3203.

The WS3203 disables classification above V_{CU_OFF} to avoid excessive power dissipation. CLASS voltage is turned off during PD thermal limit or when ADPD or DET are active. The CLASS output is inherently current limited, but should not be shorted to V_{SS} for long periods of time.

Maintain Power Signature (MPS)

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. A valid MPS consists of a minimum DC current of 10 mA (at a duty cycle of at least 75 ms on every 225 ms) and an AC impedance lower than 26.25 kΩ in parallel with 0.05 µF. The AC impedance is usually accomplished by the minimum CIN requirement of 5 µF. When APD or DEN are used to force the hotswap switch off, the DC MPS is not met. A PSE that monitors the DC MPS will remove power from the PD when this occurs. A PSE that monitors only the AC MPS may remove power from the PD.

Startup and Converter Operation

The internal PoE UVLO (Under Voltage Lock Out) circuit holds the hotswap switch off before the PSE provides full voltage to the PD. This prevents the converter circuits from loading the PoE input during detection and classification. The converter circuits will discharge C_{IN}, C_{VC}, and C_{VB} while the PD is unpowered. Thus V_{VDD}-V_{RTN} will be a small voltage just after full voltage is applied to the PD, as seen in Figure 13. The PSE drives the PI voltage to the operating range once it has decided to power up the PD. When V_{VDD} rises above the UVLO turn-on threshold (V_{UVLO-R}, ~35 V) with RTN high, the WS3203 enables the hotswap MOSFET with a ~140 Ma (inrush) current limit as seen in Figure 14. Converter switching is disabled while C_{IN} charges and V_{RTN} falls from V_{VDD} to nearly V_{VSS}, however the converter startup circuit is allowed to charge C_{VC} (the bootstrap startup capacitor). Converter switching is allowed if the PD is not in inrush, OTSD is not active, and the V_C UVLO permits it. Once the inrush current falls about 10% below the inrush current limit, the PD current limit switches to the operational level (~450 mA). Continuing the startup sequence shown in Figure 14, V_{VC} continues to rise until the startup threshold (V_{CUV}, ~11 V) is exceeded, turning the startup source off and enabling switching. The V_B regulator is always active, powering the internal converter circuits as V_{VC} rises. There is a slight delay between the removal of charge current and the start of switching as the softstart ramp sweeps above the V_{ZDC} threshold. V_{VC} falls as it powers both the internal circuits and the switching MOSFET gates. If the converter control

bias output rises to support V_{VC} before it falls to $V_{CUV} – V_{CUVH}$ (~7 V), a successful startup occurs.

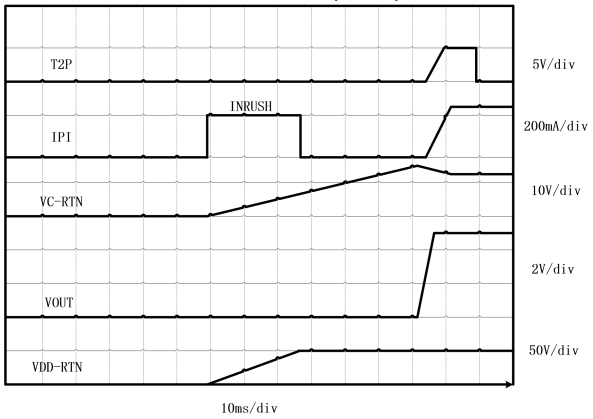


Figure 14. Power Up and Start

If V_{VDD}- V_{VSS} drops below the lower PoE UVLO (V_{UVLO-R} - V_{UVLO-H}, ~30.5 V), the hotswap MOSFET is turned off, but the converter will still run. The converter will stop if V_{VC} falls below the converter UVLO ($V_{CUV} – V_{CUVH}$, ~7 V), the hotswap is in inrush current limit, 0% duty cycle is demanded by V_{CTRL} (V_{CTRL} < V_{ZDC}, ~1.5 V), or the converter is in thermal shutdown.

PD Hotswap Operation

The internal hotswap MOSFET is protected against output faults and input voltage steps with a current limit and deglitched (time-delay filtered) foldback. An overload on the pass MOSFET engages the current limit, with V_{RTN}-V_{VSS} rising as a result. If V_{RTN} rises above ~12 V for longer than ~400us, the current limit reverts to the inrush value, and turns the converter off. The 400us deglitch feature prevents momentary transients from causing a PD reset, provided that recovery lies within the bounds of the hotswap and PSE protection. Figure 15 shows an example of recovery from a 16 V PSE rising voltage step. The hotswap MOSFET goes into current limit, overshooting to a relatively low current, recovers to ~450 mA full current limit, and charges the input capacitor while the converter continues to run. The MOSFET did not go into foldback because V_{RTN}-V_{VSS} was below 12 V after the 400us deglitch.

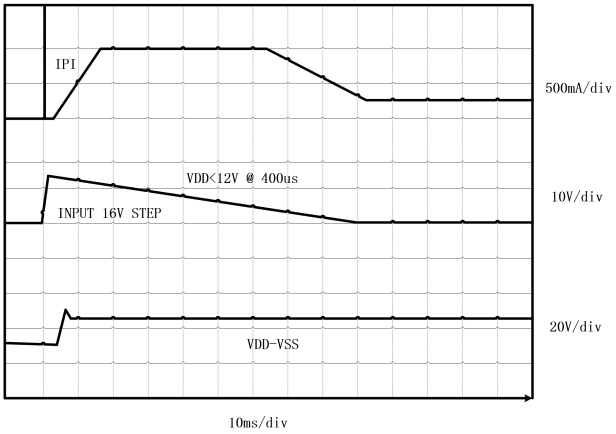


Figure 15. Response to PSE Step Voltage

The PD control has a thermal sensor that protects the internal hotswap MOSFET. Conditions like startup or operation into a V_{DD} to RTN short cause high power dissipation in the MOSFET. An over-temperature shutdown (OTSD) turns off the hotswap MOSFET and class regulator, which are restarted after the device cools. The hotswap MOSFET will be re-enabled with the inrush current limit when exiting from an over-temperature event.

Pulling DET to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off. This feature allows a PD with Option three ORing per Figure 16 to achieve adapter priority. Care must be taken with synchronous converter topologies that can deliver power in both directions

The hotswap switch will be forced off under the following conditions:
1. V_{ADPD} above V_{ADPDEN} (~1.5 V)
2. V_{DET} < V_{PD-DIS} when V_{VDD}– V_{VSS} is in the operational range
3. PD over-temperature
4. (V_{VDD}– V_{VSS}) < PoE UVLO (~30.5 V).

Converter Controller Features

The WS3203 dc/dc controller implements a typical current-mode control as shown in the Functional Block Diagram. Features include oscillator, over-current and PWM comparators, current-sense blanker, dead-time control, softstart, and gate driver. In addition, an internal slope-compensation ramp generator, frequency synchronization logic, thermal shutdown, and startup current source with control are provided.

The WS3203 is optimized for isolated converters, and does not provide an internal error amplifier. Instead, the optocoupler feedback is directly fed to the CTRL pin which serves as a current-demand control for the PWM. There is an offset of V_{ZDC} (~1.5 V) and 2:1 resistor divider between the CTRL pin and the PWM. A V_{CTRL} below V_{ZDC} will stop converter switching, while voltages above (V_{ZDC} + (2 × V_{CSMAX})) will not increase the requested peak current in the switching MOSFET. Optocoupler biasing design is eased by this limited control range.

The internal startup current source and control logic implement a bootstrap-type startup as discussed in “Startup and Converter Operation.” The startup current source charges C_{VC} from V_{DD1} when the converter is disabled (either by the PD control or the V_C control) to store enough energy to start the converter. Steady-state operating power must come from a converter (bias winding) output or other source. Loading on V_C and V_B must be minimal while C_{VC} charges, otherwise the converter may never start. The optocoupler will not load V_B when the converter is off for most situations, however care should be taken in ORing topologies where the output is powered when PoE is off.

The converter will shut off when V_C falls below its lower UVLO. This can happen when power is removed from the PD, or during a fault on a converter output rail. When one output is shorted, all the output voltages fall including the one that powers V_C. The control circuit discharges V_C until it hits the lower UVLO and turns off. A restart will initiate as described in *Startup and Converter Operation* if the converter turns off and there is sufficient V_{DD1} voltage. This type of operation is sometimes referred to as *hiccup mode* which provides robust output short protection by providing time-average heating reduction of the output rectifier.

The bootstrap control logic disables most of the converter controller circuits except the V_B regulator and internal reference. GATE will be low when the converter is disabled. RFRS, RBLNK, and RDT will be at ARTN while the V_C UVLO disables the converter. While the converter runs, RFRS, RBLNK, and RDT will be about 1.25 V.

The startup current source transitions to a resistance as (V_{VDD1} – V_{VC}) falls below 7 V, but will start the converter from adapters within t_{ST}. The lower test voltage for t_{ST} was chosen based on an assumed adapter tolerance, but is not meant to imply a hard cutoff exists. Startup takes longer and eventually will not occur as V_{DD1} decreases below the test voltage. The bootstrap source provides reliable startup from widely varying input voltages, and eliminates the continual power loss of external resistors. The startup current source will not charge above the maximum recommended V_{VC} if the converter is disabled and there is sufficient V_{DD1} to charge higher.

Current Slope Compensation and Current Limit

Current-mode control requires addition of a compensation ramp to the sensed inductive (transformer or inductor) current for stability at duty cycles near and over 50%. The WS3203 has a maximum duty cycle limit of 78%, permitting the design of wide input-range flyback and active clamp converters with a lower voltage stress on the output rectifiers. While the maximum duty cycle is 78%, converters may be designed that run at duty cycles well below this for a

narrower, 36 V to 57 V PI range. The WS3203 provides a fixed internal compensation ramp that suffices for most applications.

The WS3203 provides internal, frequency independent, slope compensation (150 mV, V_{SLOPE}) to the PWM comparator input for current-mode control-loop stability. This voltage is not applied to the current-limit comparator whose threshold is 0.55 V (V_{CSMAX}). If the provided slope is not sufficient, the effective slope may be increased by addition of R_S per Figure 20. The additional slope voltage is provided by ($I_{SL-EX} \times R_S$). There is also a small dc offset caused by the ~2.5 μA pin current. The peak current limit does not have duty cycle dependency unless R_S is used. This makes it easier to design the current limit to a fixed value. See *Current Slope Compensation* for more information.

The internal comparators monitoring CS are isolated from the IC pin by the blanking circuits while GATE is low, and for a short time (blanking period) just after GATE switches high. A 440 Ω (max) equivalent pull down on CS is applied while GATE is low.

Blanking - R_{RBLNK}

The WS3203 provides a choice between internal fixed and programmable blanking periods. The blanking period is specified as an increase in the minimum GATE on time over the inherent gate driver and comparator delays. The default period (see the Electrical Characteristics table) is selected by connecting RBLNK to RTN, and the programmable period is set with R_{RBLNK}.

The WS3203 blanker timing is precise enough that the traditional R-C filters on CS can be eliminated. This avoids current-sense waveform distortion, which tends to get worse at light output loads. There may be some situations or designers that prefer an R-C approach. The WS3203 provides a pull-down on CS during the GATE off time to improve sensing when an R-C filter must be used. The CS input signal should be protected from nearby noisy signals like GATE drive and the switching MOSFET drain.

RFRS and Synchronization

The RFRS pin programs the (free-running) oscillator frequency, and may also be used to synchronize the WS3203 converter to a higher frequency. The internal oscillator sets the maximum duty cycle at 78% and controls the slope-compensation ramp circuit. Synchronization may be accomplished by applying a short pulse (T_{SYNC}) of magnitude V_{SYNC} to RFRS as shown in Figure 19. The synchronization pulse terminates the potential on-time period, and the off-time period does not begin until the pulse terminates.

Thermal Shutdown

The dc/dc controller has an OTSD that can be triggered by heat sources including the V_B regulator, GATE driver, bootstrap current source, and bias currents. The controller OTSD turns off V_B, the GATE driver, and forces the V_C control into an under-voltage state.

Adapter ORing

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used if PoE is not available in a particular installation. While most applications only require that the PD operate when both sources are present, the WS3203 supports forced operation from either of the power sources. Figure 16 illustrates three options for diode ORing external power into a PD. Only one option would be used in any particular design. Option 1 applies power to the WS3203 PoE input, option 2 applies power between the WS3203 PoE section and the power circuit, and option 3 applies power to the output side of the converter. Each of these options has advantages and disadvantages.

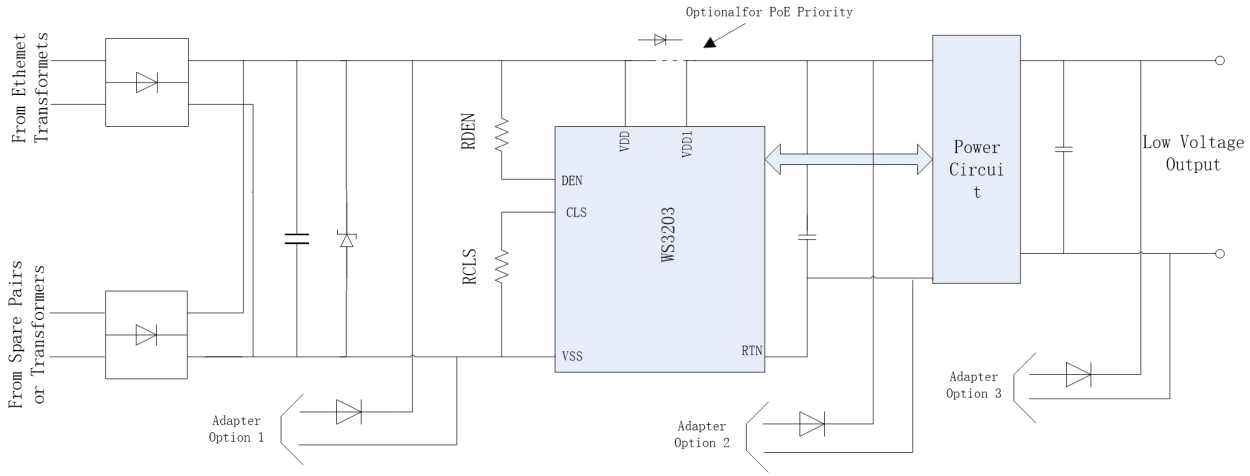


Figure 16. ORing Configurations

The IEEE standards require that the Ethernet cable be isolated from ground and all other system potentials. The adapter must meet a minimum 1500 Vac dielectric withstand test between the output and all other connections for ORing options 1 and 2. The adapter only needs this isolation for option 3 if it is not provided by the converter.

Adapter ORing diodes are shown for all the options to protect against a reverse voltage adapter, a short on the adapter input pins, and damage to a low-voltage adapter. ORing is sometimes accomplished with a MOSFET in option 3.

Using DEN to Disable PoE

The DEN pin may be used to turn the PoE hotswap switch OFF by pulling it to V_{SS} while in the operational state, or to prevent detection when in the idle state. A low on DET forces the hotswap MOSFET OFF during normal operation.

ORing Challenges

Preference of one power source presents a number of challenges. Combinations of adapter output voltage (nominal and tolerance), power insertion point, and which source is preferred determine solution complexity. Several factors adding to the complexity are the natural high-voltage selection of diode ORing (the simplest method of combining sources), the current limit implicit in the PSE, and PD inrush and protection circuits (necessary for operation and reliability). Creating simple and seamless solutions is difficult if not impossible for many of the combinations. However the WS3203 offers several built-in features that simplify some combinations.

Several examples will demonstrate the limitations inherent in ORing solutions. Diode ORing a 48 V adapter with PoE (option 1) presents the problem that either source might be higher. A blocking switch would be required to assure which source was active. A second example is combining a 12 V adapter with PoE using option 2. The converter will draw approximately four times the current at 12 V from the adapter than it does from PoE at 48 V. Transition from adapter power to PoE may demand more current than can be supplied by the PSE. The converter must be turned off while C_{IN} capacitance charges, with a subsequent converter restart at the higher voltage and lower input current. A third example is use of a 12 V adapter with ORing option 1. The PD hotswap would have to handle four times the current, and have 1/16 the resistance (be 16 times larger) to dissipate equal power. A fourth example is that MPS is lost when running from the adapter, causing the PSE to remove power from the PD. If ac power is then lost, the PD will stop operating until the PSE detects and powers the PD.

APPLICATION INFORMATION

The WS3203 will support many power supply topologies that require a single PWM gate drive and will operate with current-mode control. Figure 17 provides an example of an active clamp forward converter that uses the second gate driver to control M2, the active element in the clamp.Selecting a converter topology along with a design procedure is

beyond the scope of this applications section. Examples to help in programming the WS3203 are shown below. Additional special topics are included to explain the ORing capabilities, frequency dithering, and other design considerations.

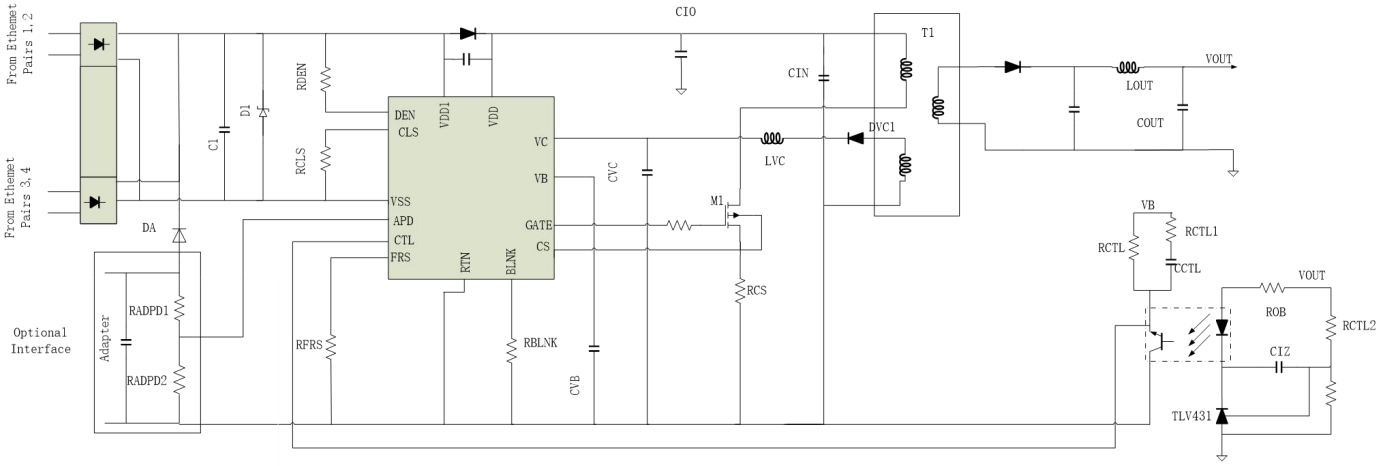


Figure 17. Driven Synchronous Flyback

Input Bridges and Schottky Diodes

Using Schottky diodes instead of PN junction diodes for the PoE input bridges and D_{VDD} will reduce the loss of this function by about 30%. There are however some things to consider when using them.

The IEEE standard specifies a maximum backfeed voltage of 2.8 V. A 100 kΩ resistor is placed between the unpowered pairs and the voltage is measured across the resistor. Schottky diodes often have a higher reverse leakage current than PN diodes, making this a harder requirement to meet. Use conservative design for diode operating temperature, select lower-leakage devices where possible, and match leakage and temperatures by using packaged bridges to help with this.

Schottky diode leakage current and lower dynamic resistance can impact the detection signature. Setting reasonable expectations for the temperature range over which the detection signature is accurate is the simplest solution. Increasing R_{DET} slightly may also help meet the requirement.

Schottky diodes have proven less robust to the stresses of ESD transients, failing as a short or becoming leaky. Care must be taken to provide adequate protection in line with the exposure levels. This protection may be as simple as ferrite beads and capacitors.

A general recommendation for the input rectifiers are 1 A or 2 A, 100 V rated discrete or bridge diodes.

Protection, D1

A TVS, D1, across the rectified PoE voltage per Figure 18 must be used. An SMAJ54A, or a part with equal to or better performance, is recommended for general indoor applications. If an adapter is connected from VDD1 to RTN, as in ORing option 2 above, voltage transients caused by the input cable inductance ringing with the internal PD capacitance can occur. Adequate capacitive filtering or a TVS must limit this voltage to be within the absolute maximum ratings. Outdoor transient levels or special applications require additional protection.

Use of diode D_{VDD} for PoE priority may dictate the use of additional protection around the WS3203. ESDevents between the PD power inputs, or the inputs and converter output, cause large stresses in the hotswap MOSFET if D_{VDD} becomes reverse biased and transient current around the WS3203 is blocked. The use of C_{VDD} and D_{RTN} in Figure 18 provides additional protection should over-stress of the WS3203 be an issue. An SMAJ54A would be a good initial selection for D_{RTN}. Individual designs may have to tune the value of C_{VDD}.

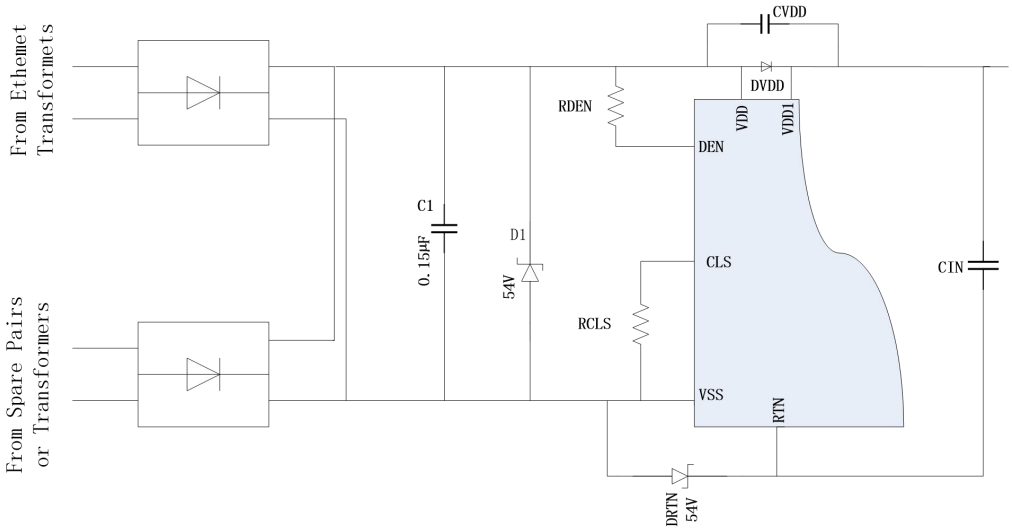


Figure 18. Example of Added ESD Protection for PoE Priority

Capacitor, C_1

The IEEE 802.3at standard specifies an input bypass capacitor (from V_{DD} to V_{SS}) of 0.05 μF to 0.12 μF. Typicallya 0.1 μF, 100 V, 10% ceramic capacitor is used.

Detection Resistor, RDEN

The IEEE 802.3at standard specifies a detection signature resistance, R_{DEN} between 23.75 kΩ and 26.25 kΩ, or 25 kΩ ± 5%. Choose an R_{DET} of 24.9 kΩ.

Classification Resistor, RCLASS

Connect a resistor from CLASS to V_{SS} to program the classification current according to the IEEE 802.3at standard. The class power assigned should correspond to the maximum average power drawn by the PD during operation. Select R_{CLASS} according to Table 1.

APD Pin Divider Network, RAPD1, RAPD2

he APD pin can be used to disable the WS3203 internal hotswap MOSFET giving the adapter source priority over the PoE source.

Setting Frequency (RRFRS) and Synchronization

The converter switching frequency is set by connecting R_{RFRS} from the RFRS pin to ARTN. The frequency may beset as high as 1 MHz with some loss in programming accuracy as well as converter efficiency. Synchronization at high duty cycles may become more difficult above 500 kHz due to the internal oscillator delays reducing the available on-time. As an example:

1. Assume a desired switching frequency (f_{SW}) of 250 kHz.
2. Compute R_{RFRS}:

   (a) $R_{RFRS}(k\Omega) = \frac{17250}{f_{SW}\ (kHz)} = \frac{17250}{250} = 69$

   (b) Select 69.8 kΩ.

The WS3203 may be synchronized to an external clock to eliminate beat frequencies from a sampled system, or to place emission spectrum away from an RF input frequency. Synchronization may be accomplished by applying a short pulse (T_{SYNC}) of magnitude V_{SYNC} to RFRS as shown in Figure 19. R_{RFRS} should be chosen so that the maximum free-running frequency is just below the desired synchronization frequency. The synchronization pulse terminates the potential on-time period, and the off-time period does not begin until the pulse terminates. The pulse at the RFRS pin should reach between 2.5 V and V_B, with a minimum width of 22 ns (above 2.5 V) and rise/fall times less than 10 ns. The RFRS node should be protected from noise because it is high-impedance. An R_T on the order of 100 Ω in the isolated example reduces noise sensitivity and jitter.

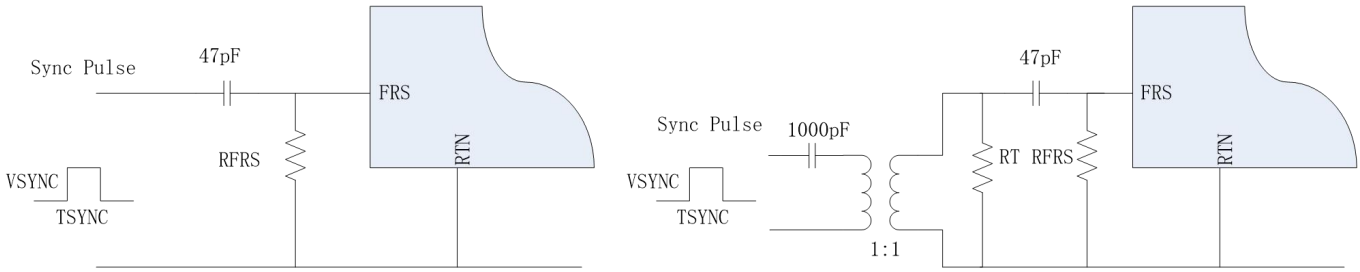


Figure 19. Synchronization

Current Slope Compensation

The WS3203 provides a fixed internal compensation ramp that suffices for most applications. R_S (see Figure 20) may be used if the internally provided slope compensation is not enough.

Most current-mode control papers and application notes define the slope values in terms of V_{PP}/T_S (peak ramp voltage / switching period), however the electrical characteristics table specifies the slope peak (V_{SLOPE}) based on the maximum (78%) duty cycle. Assuming that the desired slope, $V_{SLOPE-D}$ (in mV/period), is based on the full period, compute R_S per the following equation where V_{SLOPE}, D_{MAX}, and I_{SL-EX} are from the electrical characteristics table with voltages in mV, current in μA, and the duty cycle is unitless (e.g., D_{MAX} = 0.78).

$$R_S(\Omega) = \frac{\left[V_{SLOPE\_D}(mV) - \left(\frac{V_{SLOPE}(mV)}{D_{MAX}}\right)\right]}{I_{SL\_EX}(\mu A)} \times 1000 \qquad (6)$$

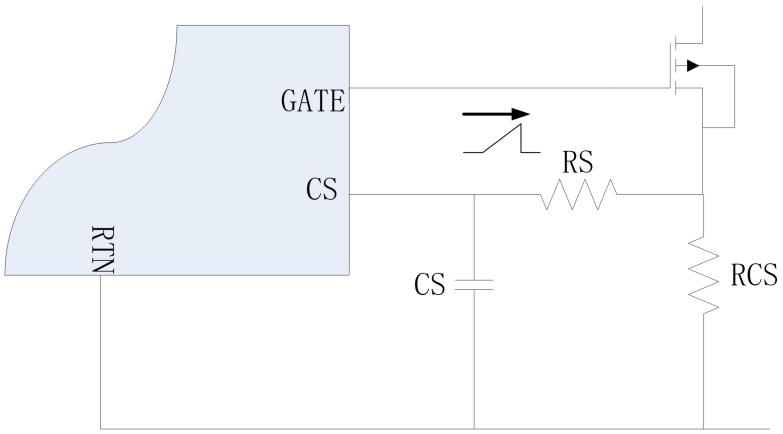


Figure 20. Additional Slope Compensation

CS may be required if the presence of RS causes increased noise, due to adjacent signals like the gate drive, to appear at the CS pin.

Blanking Period, RRBLNK

Selection of the blanking period is often empirical because it is affected by parasitics and thermal effects of every device between the gate-driver and output capacitors. The minimum blanking period prevents the current limit and PWM comparators from being falsely triggered by the inherent current spike that occurs when the switching MOSFET turns on. The maximum blanking period is bounded by the output rectifier's ability to withstand the currents experienced during a converter output short.

If blanking beyond the internal default is desired choose R_{RBLNK} using $R_{RBLNK}(k\Omega) = t_{RBLNK}$ (ns).

1. For a 100 ns blanking interval
   (a) R_{RBLNK} (kΩ) = 100
   (b) Choose R_{RBLNK} = 100 kΩ.

The blanking interval can also be chosen as a percentage of the switching period.

1. Compute RRBLNK as follows for 2% blanking interval in a switcher running at 250 kHz.

   (a) $R_{RBLNK}(k\Omega) = \frac{Blanking\_interval}{f_{SW}\ (kHz)} \times 10^4 = \frac{2}{250} \times 10^4 = 80$

   (b) Select R_{RBLNK} = 80.6 kΩ.

Estimating Bias Supply Requirements and CVC

The bias supply (VC) power requirements determine the CVC sizing and frequency of hiccup during a fault. The first step is to determine the power/current requirements of the power supply control, then use this to select CVC. The control current draw will be assumed constant with voltage to simplify the estimate, resulting in an approximate value.

First determine the switching MOSFET gate drive power.

1. Let V_{QG} be the gate voltage swing that the MOSFET Q_G is rated to (often 10 V).

   (a) $P_{GATE} = V_C \times f_{SW} \times \left(Q_{GATE} \times \frac{V_C}{V_{QG}}\right)$ $P_{GATE2} = V_C \times f_{SW} \times \left(Q_{GATE2} \times \frac{V_C}{V_{QG}}\right)$

   (b) Compute gate drive power if VC is 12 V, Q_{GATE} is 17 nC, and Q_{GATE2} is 8 nC.

   $$P_{GATE} = 12V \times 250kHz \times 17nC \times \frac{12}{10} = 61.2mW$$

$$P_{GATE2} = 12V \times 250kHz \times 8nC \times \frac{12}{10} = 28.8mW$$

(c) $P_{DRIVE} = 61.2mW + 28.8mW = 90mW$

(d) This illustrates why MOSFET Q_G should be an important consideration in selecting the switching MOSFETs.

2. Estimate the required bias current at some intermediate voltage during the C_{VC} discharge. For the WS3203, 12 V provides a reasonable estimate. Add the operating bias current to the gate drive current.

(a) $I_{DRIVE} = \frac{P_{DRIVE}}{V_C} = \frac{90mW}{12V} = 7.5mA$

(b) $I_{TOTAL} = I_{DRIVE} + I_{OPERATING} = 7.5mA + 0.92mA = 8.42mA$

3. Compute the required C_{VC} based on startup within the typical softstart period of 4 ms.

(a) $C_{VC1} + C_{VC2} = \frac{T_{STARUP} \times I_{TOTAL}}{V_{CUVH}} = \frac{4ms \times 8.42mA}{6.5V} = 5.18\mu F$

(b) For this case, a standard 10 µF electrolytic plus a 0.47 µF should be sufficient.

4. Compute the initial time to start the converter when operating from PoE.

(a) Using a typical bootstrap current of 4 mA, compute the time to startup.

(b) $T_{ST} = \frac{C_{VC1} \times V_{CUH}}{I_{VC}} = \frac{10.47\mu F \times 15V}{4mA} = 39ms$

5. Compute the fault duty cycle and hiccup frequency

(a) $T_{RECHARGE} = \frac{(C_{VC1} + C_{VC2}) \times V_{CUVH}}{I_{VC}} = \frac{(10\mu F + 0.47\mu F) \times 6.5V}{4mA} = 17ms$

(b) $T_{DISCHARGE} = \frac{(C_{VC1} + C_{VC2}) \times V_{CUVH}}{I_{TOTAL}} = \frac{(10\mu F + 0.47\mu F) \times 6.5V}{8.42mA} = 8.08ms$

(c) Note that the optocoupler current is 0 mA because the output is in current limit. Also, it is assumed I_{T2P} is 0 mA.

Duty Cycle: $D = \frac{T_{DISCHARGE}}{T_{DISCHARGE} + T_{RECHARGE}} = \frac{8.08ms}{8.08ms + 17ms} = 32\%$

(d) Hiccup Frequency: $F = \frac{1}{T_{DISCHARGE} + T_{RECHARGE}} = \frac{1}{8.08ms + 17ms} = 39.9Hz$

6. With the WS3203, the voltage rating of C_{VC1} and C_{VC2} should be 25 V minimum

7. **Switching Transformer Considerations and R_{VC}**

8. Care in design of the transformer and V_C bias circuit is required to obtain hiccup overload protection. Leading-edge voltage overshoot on the bias winding may cause V_C to peak-charge, preventing the expected tracking with output voltage. Some method of controlling this is usually required. This may be as simple as a series resistor, or an R-C filter in front of D_{VC1}. Good transformer bias-to-output-winding coupling results in reduced overshoot and better voltage tracking.

9. R_{VC} as shown in Figure 21 helps to reduce peak charging from the bias winding. This becomes especially important when tuning hiccup mode operation during output overload. Typical values for R_{VC} will be between 10Ω and 100Ω.

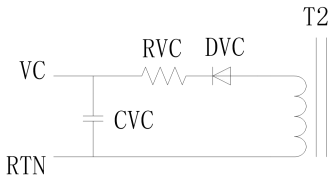


Figure 21. RVC Usage

Advanced ORing Techniques

The material in sections *Adapter ORing* and *Protection, D1* are important to consider as well. The following applications are unique to the WS3203 with the introduction of PSPD.

Option 2 ORing with PoE acting as a hot backup is eased by connecting PSPD to V_{DD} per Figure 22. This PSPD connection enables the class regulator even when ADPD is high. The R-Zener network (1.8 kΩ – 24 V) is the simplest circuit that will satisfy MPS requirements, keeping the PSE online. This network may be switched out when the ADPD is not powered with an optocoupler. This works best with a 48-V adapter and the ADPD-programmed threshold as high as possible. An example of an adapter priority application with smooth switchover between a 48 V adapter and PoE is shown on the right side of Figure 22. D_{ADPD} is used to reduce the effective ADPD hysteresis, allowing the PSE to power the load before V_{VDD1}-V_{RTN} falls too low and causes a hotswap foldback.

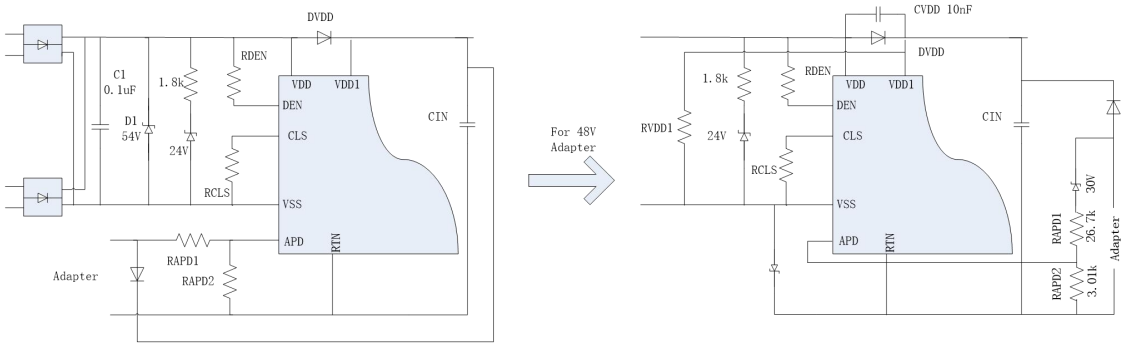


Figure 22. Option 2 PoE Backup ORing

Softstart

Converters require a softstart on the voltage error amplifier to prevent output overshoot on startup. Figure 23 shows a common implementation of a secondary-side softstart that works with the typical TL431 error amplifier. The softstart components consist of D_{SS}, R_{SS}, and C_{SS}. They serve to control the output rate-of-rise by pulling V_{CTRL} down as C_{SS} charges through R_{OB}, the optocoupler, and D_{SS}. This has the added advantage that the TL431 output and C_{IZ} are preset to the proper value as the output voltage reaches the regulated value, preventing voltage overshoot due to the error amplifier recovery. The secondary-side error amplifier will not become active until there is sufficient voltage on the secondary. The WS3203 provides a primary-side softstart which persists long enough (~4 ms) for secondary side voltage-loop softstart to take over. The primary-side current-loop softstart controls the switching MOSFET peak current by applying a slowly rising ramp voltage to a second PWM control input. The PWM is controlled by the lower of the softstart ramp or the CTRL-derived current demand. The actual output voltage rise time is usually much shorter than the internal softstart period. Initially the internal softstart ramp limits the maximum current demand as a function of time. Either the current limit, secondary-side softstart, or output regulation assume control of the PWM before the internal softstart period is over.

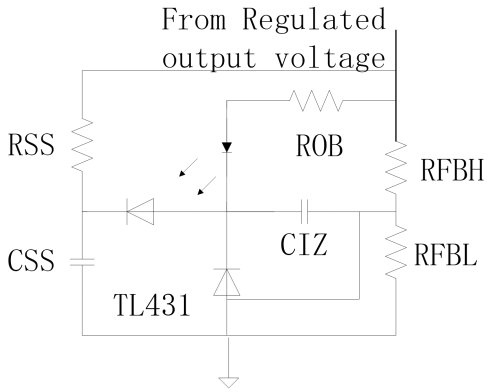


Figure 23. Error Amplifier Soft Start

Special Switching MOSFET Considerations

Special care must be used in selecting the converter switching MOSFET. The WS3203 minimum switching MOSFET V_{GATE} is ~5.5 V, which is due to the V_C lower threshold. This will occur during an output overload, or towards the end of a (failed) bootstrap startup. The MOSFET must be able to carry the anticipated peak fault current at this gate voltage

Thermal Considerations and OTSD

Sources of nearby local PCB heating should be considered during the thermal design. Typical calculations assume that the WS3203 is the only heat source contributing to the PCB temperature rise. It is possible for a normally operating WS3203 device to experience an OTSD event if it is excessively heated by a nearby device.

Frequency Dithering for Conducted Emissions Control

The international standard CISPR 22 (and adopted versions) is often used as a requirement for conducted emissions. Ethernet cables are covered as a telecommunication port under section 5.2 for conducted emissions. Meeting EMI requirements is often a challenge, with the lower limits of Class B being especially hard. Circuit board layout, filtering, and snubbing various nodes in the power circuit are the first layer of control techniques. A more detailed discussion of EMI control is presented in *Practical Guidelines to Designing an EMI Compliant PoE Powered Device With Isolated Flyback*. Additionally, IEEE802.3at sections 33.3 and 33.4 have requirements for noise injected onto the Ethernet cable based on compatibility with data transmission.

Occasionally, a technique referred to as frequency dithering is utilized to provide additional EMI measurement reduction. The switching frequency is modulated to spread the narrowband individual harmonics across a wider bandwidth, thus lowering peak measurements. The circuit of Figure 24 modulates the switching frequency by feeding a small ac signal into the RFRS pin. These values may be adapted to suit individual needs.

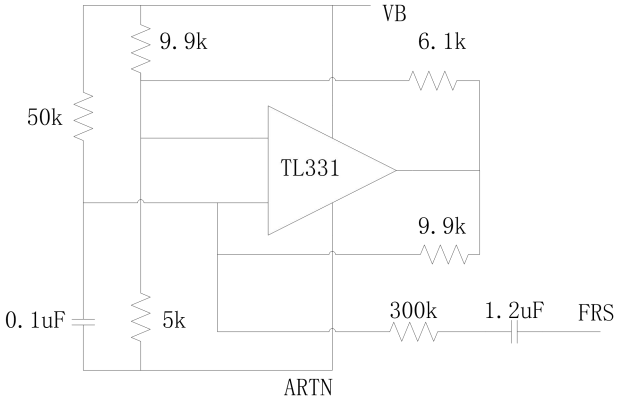


Figure 24. Frequency Dithering

ESD

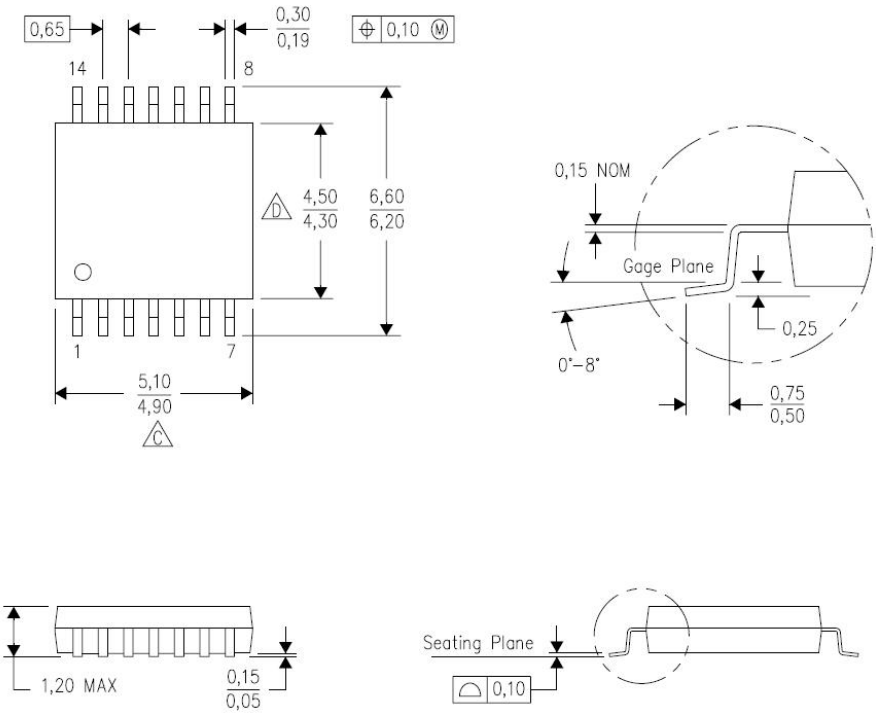
The WS3203 has been tested to EN61000-4-2 using a power supply based on Figure 1. The levels used were 8 kV contact discharge and 15 kV air discharge. Surges were applied between the PoE input and the dc output, between the adapter input and the dc output, between the adapter and the PoE inputs, and to the dc output with respect to earth. Tests were done both powered and unpowered. No WS3203 failures were observed and operation was continuous. See Figure 18 for additional protection for some test configurations.

Layout

Printed circuit board layout recommendations are provided in the evaluation module (EVM) documentation available for these devices.

PACKAGE MATERIALS INFORMATION

DEVICE PACKAGE TYPE: TSSOP-14



NOTES：

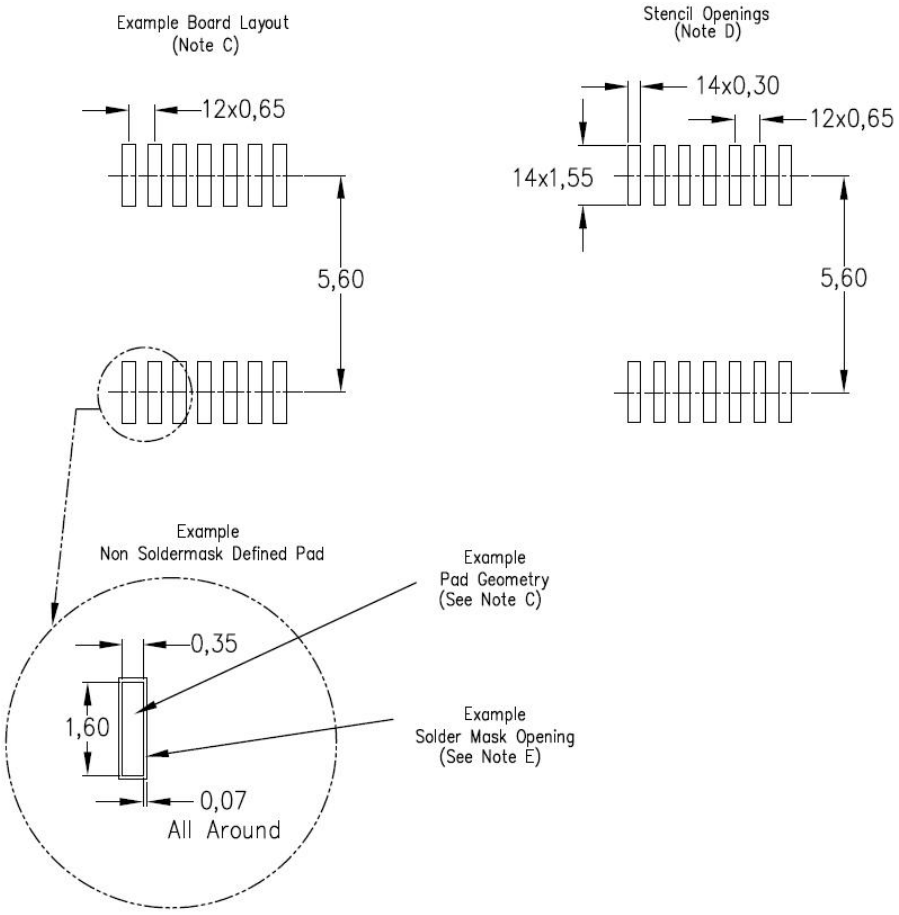
A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusions .Mold flash and protrusion shall not exceed 0.15 per side.

D. This package is designed to be soldered to a thermal pad on the boad.

LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Customer should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

D. This package is designed to be soldered to a thermal pad on the boad.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.

F. Customers should contact their board fabrication site for solder tolerances between and signal pads.

Order information

PART NUMBER	TEMP RANGE	Material	PKG TYPE	MOQ/T&R	MOQ/carton
WS3203	-40℃ ~125℃	Green	TSSOP14	1 reel=4,000/box	8 box=32,000/carton

Revision history

Data	Revision	Description
June 2021	1.1	Product release
August 2021	1.2	Change the company LOGO；