MSKSEMI SEMICONDUCTOR 美森科

ESD TVS TSS MOV GDT PLED

SN74AHC1G86DBVR-MS/SN74AHC1G86DCKR-MS

Product specification

General Description

This single 2-input exclusive-OR gate is designed for 1.65V to 5.5V Vcc operation.
The SN74AHC1G86DBVR-MS/SN74AHC1G86DCKR-MS performs the Boolean function $Y=A\oplus B$ or $Y=\overline{A}B+A\overline{B}$ in positive logic. A common application is as a true/complement element.If the input is low,the other input is reproduced in true fom at the output.If the input is highthe signal on the other input is reproduced inverted at the output.
This device is fully specified for partial-power-down applications using Iof.The Ioff circuitry disables the outputs,preventing damaging current backflow through the device when it is powered down.

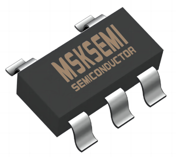
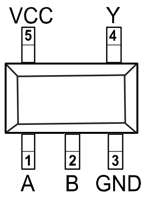
Features

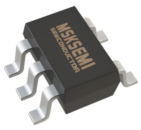
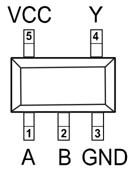
- Operate from 1.65 Vto 5.5V
- Specified from -40℃ to 125℃
- Inputs accept voltages to 5.5V
- Maxtpa of 3.7ns at 3.3V
- Low powerconsumption,10μA max Icc
- ±24-mA output drive at 3.3V
- IoffsSupports partial-power-down mode

Applications

- Wireless headsets
- Motor drives andcontrols
- TVs
- Set-top boxes
- Audio

Pinning and Marking

SOT-23-5	Pin Configurations	Marking
		

SC70-5	Pin Configurations	Marking
		

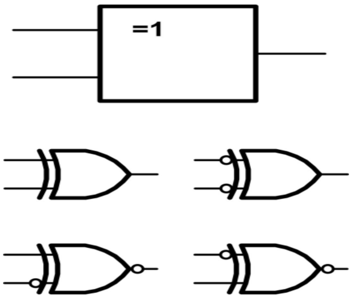
Pin Functions

Pin		Type	Description
Name	SOT23-5/SC70-5		
A	1	I	Input A
B	2	I	Input B
Y	4	O	Output Y
VCC	5	-	Positive Supply
GND	3	-	Ground

Order information

Orderable Device	Package	Packing Option
SN74AHC1G86DBVR-MS	SOT23-5	3000PCS
SN74AHC1G86DCKR-MS	SC70-5	3000PCS

Circuit Diagram



Absolute Maximum Ratings

Parameters			Min	Max.	Unit
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range		-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state		-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
Continuous current through V_{CC} or GND				±100	mA
T_J	Junction temperature under bias			150	℃
T_{stg}	Storage temperature range		-65	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

ESD Ratings

ESD			Value	Unit
V(ESD)	Electrostatic discharge	Human-body model (HBM)	8 K	V
		Charged-device model (CDM)	1.25 K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameters		Min.	Max.	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
V_{IH}	High-Level Input Voltage	V_{CC}=1.65V to1.95V	0.65×V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2		
		V_{CC}=4.5V to 5.5V	0.7×V_{CC}		
V_{IL}	Low-Level Input Voltage	V_{CC}=1.65V to1.95V		0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3×V_{CC}	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-Level Output Current	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
I_{OL}	Low-Level Output Current	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Δt/Δv	Input Transition Rise or Fall Rate	V_{CC}=1.8V±0.15V,2.5V±0.2V		20	ns/V
		V_{CC}=3.3V±0.3V		10	
		V_{CC}=5V±0.5V		5	
T_A	Operating Free-air Temperature	All Other Packages	40	125	℃

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Electrical Characteristics

FULL=–40°C to +125°C, Typical values are at TA=+25°C. (unless otherwise noted)

Parameters	Symbol	Conditions	V_{CC}	T_A	Min.	Typ.	Max.	Unit
Output								
High-Level Output Voltage	V_{OH}	I_{OH}=–100μA	1.65V to 5.5V	FULL	V_{CC}-0.1			V
		I_{OH}=–4mA	1.65		1.2			
		I_{OH}=–8mA	2.3		1.9			
		I_{OH}=–16mA	3		2.4			
		I_{OH}=–24mA			2.3			
		I_{OH}=–32mA	4.5		3.8			
Low-Level Output Voltage	V_{OL}	I_{OL}=100μA	1.65V to 5.5V	FULL			0.1	V
		I_{OL}=4mA	1.65				0.45	
		I_{OL}=8mA	2.3				0.3	
		I_{OL}=16mA	3				0.4	
		I_{OL}=24mA					0.55	
		I_{OL}=32mA	4.5				0.55	
Off-State Current	I_{off}	V_I or V_O=5.5V	0V	FULL			±10	μA
Input								
Input Leakage Current	I_I	A or B input, V_I=5.5V or GND	0V to 5.5V	FULL			±5	μA
Input Capacitance	C_i	V_I=V_{CC} or GND	3.3V	FULL		6		pF
Power Supply								
Power Supply Range	V_{CC}		1.65V to 5.5V	FULL	1.65		5.5	V
Supply Current	I_{CC}	V_I=5.5 V or GND, I_O=0	1.65V to 5.5V	FULL			10	μA
Delta Power Current	ΔI_{CC}	One Input at V_{CC} – 0.6 V, Other Inputs at V_{CC} or GND	3V to 5.5V	FULL			500	μA

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Switching Characteristics

Over recommended operating free-air temperature range,C_L=30pF or 50 pF (unless otherwise noted)

Parameter	From(Input)	To(Output)	–40°C to +125°C						Units
			V_{CC}=1.8V±0.15V		V_{CC}=2.5V±0.2V		V_{CC}=3.3V±0.3V		
			Min	Max	Min	Max	Min	Max	
t_{pd}	A or B	Y	2.1	10	1	4.9	0.6	3.7	ns

Operating Characteristics

TA=–40°C to +125°C

Parameter		Test Conditions	V_{CC}=1.8V	V_{CC}=2.5V	V_{CC}=3.3V	Units
			Typ	Typ	Typ	
C_{pd}	Power Dissipation Capacitance	f=10Mhz	20	20	20	pF

Typical Characteristics

Typical values are at TA=+25°C (unless otherwise noted)

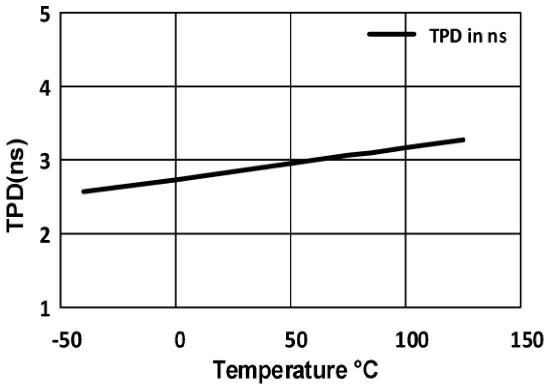


Fig.8-1. TPD Across Temperature at 3.6V V_{CC}

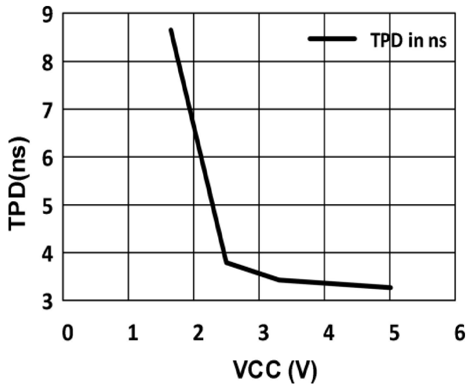
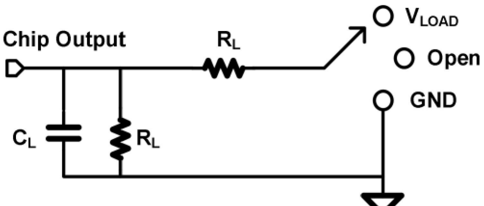


Fig.8-2. TPD Across V_{CC} at 25℃

Parameter Measurement Information

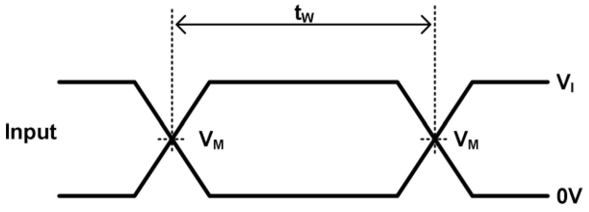


Load Circuits

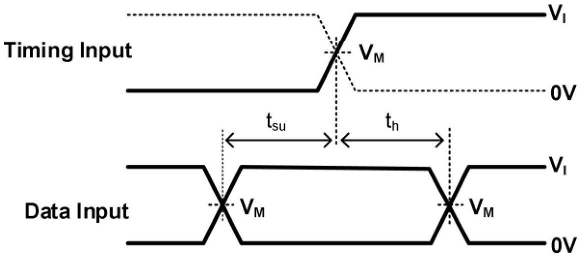
TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2×V_{CC}	15pF	1MΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2×V_{CC}	15pF	1MΩ	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	15pF	1MΩ	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	2×V_{CC}	15pF	1NΩ	0.3V

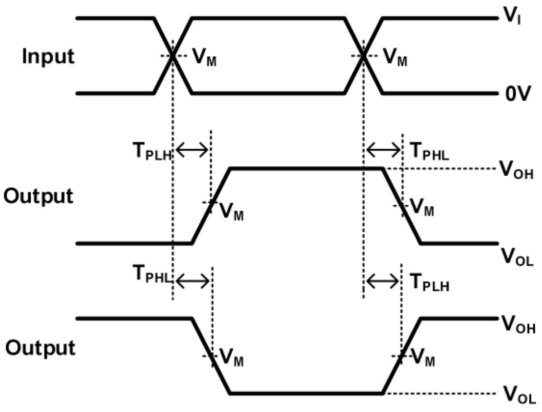
Parameter Measurement Information(Continued)



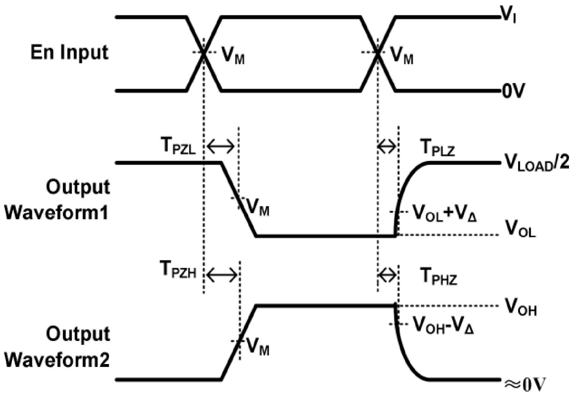
Period Time



Setup and Hold Times



Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

Notes:A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z =50.

D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all device.

Feature Description

The SN74AHC1G86DBVR-MS/SN74AHC1G86DCKR-MS device performs the Boolean function $Y = \bar{A}B + A\bar{B}$ in positive logic. This single 2-input exclusive-OR gate is designed for 1.65V to 5.5V V_{CC} operation.

A common application is as a true and complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

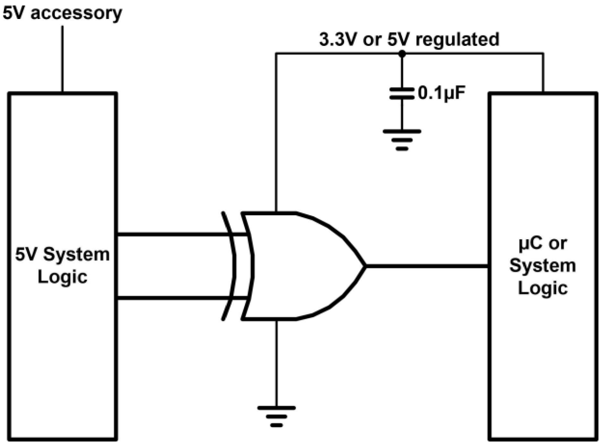
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Functional Modes

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Application Information

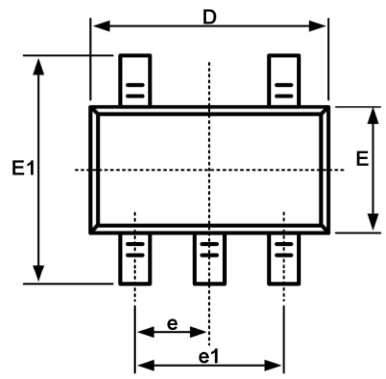
The SN74AHC1G86DBVR-MS/SN74AHC1G86DCKR-MS device can accept input voltages up to 5.5 V at any valid Vcc which makes the device suitable for down translation. This feature of the SN74LVC1G86DBVR-MS/SN74LVC1G86DCKR-MS makes it ideal for various bus interface applications.

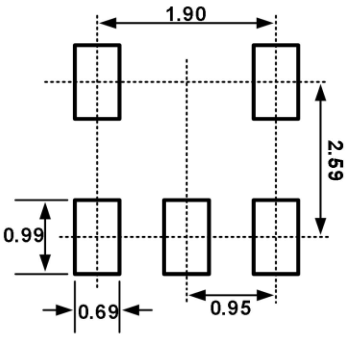


This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

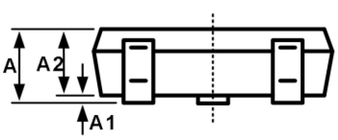
Package Outline

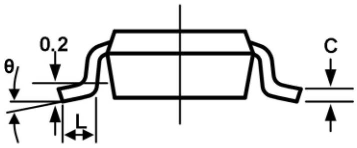
SOT23-5





Recommended Land Pattern (Unit: mm)

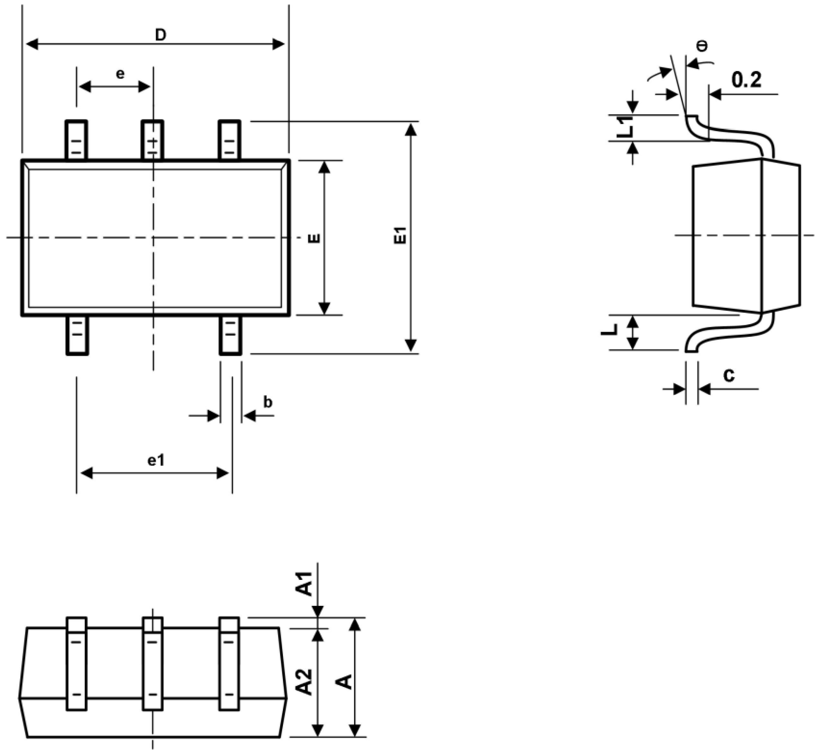




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950BSC		0.037BSC	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF		0.024REF	
θ	0°	8°	0°	8°

Package Outline

SC70-5



symbol	Dimension In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

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