FORESEE®

Industrial DDR3L Datasheet

F60C1A0004-M7

DDR3L x16 4Gb

Device Features

- **Density: 4G bits**
- **Organization**
  256Meg x 16 bits
- **Package**
  96-ball FBGA
  Lead-free (RoHS compliant) and Halogen-free
- **Power supply**
  VDD/VDDQ =1.35V (1.283 to 1.45V)
  Backward compatible DDR3 (1.5V) operation
- **Data Rate:**
  1600Mbps/1866Mbps
- **2KB page size (x16)**
  Row address: A0 to A14
  Column address: A0 to A9
- **Eight internal banks for concurrent operation**
- **Burst lengths (BL): 8 and 4 with Burst Chop (BC)**
- **Burst type (BT)**
  Sequential (8, 4 with BC)
  Interleave (8, 4 with BC)
- **CAS Latency (CL): 5, 6, 7, 8, 9, 10, 11, 12, 13, 14**
- **CAS Write Latency (CWL): 5, 6, 7, 8, 9, 10**
- **Auto precharge option for each burst access**
- **Driver strength: RZQ/7, RZQ/6 (RZQ = 240Ω)**
- **Refresh: auto-refresh, self-refresh**
- **Average refresh period**
  7.8us at TC ≤ +85°C
  3.9us at +85°C ≤TC ≤ +95°C
- **Operating temperature range**
  T_C = 0°C to +85°C (Commercial)
  T_C = -40°C to +95°C (Industrial)
- **The high-speed data transfer is realized by the 8bits prefetch pipelined architecture**
- **Double data-rate architecture: two data transfers per clock cycle**
- **Bi-directional differential data strobe (DQS and DQS#) is transmitted/received with data for capturing data at the receiver**
- **DQS is edge-aligned with data for READs; center aligned with data for WRITEs**
- **Differential clock inputs (CK and CK#)**
- **DLL aligns DQ and DQS transitions with CK transitions**
- **Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS**
- **Data mask (DM) for write data**
- **Posted CAS by programmable additive latency for better command and data bus efficiency**
- **On-Die Termination (ODT) for better signal quality**
- **Synchronous ODT**
- **Dynamic ODT**
- **Asynchronous ODT**
- **Multi-Purpose Register (MPR) for pre-defined pattern read out**
- **ZQ calibration for DQ drive and ODT Access**
- **Programmable partial array self-refresh (PASR)**
- **RESET pin for Power-up sequence and reset function**
- **SRT (Self Refresh Temperature) range**
- **Normal/Extended/ASR**
- **Programmable output driver impedance control**
- **JEDEC compliant DDR3**
- **RH-Free (Row Hammer Free) option is available**

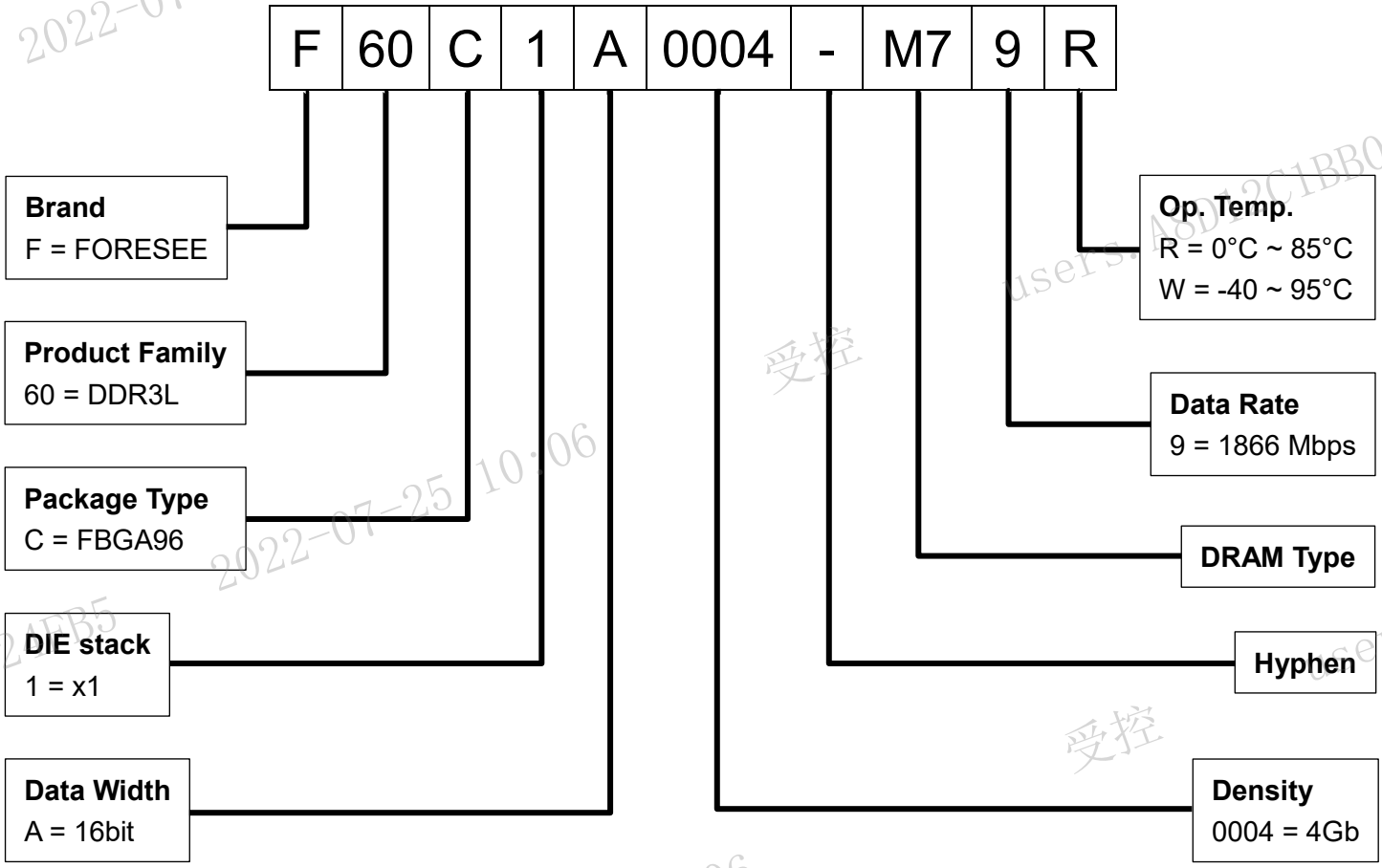
Table 1 Key Timing Parameters

Data Rate (Mbps)	CL	tRCD	tRP
1866	13	13	13
1600	11	11	11
1333	9	9	9

Table 2 Product List

Part Number	Density	Package	Op. Temperature	Size(mm)	VCC Range	Data Rate (Mbps)
F60C1A0004-M79R	4Gb	FBGA 96	0°C to +85°C	7.5*13.5	1.283V ~ 1.45V	1866
F60C1A0004-M79W	4Gb	FBGA 96	-40°C to +95°C	7.5*13.5	1.283V ~ 1.45V	1866

Figure 1 Part Number Decoder



Revision History

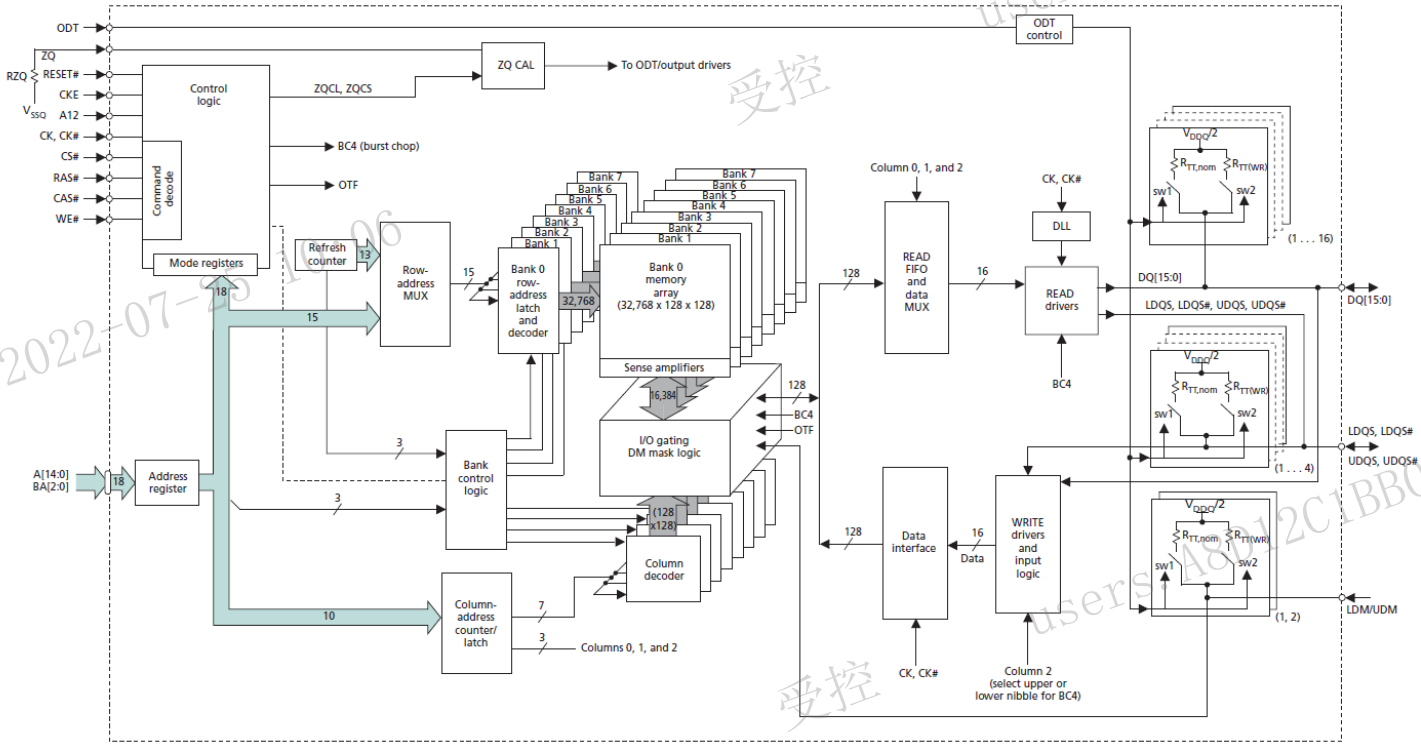
Rev.	Date	Changes	Editor
1.0	2021/07/01	Document Create.	Stephen Huang
1.1	2021/12/01	Add commercial specification	Stephen Huang
1.2	2022/01/10	Fix Pin Descriptions	Stephen Huang
1.3	2022/02/23	Add description of Package Dimensions	Stephen Huang

CONTENTS

1 General Descriptions

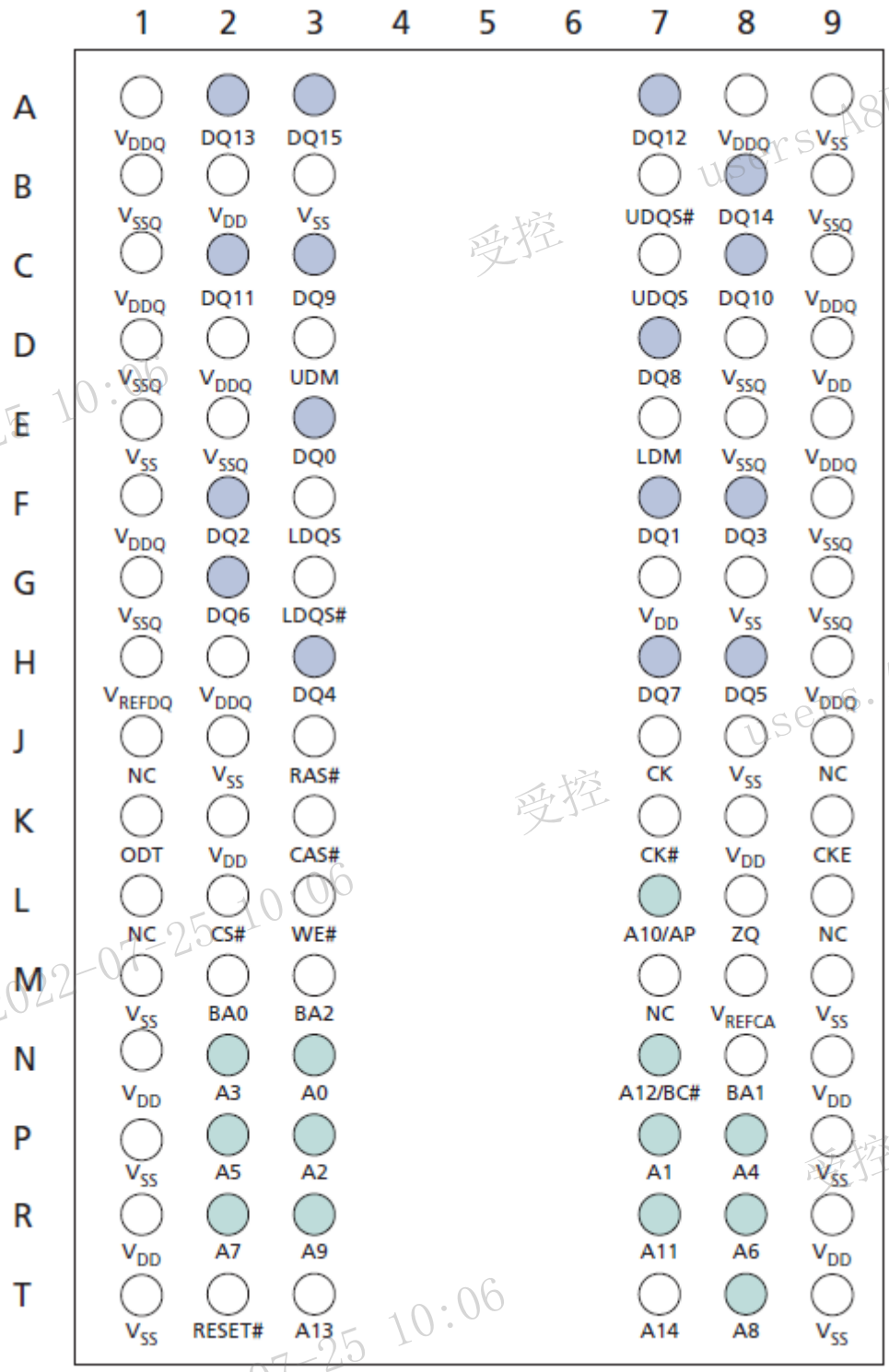
1.1 System Block Diagrams

Figure 2 System Block Diagrams



1.2 Pin Assignments (FBGA 96)

Figure 3. FBGA96 x16 DDR3L Pin (Top view)



1.3 Pin Descriptions (FBGA 96)

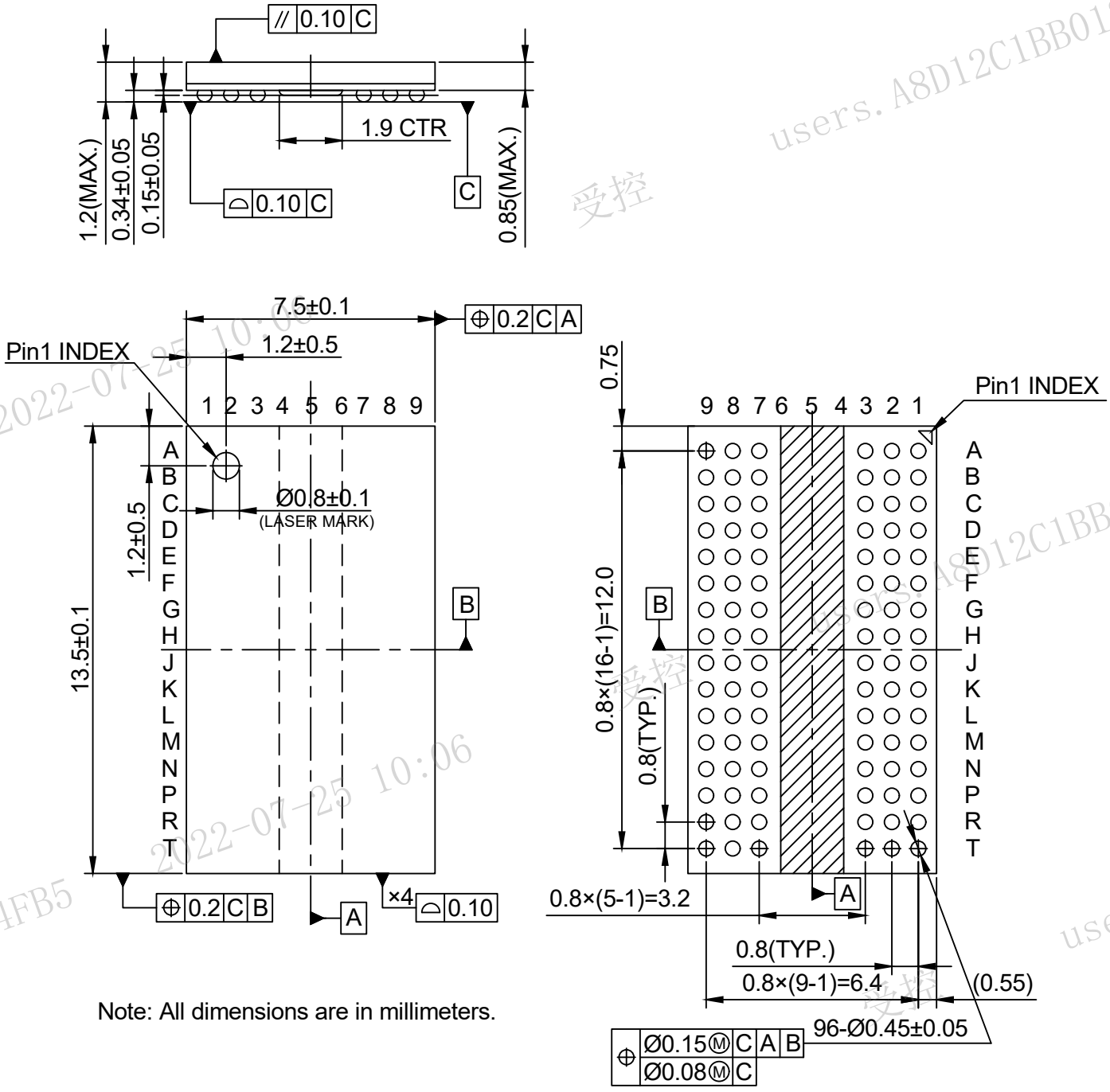
Table 3. FBGA96 x16 DDR3L Pin Descriptions

Symbol	Type	Description
A[14:13], A12, A11, A10, A[9:0]	Input	**Address inputs**: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4).
BA[2:0]	Input	**Bank address inputs**: BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
CK, CK#	Input	**Clock**: CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable**: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/ disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self-refresh entry. CKE is asynchronous for self-refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
CS#	Input	**Chip select**: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CSB is considered part of the command code. CS# is referenced to VREFCA.
DML	Input	**Input data mask**: DML is a lower-byte, input mask signal for write data. Lower-byte input data is masked when DML is sampled HIGH along with the input data during a write access. Although the DML ball is input-only, the DML loading is designed to match that of the DQ and DQS balls. DML is referenced to VREFDQ.
ODT	Input	**On-die termination**: ODT enables (registered HIGH) and disables (registered LOW) Termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQL/DQU[7:0], DQSL, DQSL#, DQSU, DQSU#, DML, and DMU for the x16. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
RAS#, CAS#, WE#	Input	**Command inputs**: RAS#, CAS#, and WEB (along with CS#) define the command being entered and are referenced to VREFCA.
RESET#	Input	**Reset**: RESET# is an active LOW CMOS input referenced to VSS. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × VDD and DC LOW ≤ 0.2 × VDDQ. RESET# assertion and desertion are asynchronous.

Symbol	Type	Description
DQ[15:0]	I/O	**Data input/output**: Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to VREFDQ.
DQS, DQS#	I/O	**Data strobe**: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
VDD	Supply	**Power supply**: 1.5V ±0.075V.
VDDQ	Supply	**DQ power supply**: 1.5V ±0.075V. Isolated on the device for improved noise immunity.
VREFCA	Supply	**Reference voltage for control, command, and address**: VREFCA must be maintained at all times (including self-refresh) for proper device operation.
VREFDQ	Supply	**Reference voltage for data**: VREFDQ must be maintained at all times (excluding self-refresh) for proper device operation.
VSS	Supply	**Ground**.
ZQ	Reference	**External reference ball for output drive calibration**: This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
NC	–	**No connect**: These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

1.4 Package Dimensions

Figure 4. Package Dimensions



Note: All dimensions are in millimeters.

2 COMMAND OPERATION

2.1 Command Sets

The DDR3 SDRAM recognizes the following commands specified by the CS#, RAS#, CAS#, WE# and address pins.

Table 4. Command Truth Table

Function	Symbol	CKE		CS#	RAS#	CAS#	WE#	BA0-2	A12(/BS)	A10(AP)	A0-A15	Note
		Previous	Current									
Mode register set	MRS	H	H	L	L	L	L	BA	op-code			
Auto refresh	REF	H	H	L	L	L	H	V	V	V	V	
Self-refresh entry	SELF	H	L	L	L	L	H	V	V	V	V	6,8,11
Self-refresh exit	SELEX	L	H	H	X	X	X	X	X	X	X	6,8,7
		L	H	L	H	H	H	V	V	V	V	11
Single bank precharge	PRE	H	H	L	L	H	L	BA	V	L	V	
Precharge all banks	PALL	H	H	L	L	H	L	V	V	H	V	
Bank activate	ACT	H	H	L	L	H	H	BA	RA			12
Write (Fixed BL)	WRIT	H	H	L	H	L	L	BA	V	L	CA	
Write (BC4, on the fly)	WRS4	H	H	L	H	L	L	BA	L	L	CA	
Write (BL8, on the fly)	WRS8	H	H	L	H	L	L	BA	H	L	CA	
Write with auto precharge (Fixed BL)	WRITA	H	H	L	H	L	L	BA	V	H	CA	
Write with auto precharge (BC4, on the fly)	WRAS4	H	H	L	H	L	L	BA	L	H	CA	
Write with auto precharge (BL8, on the fly)	WRAS8	H	H	L	H	L	L	BA	H	H	CA	
Read (Fixed BL)	READ	H	H	L	H	L	H	BA	V	L	CA	
Read (BC4, on the fly)	RDS4	H	H	L	H	L	H	BA	L	L	CA	
Read (BL8, on the fly)	RDS8	H	H	L	H	L	H	BA	H	L	CA	
Read with auto precharge (Fixed BL)	READA	H	H	L	H	L	H	BA	V	H	CA	
Read with auto precharge (BC4, on the fly)	RDAS4	H	H	L	H	L	H	BA	L	H	CA	
Read with auto precharge (BL8, on the fly)	RDAS8	H	H	L	H	L	H	BA	H	H	CA	
No operation	NOP	H	H	L	H	H	H	V	V	V	V	9
Device deselect	DESL	H	H	H	X	X	X	X	X	X	X	10
Power down mode entry	PDEN	H	L	H	X	X	X	X	X	X	X	5,11
		H	L	L	H	H	H	V	V	V	V	
Power down mode exit	PDEX	L	H	H	X	X	X	X	X	X	X	5,11
		L	H	L	H	H	H	V	V	V	V	
ZQ calibration long	ZQCL	H	H	L	H	H	L	X	X	H	X	
ZQ calibration short	ZQCS	H	H	L	H	H	L	X	X	L	X	

Remark:
[1] H = VIH; L = VIL; V =VIH or VIL (defined logical level).
[2] X = Don't care (defined or undefined, including floating around VREF) logical level.
[3] BA = Bank Address. RA = Row Address. CA = Column Address. /BC = Bust Chop.

Notes:
[1] All DDR3 commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The most significant bit (MSB) of BA, RA, and CA are device density and configuration dependent.
[2] RESET# is an active low asynchronous signal that must be driven high during normal operation.
[3] Bank Addresses (BA) determines which bank is to be operated upon. For MRS, BA selects a mode register.
[4] Burst READs or WRITEs cannot be terminated or interrupted and fixed/on the fly BL will be defined by MRS.
[5] The power-down mode does not perform any refresh operations.
[6] The state of ODT does not affect the states described in this table. The ODT function is not available during self-refresh.
[7] Self-refresh exit is asynchronous.
[8] VREF (both VREFDQ and VREFCA) must be maintained during self-refresh operation. VREFDQ supply may be turned off and VREFDQ may take any value between VSS and VDD during self-refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write leveling activity may not occur earlier than 512 nCK after exit from self-refresh.
[9] The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
[10] The DESL command performs the same function as a NOP command.
[11] Refer to the CKE Truth Table for more detail with CKE transition.
[12] No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

2.2 No Operation Command [NOP]

The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
The no operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# low, RAS#, CAS#, WE# high).
This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

2.3 Device Deselect Command [DESL]

The deselect function (CS# high) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

2.4 Mode Register Set Command [MR0 to MR3]

The mode registers are loaded via row address inputs. See mode register descriptions in the Programming the mode register section. The mode register set command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

2.5 Bank Activate Command [ACT]

This command is used to open (or activate) a row in a particular bank for a subsequent access. The values on the BA inputs select the bank, and the address provided on row address inputs selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.
Note: No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

2.6 Read Command [READ, RDS4, RDS8, READA, RDAS4, RDAS8]

The read command is used to initiate a burst read access to an active row. The values on the BA inputs select the bank, and the address provided on column address inputs selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

2.7 Write Command [WRIT, WRS4, WRS8, WRITA, WRAS4, WRAS8]

The write command is used to initiate a burst write access to an active row. The values on the BA inputs select the bank, and the address provided on column address inputs selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data will be written to memory; if the DM signal is registered high, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

2.8 Precharge Command [PRE, PALL]

The precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA select the bank. Otherwise, BA are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any read or write commands being issued to that bank. A precharge command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

2.9 Auto precharge Command [READA, WRITA]

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto precharge function. When a read or a write command is given to the DDR3 SDRAM, the CAS# timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the read or write command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the read or write command is issued, then the auto precharge function is engaged. During auto precharge, a read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is (AL* + tRTP) cycles later from the read with auto precharge command.

Auto precharge can also be implemented during write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS# latency) thus improving system performance for random data access. The tRAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

Note: AL (Additive Latency), refer to Posted CAS# description in the Register Definition section.

2.10 Auto-Refresh Command [REF]

Auto-refresh is used during normal operation of the DDR3 SDRAM and is analogous to CAS#-before-RAS# (CBR) refresh in FPM/EDO DRAM. This command is non persistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an auto-refresh command.

A maximum of eight auto-refresh commands can be posted to any given DDR3, meaning that the maximum absolute interval between any auto-refresh command and the next auto-refresh command is 9 x tREFI. This maximum absolute interval is to allow DDR3 output drivers and internal terminators to automatically recalibrate compensating for voltage and temperature changes.

2.11 Self-Refresh Command [SELF]

The self-refresh command can be used to retain data in the DDR3, even if the rest of the system is powered down. When in the self-refresh mode, the DDR3 retains data without external clocking. The self-refresh command is initiated like an auto-refresh command except CKE is disabled (low).

The DLL is automatically disabled upon entering self-refresh and is automatically enabled and reset upon exiting self-refresh. The active termination is also disabled upon entering self-refresh and enabled upon exiting self-refresh. (512 clock cycles must then occur before a read command can be issued). Input signals except CKE are "Don't Care" during self-refresh. The procedure for exiting self-refresh requires a sequence of commands.

First, CK and /CK must be stable prior to CKE going back high. Once CKE is high, the DDR3 must have NOP commands issued for tXS DLL because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and out-put calibration is to apply NOPs for 512 clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.

2.12 ZQ calibration Command [ZQCL, ZQCS]

ZQ calibration command (short or long) is used to calibrate DRAM RON and ODT values over PVT. ZQ Calibration Long (ZQCL) command is used to perform the initial calibration during power-up initialization sequence.

ZQ Calibration Short (ZQCS) command is used to perform periodic calibrations to account for VT variations. All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self-refresh.

2.13 CKE Truth Table

[Refer to section 4.2 in JEDEC Standard No. JESD79-3F]

3 Electrical Characteristic

All voltages are referenced to each VSS (GND).
Execute power-up and Initialization sequence before proper device operation can be achieved.

3.1 Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	-0.4	1.975	V	1
V_{DDQ}	V_{DD} supply voltage relative to V_{SSQ}	-0.4	1.975	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4	1.975	V	
T_C	Operating case temperature - Commercial	0	85	°C	2, 3
	Operating case temperature - Industrial	-40	95	°C	2, 3
T_{STG}	Storage temperature	-55	150	°C	

Notes:
[1] V_{DD} and V_{DDQ} must always be within 300mV of each other, and V_{REF} must not be greater than 0.6 × V_{DDQ}.
When V_{DD} and V_{DDQ} are < 500mV, V_{REF} can be ≤ 300mV.
[2] MAX operating case temperature. T_C is measured in the center of the package.
[3] Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

3.2 Operating Temperature Condition

Table 6. Operating Temperature Condition

Product grades	Parameter	Symbol	Rating	Unit	Note
Commercial	Operating case temperature	T_C	0 to +85	°C	1, 2, 3, 4
Industrial	Operating case temperature	T_C	-40 to +95	°C	1, 2, 3, 4

Notes:
[1] MAX operating case temperature T_C is measured in the center of the package, as shown below.
[2] A thermal solution must be designed to ensure that the device does not exceed the maximum T_C during operation.
[3] Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
[4] If T_C exceeds 85°C, but is less than 95°C, the DRAM must be refreshed manually at 2x refresh(7.8μs), which is a 3.9μs interval refresh rate. The use of self-refresh temperature (SRT) or automatic self-refresh (ASR), must be enabled.

3.3 Recommended DC Operating Conditions

Table 7. Recommended DC operating Conditions for DDR3L (1.35V)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1~7
I/O Supply voltage	V_{DDQ}	1.283	1.35	1.45	V	1~7

Notes:
[1] V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be ≤ V_{DD}. VSS = VSSQ.
[2] V_{DD} and V_{DDQ} may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
[3] Maximum DC value may not be greater than 1.425V. The DC value is the linear average of $V_{DD}/V_{DDQ}(t)$ over a very long period of time (for example, 1 second).
[4] Under these supply voltages, the device operates to this DDR3L specification.
[5] If the maximum limit is exceeded, input levels shall be governed by DDR3specifications.
[6] Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.
[7] Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3 operation (see V_{DD} Voltage Switching.

3.4 DC Characteristics

Speed / Parameter	Symbol	DDR3L-1333	DDR3L-1600	DDR3L-1866	Units	Notes
Operating current 0: One bank ACTIVATE-to- PRECHARGE	IDD0	55	57	59	mA	1, 2
Operating current 1: One bank ACTIVATE-to-READ-to- PRECHARGE	IDD1	78	81	84	mA	1, 2
Precharge power-down current: Slow exit	IDD2P0	8	8	8	mA	1, 2
Precharge power-down current: Fast exit	IDD2P1	12	14	16	mA	1, 2
Precharge quiet standby current	IDD2Q	22	24	26	mA	1, 2
Precharge standby current	IDD2N	22	24	26	mA	1, 2
Precharge standby ODT current	IDD2NT	29	31	33	mA	1, 2
Active power-down current	IDD3P	24	26	28	mA	1, 2
Active standby current	IDD3N	36	38	40	mA	1, 2
Burst read operating current	IDD4R	145	155	165	mA	1, 2
Burst write operating current	IDD4W	145	155	165	mA	1, 2
Burst refresh current	IDD5B	229	235	242	mA	1, 2
Room temperature self-refresh	IDD6	12	12	12	mA	1, 2, 3
Extended temperature self-refresh	IDD6ET	16	16	16	mA	2, 4
All banks interleaved read current	IDD7	180	190	200	mA	1, 2
Reset current	IDD8	IDD2P + 2mA	IDD2P + 2mA	IDD2P + 2mA	mA	1, 2

Notes:
[1] T_C = 85°C; SRT and ASR are disabled.
[2] Enabling ASR could increase $I_{DD[x]}$ by up to an additional 2mA.
[3] Restricted to $T_{C(MAX)}$ = 85°C.
[4] T_C = 85°C; ASR and ODT are disabled; SRT is enabled.
[5] The I_{DD} values must be derated (increased) on IT-option devices when operated outside of the range 0°C ≤ TC ≤ +85°C:
5a) When TC < 0°C: IDD2P0, IDD2P1 and IDD3P must be derated by 4%; IDD4R and IDD4W must be derated by 2%; and IDD6, IDD6ET and IDD7 must be derated by 7%.
5b) When TC > 85°C: IDD0, IDD1, IDD2N, IDD2NT, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, and IDD5B must be derated by 2%; IDD2Px must be derated by 30%.

3.5 Pin Capacitance(T_C = 25°C, VDD, VDDQ = 1.35V)

Table 8. Pin Capacitance

Capacitance Parameters	Symbol	DDR3L-1333		DDR3L-1600		DDR3L-1866		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Input/output capacitance	C_{IO}	1.4	2.2	1.4	2.2	1.4	2.2	pF	1,2
Input capacitance, CK and CK#	C_{CK}	0.8	1.4	0.8	1.4	0.8	1.4	pF	2
Input capacitance delta, CK and CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	pF	2, 3
Input/output capacitance delta DQS and DQS#	C_{DDQS}	0	0.15	0	0.15	0	0.15	pF	3
Input capacitance, (CTRL, ADD, CMD input-only pins)	C_I	0.75	1.3	0.75	1.2	0.75	1.2	pF	3
Input capacitance delta, (All CTRL input-only pins)	C_{DI_CTRL}	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	4
Input capacitance delta, (All ADD/CMD input-only pins)	$C_{DI\_ADD\_CMD}$	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	5
Input/output capacitance delta, (All I/O pins)	C_{DIO}	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	6
Input/output capacitance of ZQ pin	C_{ZQ}	-	3	-	3	-	3	pF	7

Notes:
1. V_{DD} = 1.35V (1.283–1.45V), V_{DDQ} = V_{DD}, V_{REF} = V_{SS}, f = 100 MHz, T_C = 25°C. $V_{OUT(DC)}$ = 0.5 × V_{DDQ}, V_{OUT} = 0.1V (peak-to-peak).
2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes. C_{DDQS} is for DQS vs. DQS# separately.
4. C_{DIO} = $C_{IO(DQ)}$ - 0.5 × ($C_{IO(DQS)}$ + $C_{IO(DQS\#)}$).
5. Excludes CK, CKB; CTRL = ODT, CSB, and CKE; CMD = RASB, CASB, and WEB; ADDR = A[n:0], BA[2:0].
6. C_{DI_CTRL} = $C_{I(CTRL)}$ - 0.5 × ($C_{CK(CK)}$ + $C_{CK(CKB)}$).
7. $C_{DI\_CMD\_ADDR}$ = $C_{I(CMD\_ADDR)}$ - 0.5 × ($C_{CK(CK)}$ + $C_{CK(CKB)}$).

(End of Document)