1-MSPS, ULTRA LOW POWER, 3.0 V – 4.5 V, 10-BIT SAR ANALOG-TO-DIGITAL CONVERTER

DESCRIPTION

The XC11663A is a 10-bit, high speed, low power, and small-sized Successive-Approximation-Register (SAR) ADC. The supply current drops at lower sampling rates because the device automatically power down after conversion.

The XC11663A version can operate from a single 3.0 V to 4.5 V supply with a 1-MSPS throughput.

The XC11663A is available in a 6-pin SOT-23 package and has an operating temperature range of -40°C to 85°C.

The XC11663A is a drop-in replacement for the MAX11663.

FEATURES

- Single 3.0 V to 4.5 V Supply Operation for XC11663A
- Fast Throughput Rate: 1 MSPS
- 10-Bit Resolution
- Low Power (XC11663A typical):
  2.20mW (3.3 V, 1 MSPS)
  9.60mW (4.5 V, 1 MSPS)
- ±0.5LSB INL, ±0.5LSB DNL
- No Data Latency
- SPI/QSPI/MICROWIRE™ Compatible Serial Interface
- Guaranteed Operation from –40°C to 85°C
- 6-Pin SOT-23 Package
- Second-Source for MAX11663

APPLICATIONS

- Data Acquisition
- Portable Data Logging
- Medical Instrumentation
- Battery-Operated Systems
- Communication Systems
- Automotive

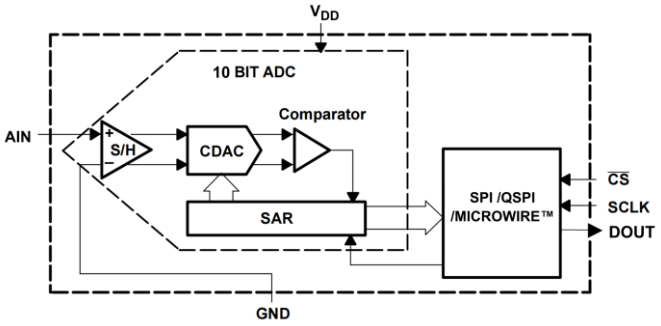


Figure 1. Functional Block Diagram

SPECIFICATIONS

At-40℃ to 85℃, f_{SAMPLE} = 1 MSPS and f_{SCLK} = 16.6 MHz if 3.0 V ≤ V_{DD} ≤ 4.5 V. (unless otherwise noted)

PARAMETER	TEST CONDITIONS	XC11661A			XC11663A			XC11665A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE											
Resolution			**8**			**10**			**12**		Bits
No missing codes		**8**			**10**			**12**			Bits
Integral linearity			**0.5**			**0.5**			**1**		LSB
Differential linearity			**0.5**			**0.5**			**1**		LSB
f_{SAMPLE} Throughput rate	f_{SCLK} = 16.6 MHz, 3.0 V ≤ V_{DD} ≤ 4.5 V			**1**			**1**			**1**	MSPS
SNR	f_{IN} = 100 kHz		**49**			**61**			**72**		dB
THD	f_{IN} = 100 kHz		**-66**			**-73.5**			**-83**		dB

XC11663A

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 16.6 MHz, V_{DD} = 3.3 V		**0.66**	**1.51**	mA
		f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 16.6 MHz, V_{DD} = 4.5 V		**2.13**	**3.38**	
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16.6 MHz, V_{DD} = 3.3 V		**0.54**	**1.24**	
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16.6 MHz, V_{DD} = 4.5 V		**1.72**	**2.78**	
POWER DISSIPATION, XC11663A						
Normal operation		f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 16.6 MHz, V_{DD} = 3.3 V		**2.20**	**5.00**	mW
		f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 16.6 MHz, V_{DD} = 4.5 V		**9.60**	**15.2**	mW

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

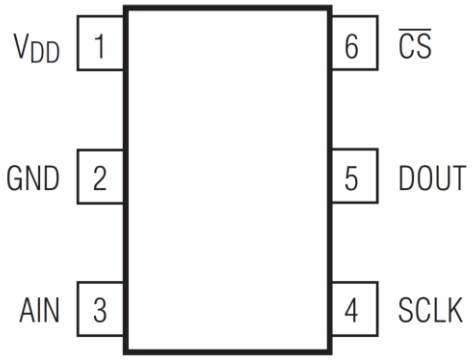


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
V_{DD}	1	Power Supply Input.
GND	2	The ground return for the supply and signals.
AIN	3	Analog Input. This signal can range from 0 V to V_{DD}.
SCLK	4	Digital clock input. This clock directly controls the conversion and readout processes.
DOUT	5	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
$\overline{CS}$	6	Chip Select. On the falling edge of $\overline{CS}$, a conversion process begins.

TYPICAL CONNECTION

Figure 3 shows a typical connection diagram for the XC11663A. The 3.3 V supply should come from a stable power supply such as an LDO. The supply to XC11663A should be decoupled to the ground. Two decoupling capacitors, one 1-µF and one 10-nF, are suggested to be inserted between the V_{DD} and GND pins of the converter. The capacitors should be placed as close as possible to the pins of the device. Always set the V_{DD} supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

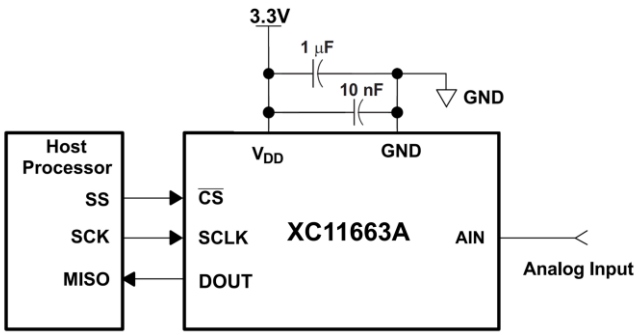


Figure 3. Typical Circuit Configuration

TIMING DIAGRAM

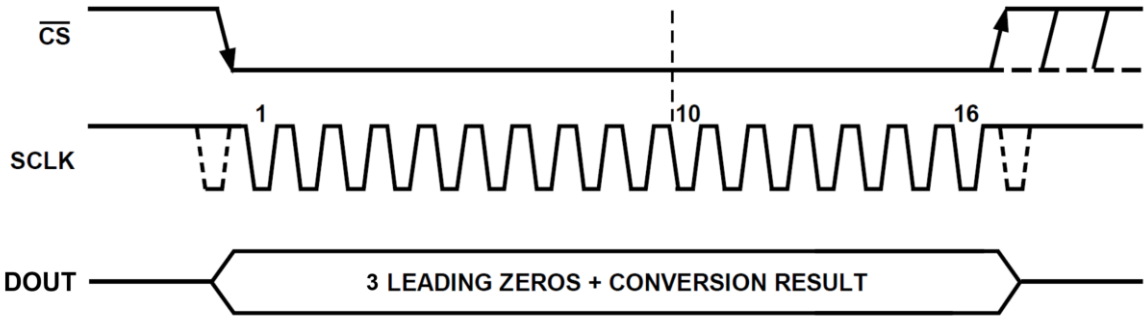


Figure 4. Timing Diagram

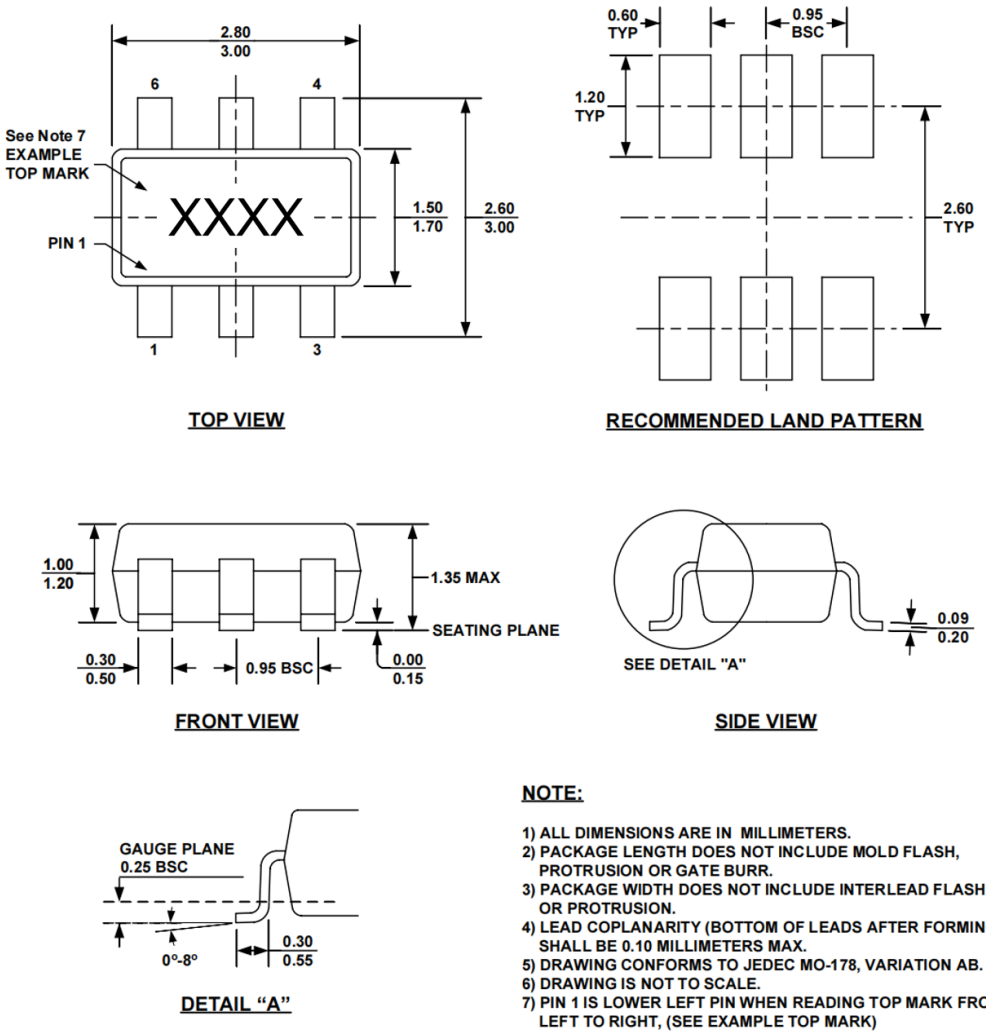
Unlike the MAX11663 series conversion, the MAX11663 will output the conversion result through DOUT after the second SCLK falling edge after the falling edge of $\overline{CS}$. However, the XC11663A series will output 3 leading zeros from DOUT following the 10-bit conversion result after the fourth SCLK falling edge after the $\overline{CS}$ falling edge, with the 8-bit result followed by four trailing zeros, and the 10-bit result followed by two trailing zeros. After that, DOUT enters a three-state and the transition cycle ends.

POWER-DOWN MODE

The XC11663A has an auto power-down feature. Besides powering down all circuitry, the converter consumes only a small amount of current in this mode. The device automatically wakes up when $\overline{CS}$ falls. However, not all of the functional blocks are fully powered until sometime before the third falling edge of SCLK. The device powers down once it reaches the end of conversion which is the 16th falling edge of SCLK for the XC11663A. The device enters power down mode if $\overline{CS}$ goes high before the 10th SCLK falling edge. Ongoing conversion stops and DOUT goes to three-state under this power down condition.

These converters achieve lower power dissipation for a fixed throughput rate by using higher SCLK frequencies. Higher SCLK frequencies reduce the acquisition time and conversion time. This means the converters spend more time in auto power-down mode per conversion cycle. For a particular SCLK frequency, the acquisition time and conversion time are fixed. Therefore, a lower throughput increases the proportion of the time the converters are in power down, thereby reducing power consumption.

OUTLINE DIMENTIONS



NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.
2. After access, the components are stored in an electrostatic packaging protective bag.
3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.
4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.