SY8686R

High Efficiency and High Integration PMIC

Advanced Design Specification

General Description

The SY8686R is an integrated power management unit. It is designed to power a wide range of microcontrollers and solid-state drive applications.

The device includes 3 buck converters using integrated power FETs and 2 low-dropout regulators (LDOs). The Buck1 and LDO2 can also be configured as load switch, which is not a programmable function by I^2C interface. Each of the regulators can be programmed for a wide range of output voltages through the I^2C interface. Each buck converter switches at high switching frequency, requiring only three small components for operation.

The SY8686R is available in a 2.42 x 2.82 mm 36balls CSP package.

Ordering Information

SY8686 □(□□ □)

- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8686RUXS	CSP2.42×2.82-36	

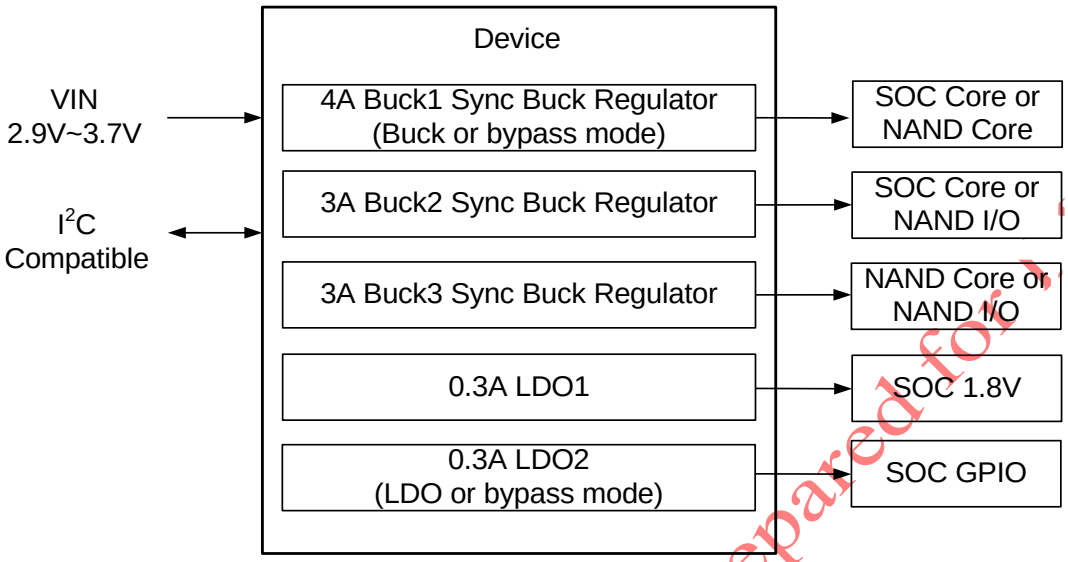
Features

- Wide Input Voltage Range
  - Vin = 2.9V to 3.7V
- Channel 1 Synchronous Buck:
  - 4A Maximum Output Current Capability
  - 2.1V to 3.3V Programmable, 12.5mV Step
  - Bypass Mode or Buck Mode Selection
  - 40mohm/25mohm R_{DS_ON}
- Channel 2 Synchronous Buck:
  - 3A Maximum Output Current Capability
  - 0.6V to 1.5V Programmable, 9.375mV Step
  - 80mohm/35mohm R_{DS_ON}
- Channel 3 Synchronous Buck:
  - 3A Maximum Output Current Capability
  - 1.0V to 3.3V Programmable, 12.5mV Step
  - 50mohm/50mohm R_{DS_ON}
- Channel 4 LDO1:
  - 0.3A Maximum Output Current Capability
  - 1.0V to 2.5V Programmable, 12.5mV Step
- Channel 5 LDO2:
  - 0.3A Maximum Output Current Capability
  - 1.6V to 3.3V Programmable, 12.5mV Step
- I_2C Interface up to 1MHz
- Auto PWM/PFM or Forced PWM Controlled by I^2C Interface
- Output Voltage Level of Each Channel Controlled by I^2C Interface
- Reliable Protections:
  - Input/output Over Voltage Protection (OVP)
  - Short Circuit Protection (SCP)
  - Over Temperature Protection (OTP)
- Compact Package: CSP2.42×2.82-36

Applications

- Solid State Drives
- Microcontroller

Application Circuit

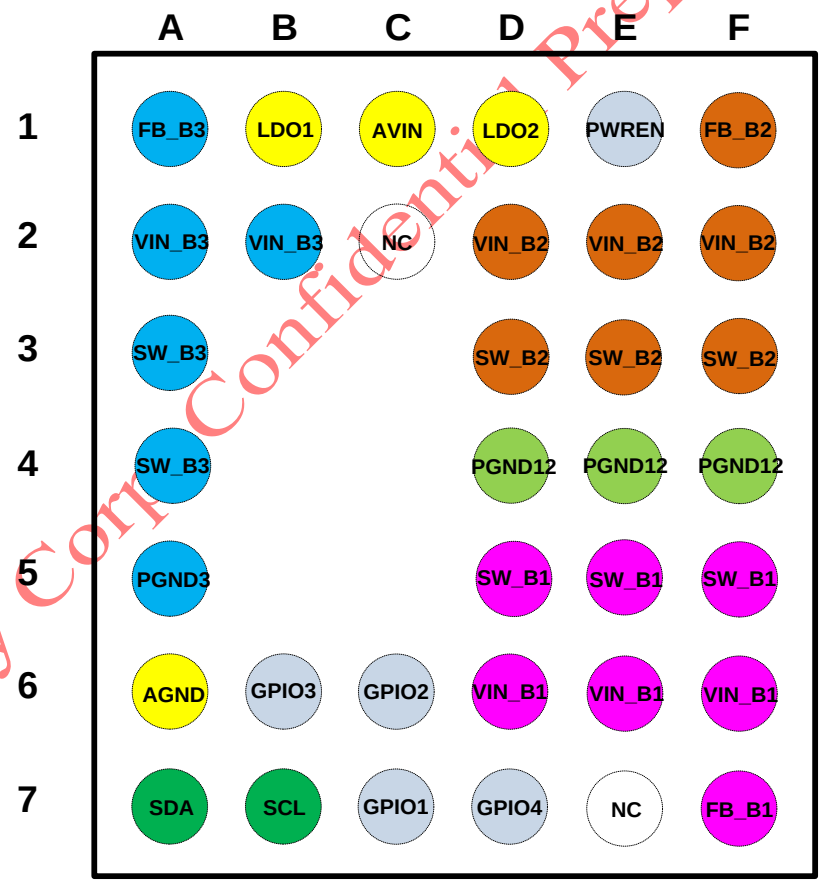


Note: Operation mode of Buck1 & LDO2 is defined in Table 3

Figure 1. Simplified Application Circuit

Pin-out (top view)

	A	B	C	D	E	F
1	FB_B3	LDO1	AVIN	LDO2	PWREN	FB_B2
2	VIN_B3	VIN_B3	NC	VIN_B2	VIN_B2	VIN_B2
3	SW_B3			SW_B2	SW_B2	SW_B2
4	SW_B3			PGND12	PGND12	PGND12
5	PGND3			SW_B1	SW_B1	SW_B1
6	AGND	GPIO3	GPIO2	VIN_B1	VIN_B1	VIN_B1
7	SDA	SCL	GPIO1	GPIO4	NC	FB_B1



(CSP2.42×2.82-36)

Top Mark: GYN*xyz*(Device code: GYN, ***x=year code, y=week code, z= lot number code***)

Pin Descriptions

Pin Number	Pin Name	Pin Description
A1	FB_B3	Feedback for Buck3 Regulator.
B1	LDO1	Output for LDO1 Regulator.
C1	AVIN	Dedicated VIN Power Input for LDO1 & 2 Regulators and Analog VIN nput.
D1	LDO2	Output for LDO2 Regulator.
E1	PWREN	Power Enable Input.
F1	FB_B2	Feedback for Buck2 Regulator.
A2,B2	VIN_B3	Dedicated Buck3 VIN Power Input.
C2	NC	Not Connected.
D2,E2,F2	VIN_B2	Dedicated Buck2 VIN Power Input.
A3,A4	SW_B3	Switch Pin for Buck3 Regulator.
D3,E3,F3	SW_B2	Switch Pin for Buck2 Regulator.
D4,E4,F4	PGND12	Power Ground for Buck1 and Buck2.
A5	PGND3	Power Ground for Buck3.
D5,E5,F5	SW_B1	Switch Pin for Buck1 Regulator.
A6	AGND	Analog Ground.
B6	GPIO3	General Purpose I/O Port 3.
C6	GPIO2	General Purpose I/O Port 2.
D6,E6,F6	VIN_B1	Dedicated Buck1 VIN Power Input.
A7	SDA	I2C Data Input and Output.
B7	SCL	I2C Clock Input.
C7	GPIO1	General Purpose I/O Port 1.
D7	GPIO4	General Purpose I/O Port 4.
E7	NC	Not Connected.
F7	FB_B1	Feedback for Buck1 Regulator.

Function Block Diagram

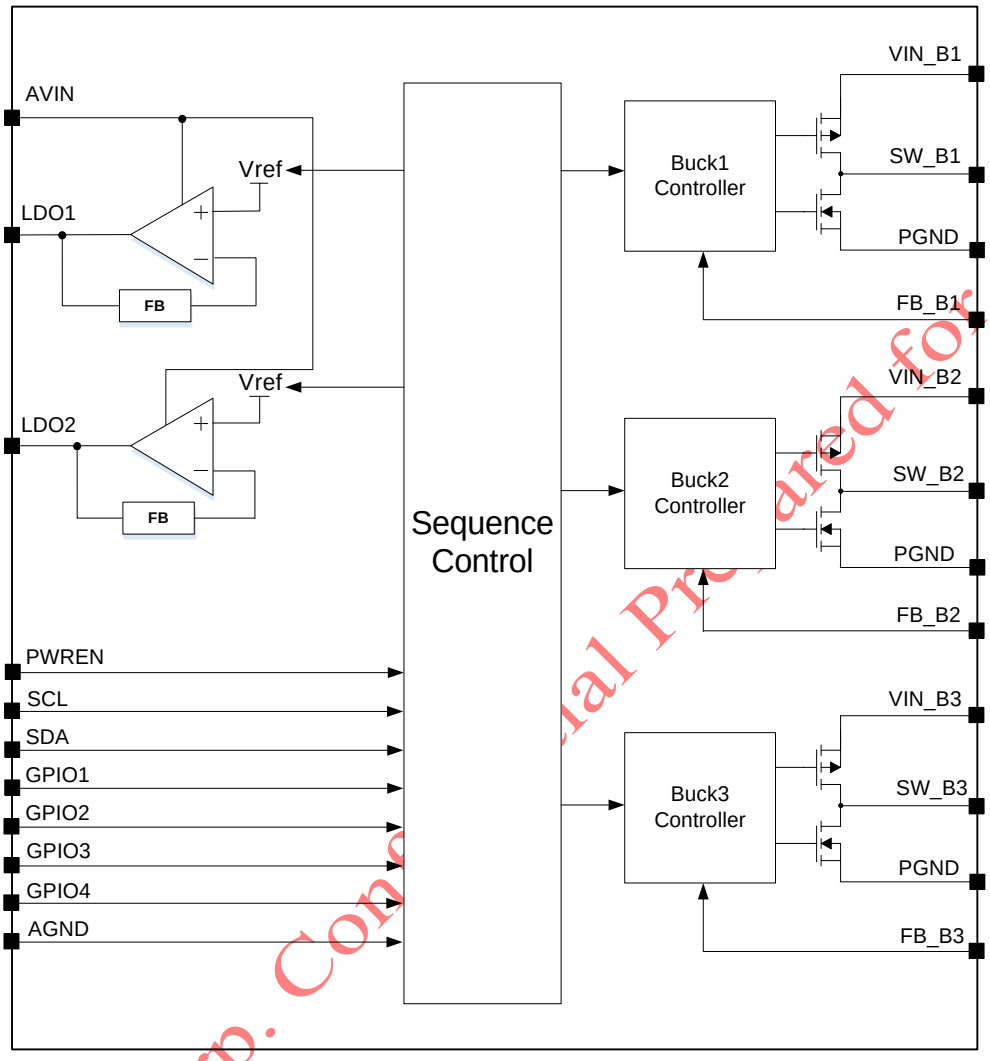


Figure 2. Function Block Diagram

Power On/Off Sequence

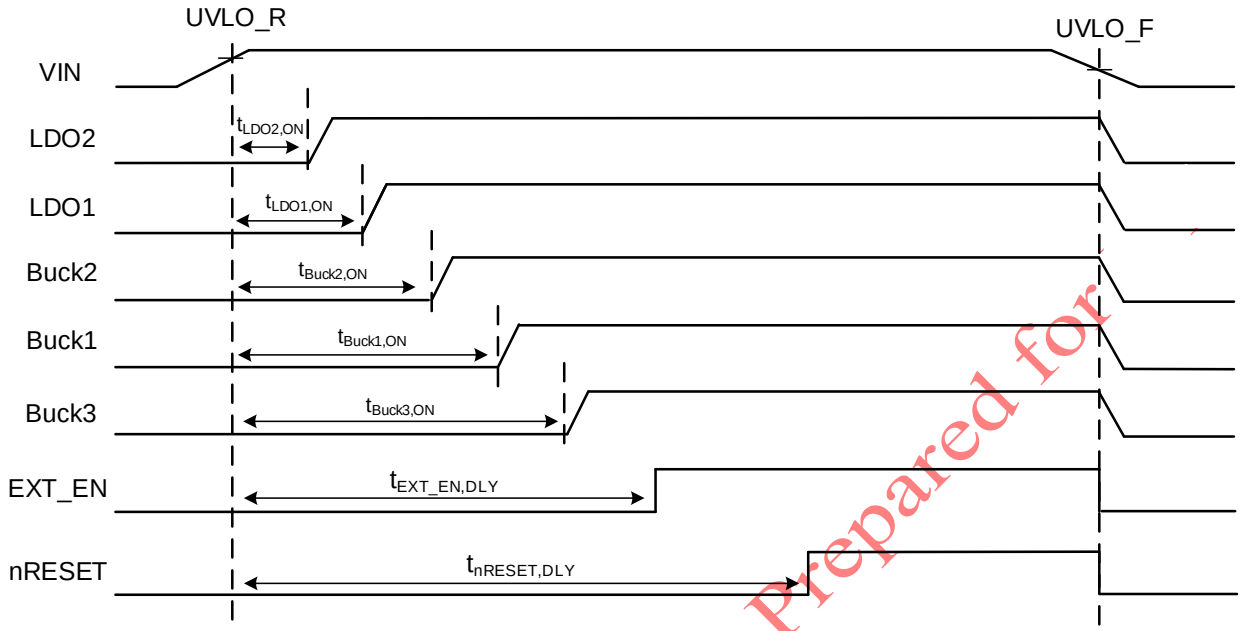


Figure 3. Power on/off Sequence

- Power-on delay time of power rail:
  $t_{LDO1,ON}/t_{LDO2,ON}/t_{Buck1,ON}/t_{Buck2,ON}/t_{Buck3,ON}$=0.5~8ms, 0.5ms/Step.
- EXT_EN delay time: $t_{EXT\_EN,DLY}$=3ms~9ms, 2ms/Step.
- nRESET delay time: $t_{nRESET,DLY}$ =4ms~28ms,4ms/Step.

Absolute Maximum Ratings (Note 1)

All Pins to GND ---------- -0.3 to 6V
Power Dissipation,
P_D @ T_A = 25°C CSP 2.42×2.82-36 ---------- 2.56W
Package Thermal Resistance (Note 2)
θ_{JA} , CSP 2.42×2.82-36 ---------- 39°C/W
θ_{JC} , CSP 2.42×2.82-36 ---------- 0.5°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -55°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage, VIN---------- 2.7V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN}=3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Inputs Voltage			2.9		3.7	V
UVLO Threshold Rising	$V_{UVLO,Rising}$			2.6	2.7	V
UVLO Hysteresis	$V_{UVLO,HYS}$			100		mV
Operating Supply Current		All regulators disabled		30		μA
Operating Supply Current		All regulators enabled but no load		200		μA
Logic Level High	V_{HIGH}		1.2			V
Logic Level Low	V_{LOW}				0.4	V
Thermal Shutdown		Temperature rising		150		°C
Thermal Shutdown Hysteresis				15		°C
VIN OV Shutdown Threshold Rising				3.9		V
VIN OV Shutdown Threshold Falling				3.6		V
VIN OVP Deglitch Time				20		μs
Buck1						
Output Voltage Range	V_{OUT1}	Controllable by I²C interface	2.1		3.3	V
Output Voltage Accuracy	ΔV_{OUT1}	PWM mode operation	-1		1	%
Switching Frequency	F_{OSC1}			2.25		MHz
Main PFET R_{DS_ON}	$R_{DS\_ON,P1}$			40		mΩ
Main NFET R_{DS_ON}	$R_{DS\_ON,N1}$			25		mΩ
High Side FET Current Limit	I_{LIM1_HS}		5.1			A
Maximum Output DC Load Current	I_{OUT1}		4			A
Internal Soft Start Time	T_{SS1}	10% to 90% of V_{NOM}		500		μs
Discharge Resistor	R_{DIS1}			4.4	8.75	Ω
OVP Threshold	V_{OVP1}		115	120	125	%
OVP Hysteresis	$V_{OVP1,HYS}$			5		%
OVP Deglitch Time	t_{OVP1}			20		μs
Short Circuit Protection Threshold	V_{SCP1}			30		%
Short Circuit Protection Deglitch Time	t_{SCP1}			50		μs
Buck1 @ Bypass Mode						
Output Voltage Range	V_{OUT1}		2.9		3.7	V
Main PFET R_{ON}	$R_{DS\_ON,P1}$			40		mΩ
Load Switch Current Limit	I_{LIM1_HS}	Shut down after deglitch time and stays off for off-time	5.1			A
Load Switch Current Shutdown Deglitch Time	t_{LIM1_HS}			200		μs

Load Switch Current Shutdown Off-time				10		ms
Internal Soft Start Time	T_{SS1}	10% to 90% of V_{NOM}		500		µs
Short Circuit Protection Threshold	V_{SCP1}			30		%
Short Circuit Protection Deglitch Time	t_{SCP1}			50		µs
Buck2						
Output Voltage Range	V_{OUT2}	Controllable by I²C interface	0.6		1.5	
Output Voltage Accuracy	ΔV_{OUT2}	PWM mode operation	-1		1	%
Switching Frequency	F_{OSC2}			2.25		MHz
Main PFET R_{DS_ON}	$R_{DS\_ON,P2}$			80		mΩ
Main NFET R_{DS_ON}	$R_{DS\_ON,N2}$			35		mΩ
High Side FET Current Limit	I_{LIM2_HS}		4.2			A
Maximum Output DC Load Current	I_{OUT2}		3			A
Internal Soft Start Time	T_{SS2}	10% to 90% of V_{NOM}		500		µs
Discharge Resistor	R_{DIS2}			9.4	20	Ω
OVP Threshold	V_{OVP2}		115	120	125	%
OVP Hysteresis	$V_{OVP2,HYS}$			5		%
OVP Deglitch Time	t_{OVP2}			20		µs
Short Circuit Protection Threshold	V_{SCP2}			30		%
Short Circuit Protection Deglitch Time	t_{SCP2}			50		µs
Buck3						
Output Voltage Range	V_{OUT3}	Controllable by I²C interface	1		3.3	V
Output Voltage Accuracy	ΔV_{OUT3}	PWM mode operation	-1		1	%
Switching Frequency	F_{OSC3}			2.25		MHz
Main PFET R_{DS_ON}	$R_{DS\_ON,P3}$			50		mΩ
Main NFET R_{DS_ON}	$R_{DS\_ON,N3}$			50		mΩ
High Side FET Current Limit	I_{LIM3_HS}		4.2			A
Maximum Output DC Load Current	I_{OUT3}		3			A
Internal Soft Start Time	T_{SS3}	10% to 90% of V_{NOM}		500		µs
Discharge Resistor	R_{DIS3}			9.4	20	Ω
OVP Threshold	V_{OVP3}		115	120	125	%
OVP Hysteresis	$V_{OVP3,HYS}$			5		%
OVP Deglitch Time	t_{OVP3}			20		µs
Short Circuit Protection Threshold	V_{SCP3}			30		%
Short Circuit Protection Deglitch Time	t_{SCP3}			50		µs
LDO1/2						

LDO1 Output Voltage Range	V_{OUT_LDO1}	Controllable by I²C interface	1		2.5	V
Output Voltage Accuracy	$\Delta V_{OUT\_LDO1/2}$		-1		1	%
Current Limit	$I_{LIM\_LDO1/2}$		0.4			A
Current Shutdown Deglitch Time	$t_{LIM\_LDO1/2}$			200		µs
Maximum Output DC Load Current	$I_{OUT\_LDO1/2}$		0.3			A
Internal Soft Start Time	$T_{SS\_LDO1/2}$	10% to 90% of V_{NOM}		215		µs
Discharge Resistor	$R_{DIS\_LDO1/2}$			50	125	Ω
OVP Threshold	$V_{OVP\_LDO1/2}$		115	120	125	%
OVP Hysteresis	$V_{OVP\_LDO1/2,HYS}$			5		%
OVP Deglitch Time	$t_{OVP\_LDO1/2}$			10		µs
Short Circuit Protection Threshold	$V_{SCP\_LDO1/2}$			30		%
Short Circuit Protection Deglitch Time	$t_{SCP\_LDO1/2}$			50		µs
LDO2 @ Bypass Mode						
Output Voltage Range	$V_{LDO2,BYPASS}$		2.9	3.3	3.7	V
Main PFET R_{DS_ON}	$R_{DS\_ON,LDO2}$			300		mΩ
Load Switch Current Limit	I_{LIM_HS}		0.4			A
Load Switch Current Shutdown Deglitch Time	t_{LIM_HS}			200		µs
Load Switch Current Shutdown Off-time				10		ms
Internal Soft Start Time	T_{SS_LDO2}	10% to 90% of V_{NOM}		215		µs
Short Circuit Protection Threshold	$V_{SCP,LDO2}$			30		%
Short Circuit Protection Deglitch Time	$t_{SCP,LDO2}$			50		µs
I²C Compatible I/O (SDA,SCL)						
Maximum Operating Frequency	f_{SCL}			400		kHz
SDA and SCL Pin Input Logic Thresholds	Logic Low				0.4	V
	Logic High		1.2			V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Application

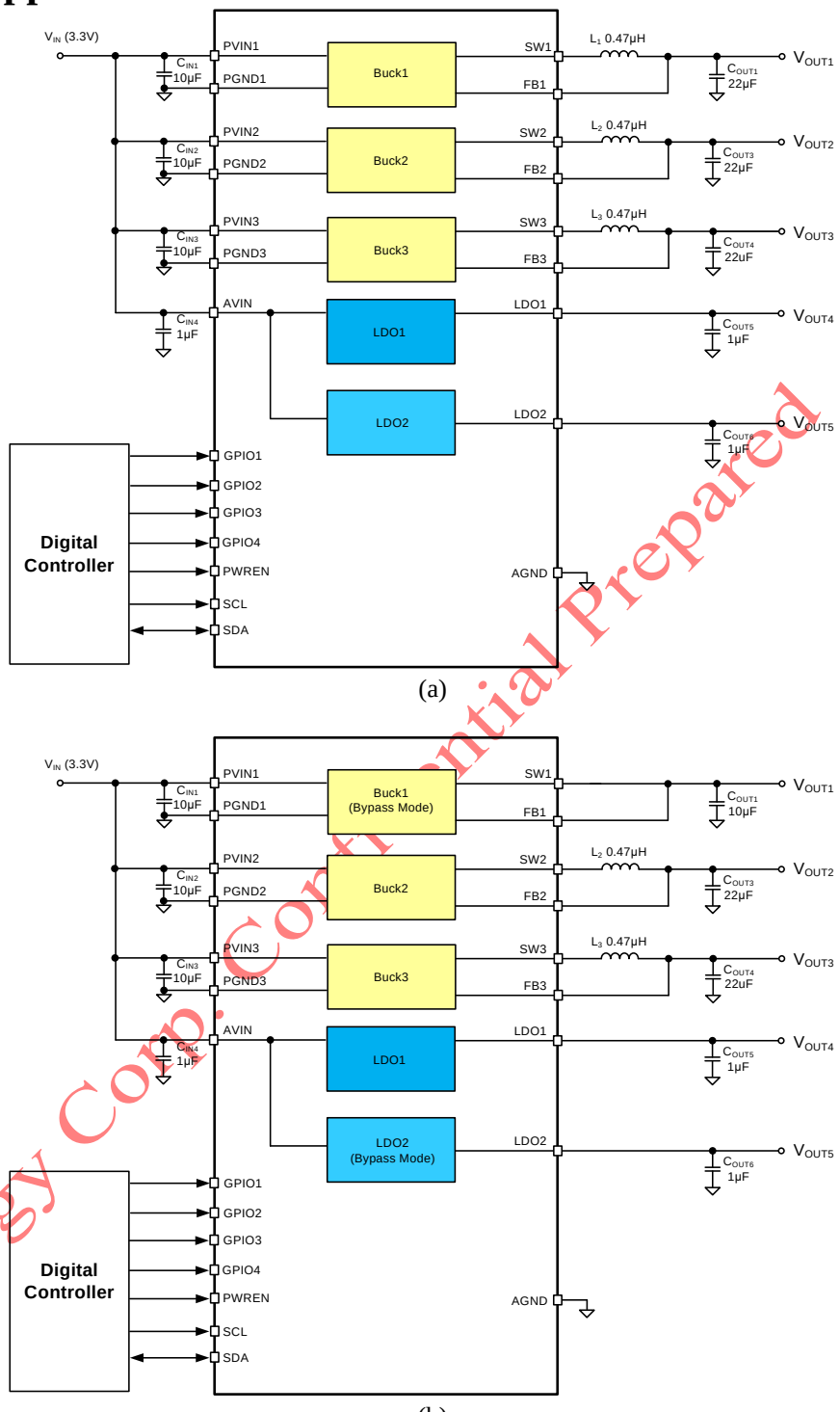


Figure 4. Application Circuit:
(a) Bcuk1: Buck mode, LDO2: LDO mode,
(b) Bcuk1: Bypass mode, LDO2: Bypass mode.

I²C Compatible Interface

The device integrates an I²C compatible interface. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 1MHz and uses standard I²C commands. The device always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.
The I²C interface is fully functional after VIN is above UVLO threshold.

I²C Interface Timing Diagram

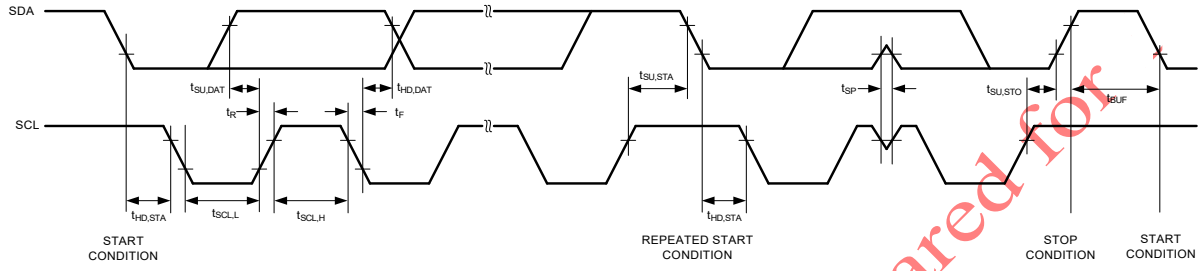


Figure 5. I²C Interface Timing Diagram

I²C Device Address

When communicating with multiple devices using the I²C interface, each device must have its own unique address so the host can distinguish between the devices. The PMIC slave address is <0100101x> where 'x' is the read/write control bit.

START and STOP Conditions

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.

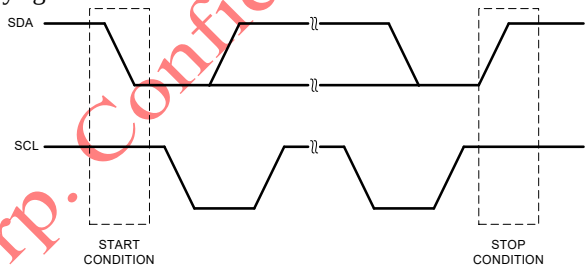


Figure 6. Start and Stop Conditions

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

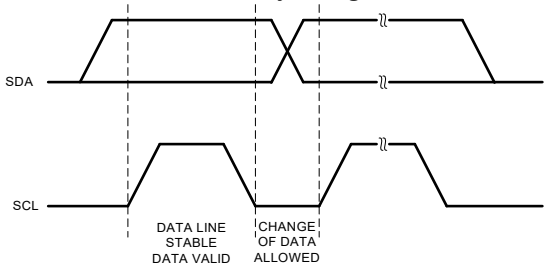


Figure 7. Data validity

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

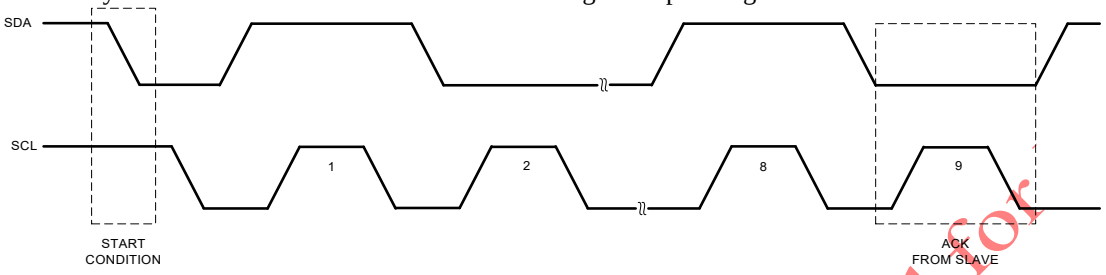


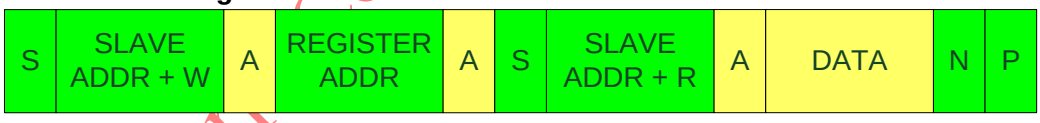
Figure 8. I²C Acknowledge

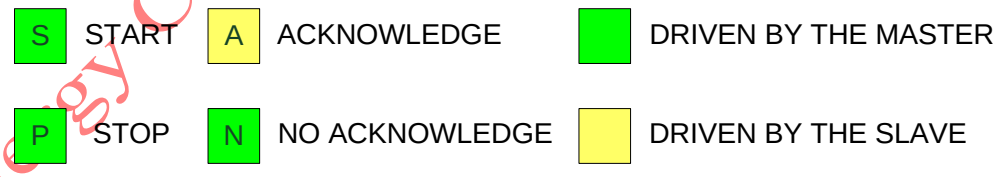
Data Transactions

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address (0100101x) followed by R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the device acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the device which register the master will write or read. Once the device receives a register address byte it will respond with an Acknowledge.

Write to a Register

Read from a Register





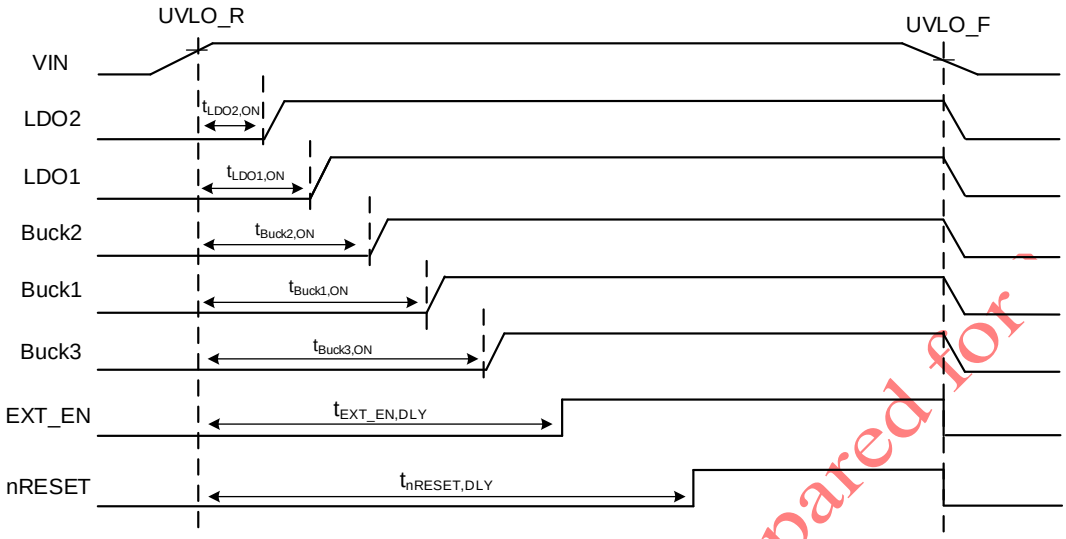
Description

1. Overview

	Output program range	Output Program Step	R_{DS_ON}		I_{OUT} MAX	HS current limit(fix)	Discharge Resistor	Startup Delay	Soft start time
			HS	LS					
Buck1 (Note)	0.6-1.5V	9.375mV	40mΩ	25mΩ	4.0A	5.1A	4.4Ω	0.5~8ms, 0.5ms/Step	0.5ms
	0.8-2.0V	12.5mV							
	2.1-3.3V	12.5mV							
Buck2 (Note)	0.6-1.5V	9.375mV	80mΩ	35mΩ	3.0A	4.2A	9.4Ω	0.5~8ms, 0.5ms/Step	0.5ms
	0.8-2.0V	12.5mV							
Buck3	1.0-3.3V	12.5mV	50mΩ	50mΩ	3.0A	4.2A	9.4Ω	0.5~8ms, 0.5ms/Step	0.5ms
LDO1	1.0-2.5V	12.5mV			0.3A	0.4A	50Ω	0.5~8ms, 0.5ms/Step	0.215ms
LDO2	1.6-3.3V	12.5mV			0.3A	0.4A	50Ω	0.5~8ms, 0.5ms/Step	0.215ms

Note: Output range is configured by vendor ONLY.

2. Power Sequence



Note: Delay time is configured by vendor ONLY, and shown in Table 3.

Figure 9. VIN power on/off Sequence

(1) When V_{IN} exceeds UVLO rising threshold, each channel will start up after the delay time. The power-on delay time can be set from 0.5ms to 8ms (0.5ms/Step) to provide different power sequence for customer, which is configured by vendor only. If V_{IN} is smaller than UVLO falling threshold, all channels will be turned off, immediately.

(2) nRESET and EXT_EN are open drain outputs; it is high impedance after the delay time when V_{IN} exceeds UVLO rising threshold. The delay time of nRESET can be set 4ms to 28ms (4ms/Step) and the delay time of EXT_EN can be set from 3ms to 9ms (2ms/Step), configuring by vendor only. The nRESET and EXT_EN will be pulled low immediately when any output is out of regulation and V_{IN} is lower than UVLO falling threshold. And, the nRESET stays high in sleep and deep sleep modes.

2.1 Under-Voltage Lockout (UVLO)

The UVLO is achieved by detecting VIN voltage. If the voltage of VIN pin exceeds $V_{IN,RISING}$ voltage(typ.=2.6V), all rails will start up after delay times which are listed below table. When VIN pin voltage is lower than $V_{IN,FALLING}$ voltage(typ.=2.5V), all rails are shut down after delay time. The UVLO hysteresis (typ.=0.1V) is designed to prevent shutdown caused by supply transients.

2.2 External Enable (EXT_EN)

The device provides an external power supply enable function, EXT_EN, configuring at GPIO2. It is used to control an external regulator to expand the power rail. If the voltage of VIN pin exceeds $V_{IN,RISING}$ voltage(typ.=2.6V), the EXT_EN will become high impedance after fixed delay. When VIN pin voltage is lower than $V_{IN,FALLING}$ voltage(typ.=2.5V) or fault occurs, the EXT_EN will go low, immediately.

2.3 nRESET

nRESET acts a power good indicator, which is an open drain output. This pin will become high impedance after fixed delay, when VIN higher than UVLO threshold. It will be pulled low immediately when any output goes out of regulation.

3. State Machine

The device contains six internal states. In the RESET state, the device is waiting for the input voltage on VIN to be within a valid range between VIN_UVLO and VIN OVP threshold. At this state, all regulators will be off. The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults will be presented. When entering the ACTIVE state from the RESET, THERMAL, OV/SCP fault, all regulators are powered on following their power up sequence.

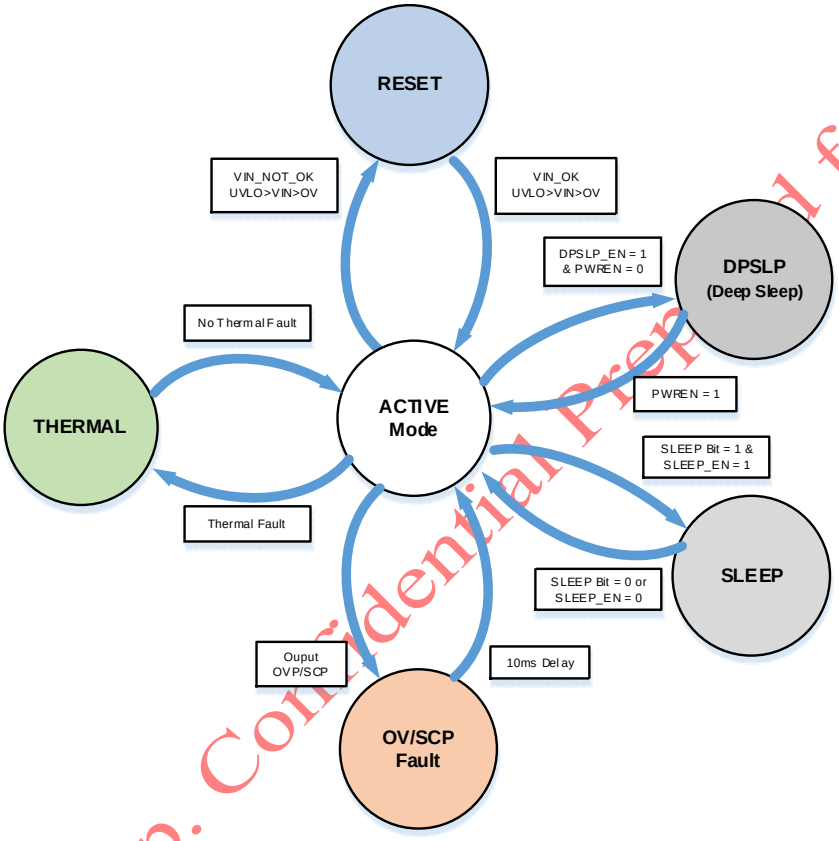


Figure 10. State Machine

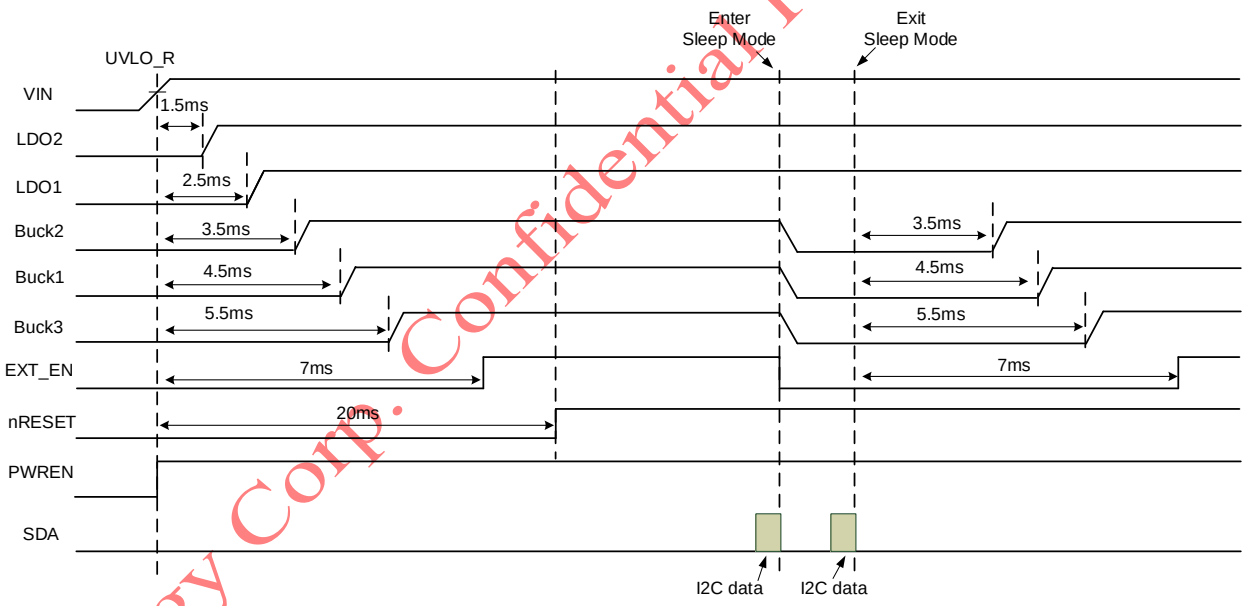
4. Sleep Mode State

Each output can be programmed to be on or off in the sleep state. The outputs will not follow any sequencing when they are turned off as they enter the sleep state. They will turn on with power up sequence when they exit the sleep state. Buck 1~3 and LDO1/2 can be programmed to turn off or keep on in the sleep state by I²C. The IC can enter SLEEP state via I²C registers SLEEP and SLEEP EN. Table 1 shows the conditions to enter SLEEP state.

I²C stays enabled in SLEEP state. The IC exits the SLEEP state when the conditions to enter SLEEP state are no longer present.

Table 1. Truth Table of SLEEP Mode Enter/exit

PWREN	0x15h[3]	0x15h[2]	Result
	SLEEP	SLEEP_EN	
x	0	0	Active Mode
x	1	0	Active Mode
x	0	1	Active Mode
x	1	1	Sleep Mode



Sleep mode setting: LDO1/2 ON, Buck1/2/3 OFF.

Figure 11. Conceptual of Sequence for Enter/exit Sleep Mode

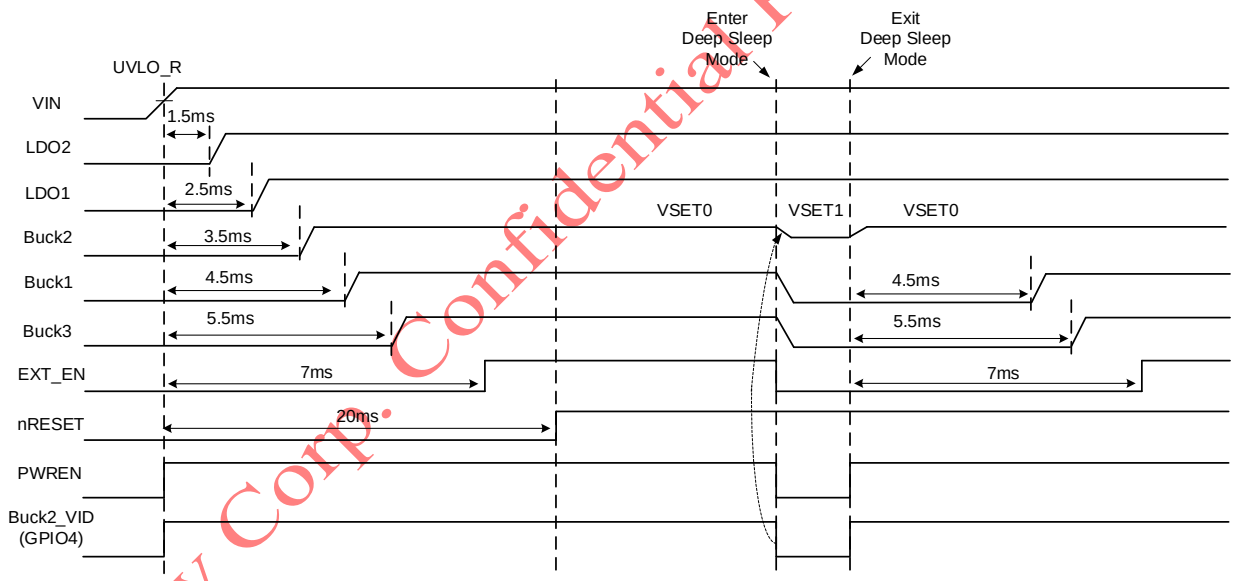
5. Deep Sleep (DPSLP) Mode State

The DPSLP state is another low power operating mode for the operating system. It is intended to be used in the lowest power configuration, comparing with SLEEP mode setting. It is similar to the SLEEP state, but DPSLP uses slightly different configurations to enter and exit this mode. Each output can be programmed to be off in the DPSLP state. This programming can be different, comparing with the SLEEP state. The outputs will not follow any sequencing when they are turned off as they enter the sleep state. They will turn on with power up sequence when they exit the DPSLP state.

This device can enter DPSLP state by PWREN pin. Table 2 shows the conditions to enter DPSLP state. I^2C interface is valid in DPSLP state. This device exits the DPSLP state when the conditions to enter DPSLP state are no longer present.

Table 2. Truth Table of DPSLP Mode Enter/exit

PWREN	0x15h[0] DPSLP_EN	Result
0	1	Deep Sleep Mode
1	1	Active Mode



Deep sleep mode setting: LDO1/2 ON, Buck2 ON, Buck1/3 OFF.

Figure 12. Conceptual of Sequence for Enter/exit Deep Sleep Mode

6. Protection Function

Protection		Mechanism
VIN Over Voltage Protection (VINOVP)		VIN_OV_SLE bit=1: When VIN rise above 3.9V, shutdown all. When VIN decreases to 3.6V, restart with power up sequence.
Over Temperature Protection (OTP)		When temperature exceeds 150°C, shutdown all. When temperature cool down to 135°C, restart following the power up sequence.
Output Over Voltage Protection (OVP)		>125% with 20µs deglitch time, shutdown all for 10ms then restart with power up sequence.
Output Short Circuit Protection (SCP)		<30% with 50µs deglitch time, shutdown all for 10ms then restart with power up sequence.
Over Current Protection (OCP)	Buckx	Inductor current peak current limit, and then keep regulation.
	LDO mode	Limit LDO current. If I_{out}=0.4A over 200us, the IC shuts down all for 10ms then restart with power up sequence.
	LDO2 bypass mode	Limit load switch current. If I_{out}=0.4A over 200us, the IC shuts down all for 10ms then restart with power up sequence.
	Buck1 bypass mode	Limit load switch current. If I_{out} = 5.1A over 200us, the IC shuts down all for 10ms then restart with power up sequence.

6.1 Output over Voltage and Short Circuit Protection

If anyone output occurs short or over voltage condition, this device will be shut down for 10ms then will restart with power up sequence. If the short or over voltage condition still exists in the ACTIVE state, this device will be shut down again for 10ms then restart, until the fault condition is removed.

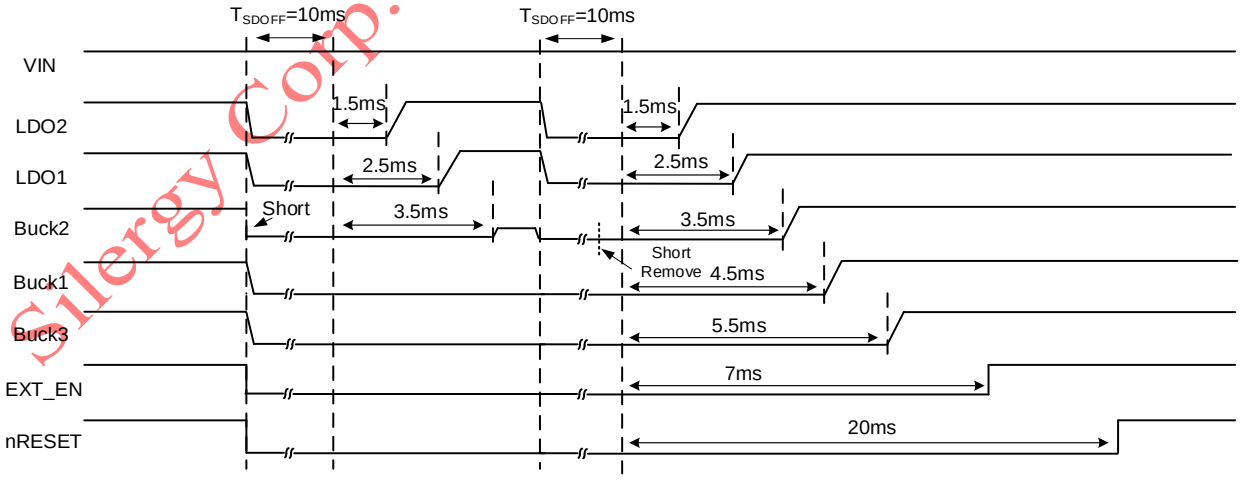


Figure 13. Conceptual of Buck2 Occurring Output Short Circuit Event in Active Mode

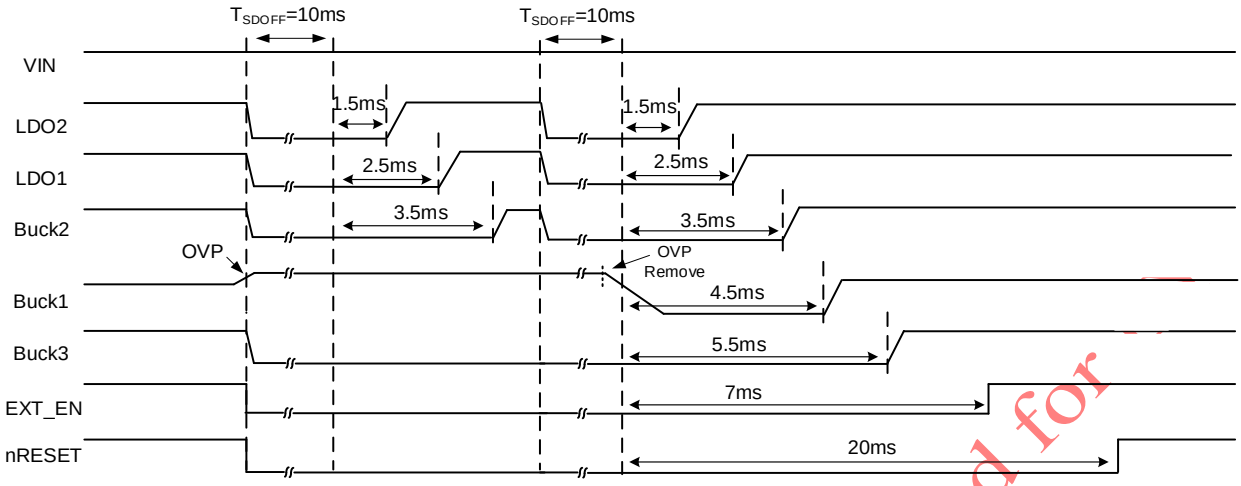


Figure 14. Conceptual of Buck1 Occurring Output over Voltage Event in Active Mode

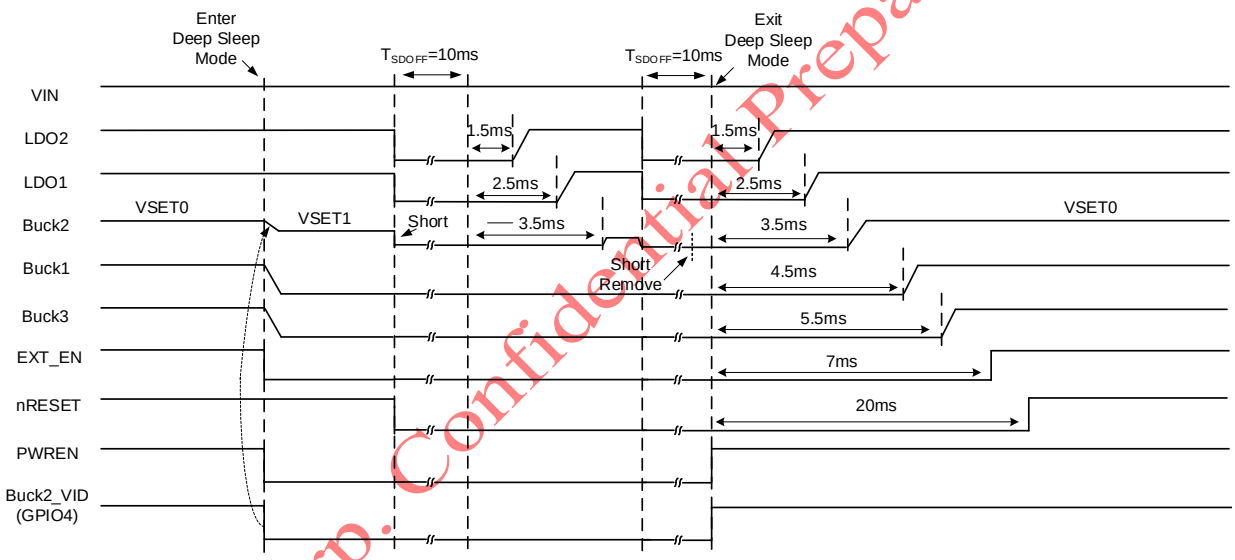


Figure 15. Conceptual of Buck2 Occurring Output Short Circuit Event in Deep Sleep Mode

6.2 Input over Voltage Protection

VIN OVP threshold is 3.9V. When VIN exceeds 3.9V, all channels will be turned off. The OVP hysteresis is 0.3V. When VIN decreases to 3.6V, all channels will restart follow power on sequence.

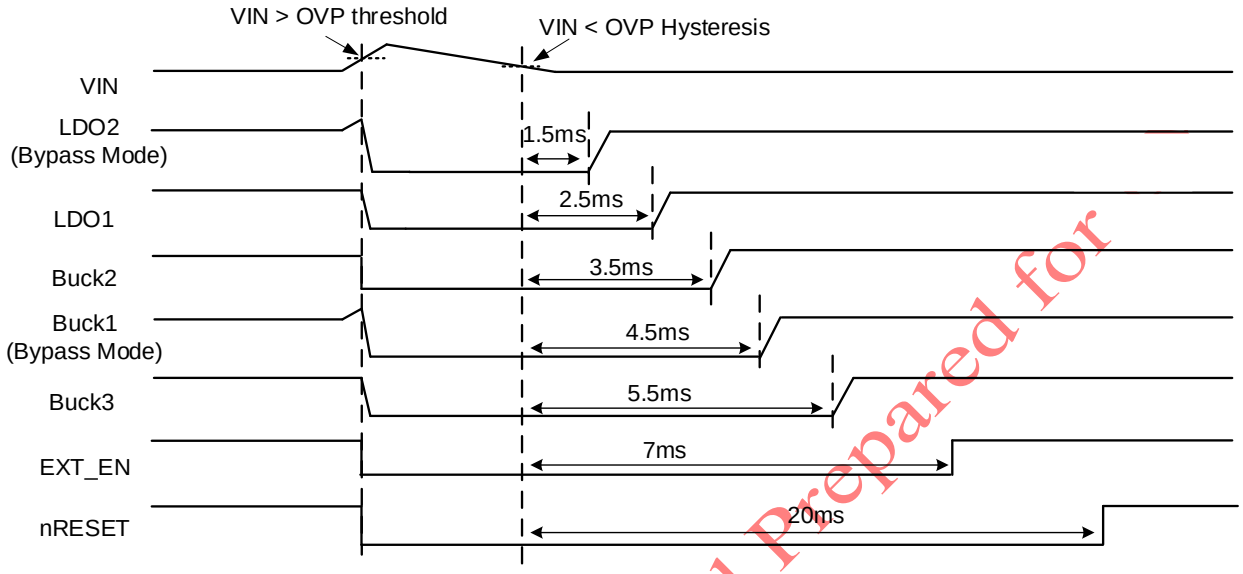


Figure 16. Conceptual of Input over Voltage Protection Mechanism

6.3 Output Current Limit

The Buck converter limits the HS switch current and LS switch current in each switching cycle. Potentially, this protection mechanism creates a short circuit scenario to shut down the device. That is, this device will turn off all supplies off for 10ms then restart with sequence in periodically, if fault event not removing.

For LDO, when the output current reaches the current limit threshold, the LDO will limit the output current. If current limit loop functions for 200µs or short circuit is detected, the device will be shut down for 10ms then restart with sequence in periodically, if fault event not removing.

For buck1 acts being load switch in by pass mode, when the output current exceeds 5.1A, the device will limit the current. If current limit loop functions for 200µs the device will be shut down for 10ms then restart with sequence in periodically, if fault event not removing.

6.4 Thermal Shutdown

A thermal shutdown is implemented to prevent damage, because of excessive heat and power dissipation. Once the junction temperature exceeds 150°C, the device will be shut down. When the temperature decreases to 135°C the device will automatically restart to perform the start-up sequence with the same voltages and programming as it has been programmed before the thermal shutdown.

Register Address Map

Address	D7	D6	D5	D4	D3	D2	D1	D0
0x03h	TRST_DLY			x	x	x	x	x
0x04h	x	ENB1BYP MODE	x	x	x	x	DIS OVUV SHDN	x
0x09h	x	x	DIS_OTP	x	x	x	x	x
0x0Eh	x	x	x	Reserved	x	x	x	x
0x15h	x	x	x	x	SLEEP	SLEEP EN	x	DPSLP EN
0x32h	B1_VSET0	B1_VSET0						
0x33h	B1_VSET1	B1_VSET1						
0x34h	B1_ON	x	x	B1_SLEEP_ EN	x	B1_DP_ SLEEP_EN	x	B1_FOR-CEPWM
0x42h	Reserved	B2_VSET0						
0x43h	Reserved	B2_VSET1						
0x44h	B2_ON	x	x	B2_SLEEP_ EN	x	B2_DP_ SLEEP_EN	x	B2_FOR-CEPWM
0x52h	B3_VSET0							
0x53h	B3_VSET1							
0x54h	B3_ON	x	x	B3_SLEEP_ EN	x	B3_DP_ SLEEP_EN	x	B3_FOR-CEPWM
0xA1h	LDO1_VSET							
0xA2h	LDO1_ON	x	x	LDO1_ SLEEP_EN	LDO1_DP_ SLEEP_EN	x	x	x
0xA7h	LDO2_VSET							
0xA8h	LDO2_ON	x	x	LDO2_ SLEEP_EN	LDO2_DP_ SLEEP_EN	x	x	X
0xADh	x	x	x	x	x	x	LDO2_ILIM _SHUT-DOWN_DIS	LDO1_ILIM_ SHUT-DOWN_DIS
0xECh	x	x	x	LDO2_LSW _MODE	x	x	x	x

Note 1: x means don't care for application
Note 2: Summary for Read ONLY (RO) bit

- Bit 5~7(TRST_DLY) @0x03h
- Bit 6(ENB1BYP MODE) @ 0x04h
- Bit 7(B1_VSET0) @ 0x32h
- Bit 7(B1_VSET1) @ 0x33h
- Bit 4(LDO2_LSW_MODE) @ 0xECh
- Including reserved bits

Note 3: Except bits listed in Note 2, others are Read/Write (R/W) bit

Configuration Parameter

Table 3. Configuration for Architecture & Output Range

Rail	Output Program Range	Output Program Step	Default Output Voltage	Startup Delay	Soft Start Time
Buck1	2.1-3.3V	12.5mV	VSET0=2.5V (A0h) VSET1=2.5V (A0h)	$t_{Buck1,ON}$=1.0ms	0.5ms
Buck2	0.6-1.5V	9.375mV	VSET0=0.9V (20h) VSET1=0.75V (10h)	$t_{Buck2,ON}$=1.0ms	0.5ms
Buck3	1.0-3.3V	12.5mV	VSET0=1.8V (50h) VSET1=1.2V (20h)	$t_{Buck3,ON}$=2.0ms	0.5ms
LDO1	1.0-2.5V	12.5mV	1.8V	$t_{LDO1,ON}$=0.5ms	0.215ms
LDO2	Bypass mode			$t_{LDO2,ON}$=0.5ms	0.215ms

Table 4. Configuration for GPIO Function

GPIO	Setting
GPIO1	nRESET, 12ms delay time
GPIO2	Buck1 Bypass/Buck Mode Select High: Bypass Mode Vout=Vin Low: Buck Mode Vout=2.5V
GPIO3	Buck3_VID: High: VSET0 Low: VSET1
GPIO4	Buck2_VID: High: VSET0 Low: VSET1

Table 5. Default State of Power Rails in Deep Sleep/Sleep Mode

Rail	Sleep Mode	Deep Sleep Mode
Buck1	OFF	OFF
Buck2	ON	ON
Buck3	OFF	OFF
LDO1	ON	ON
LDO2	ON	ON

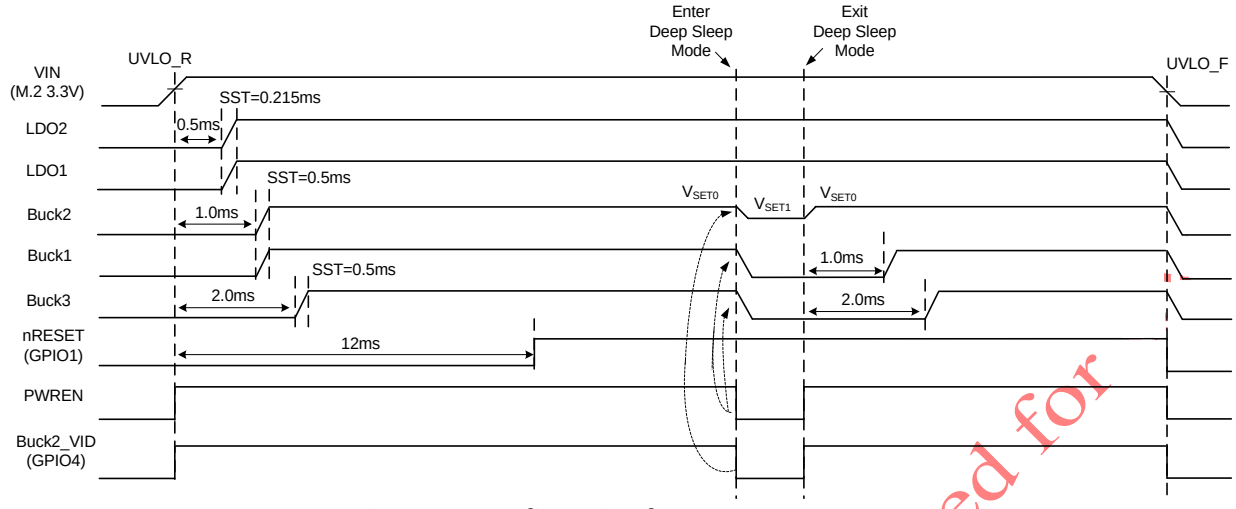


Figure 17. Configuration for Power Sequence.

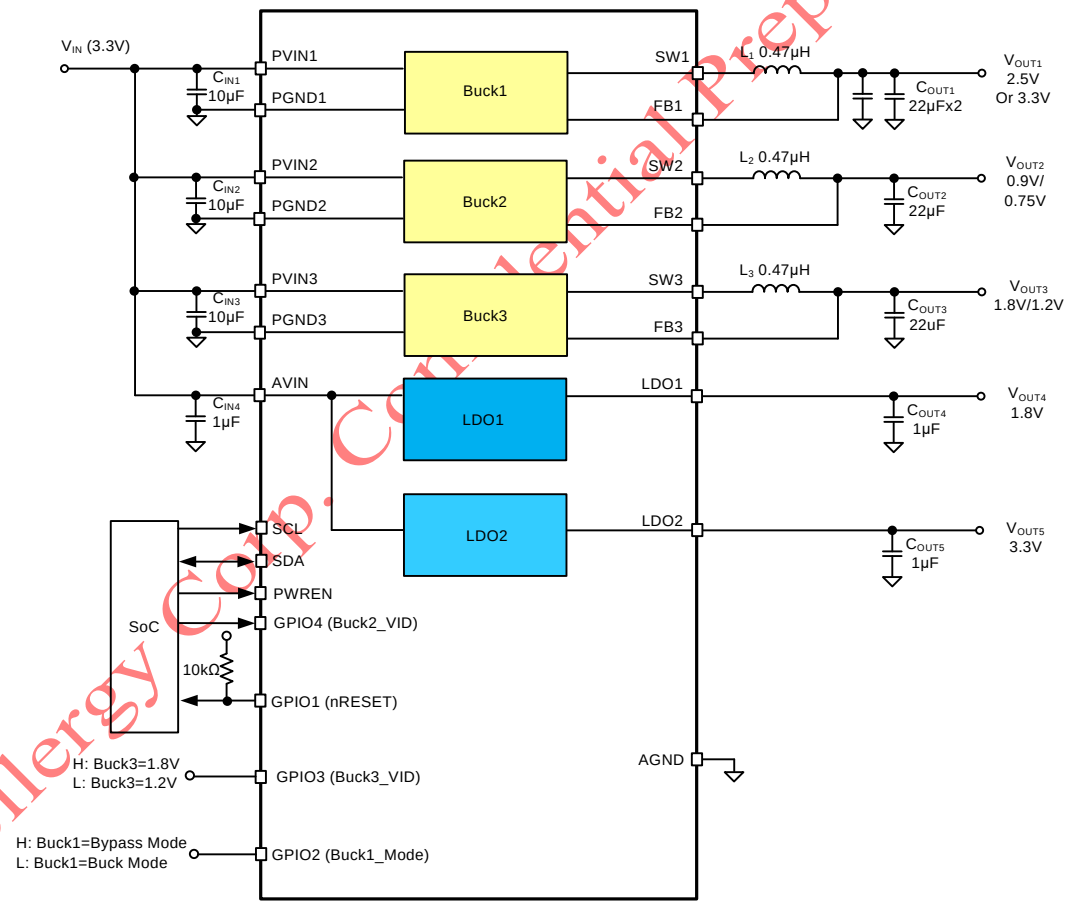


Figure 18. Application Circuit

Register Address Map

Address	Bit	Default (Binary)	Type	Range	Resolution
0x03h	TRST_DLY [7:5]	011b	RO	001: 4ms, 010: 8ms, 011: 12ms, 100: 16ms, 101: 20ms, 110, 24ms, 111, 28ms	-
0x04h	ENB1BYP MODE [6]	0b	RO	0 – Disable Buck 1 Bypass Mode 1 – Enable Buck 1 Bypass Mode	-
	DISOVUV SHDN [1]	0b	R/W	0 – Enable hiccup mode or OVUVFLT state in ACTIVE Mode 1 – Disable hiccup mode or OVUVFLT state in ACTIVE Mode	-
0x09h	DIS_OTP [5]	0b	R/W	0 – Enable OTP 1 – Disable OTP	-
0x0Eh	Reserved	-	-		-
0x15h	SLEEP [3]	0b	R/W	0 – PMIC operates in power on state 1 – PMIC enters into SLEEP state	-
	SLEEP_EN [2]	0b	R/W	0 – SLEEP Mode is disabled 1 – SLEEP Mode is enabled	-
	DPSLP_EN [0]	1b	R/W	0 – DPSLP Mode is disabled 1 – DPSLP Mode is enabled	-
0x32h	B1_VSET0 [7]	1b	RO	2.1V-3.3V	12.5mV
	B1_VSET0 [6:0]	0100000b	R/W		
0x33h	B1_VSET1 [7]	1b	RO	2.1V-3.3V	12.5mV
	B1_VSET1 [6:0]	0100000b	R/W		
0x34h	B1_ON [7]	1b	R/W	0 – Buck1 Disable. 1 – Buck1 Enable.	-
	B1_SLEEP_EN [4]	1b	R/W	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	-
	B1_DP_SLEEP_EN [2]	1b	R/W	0 – Buck1 stays on when the IC enters Deep Sleep mode 1 – Buck1 turns off when the IC enters Deep Sleep mode	-
	B1_FORCEPWM [0]	0b	R/W	0 – Buck1 enters LPM at light load 1 – Buck1 forced into PWM at light load	-

Address	Bit	Default (Binary)	Type	Range	Resolution
0x42h	B2_VSET0 [6:0]	0100000b	R/W	0.6V-1.5V	9.375mV
0x43h	B2_VSET1 [6:0]	0010000b	R/W	0.6V-1.5V	9.375mV
0x44h	B2_ON [7]	1b	R/W	0 – Buck2 Disable. 1 – Buck2 Enable.	-
	B2_SLEEP_EN [4]	0b	R/W	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	-
	B2_DP_SLEEP_EN [2]	0b	R/W	0 – Buck2 stays on when the IC enters Deep Sleep mode 1 – Buck2 turns off when the IC enters Deep Sleep mode	-
	B2_FORCEPWM [0]	0b	R/W	0 – Buck2 enters LPM at light load 1 – Buck2 forced into PWM at light load	-
0x52h	B3_VSET0 [7:0]	01010000b	R/W	1V-3.3V	12.5mV
0x53h	B3_VSET1 [7:0]	00100000b	R/W	1V-3.3V	12.5mV
0x54h	B3_ON [7]	1b	R/W	0 – Buck3 Disable. 1 – Buck3 Enable.	-
	B3_SLEEP_EN [4]	1b	R/W	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	-
	B3_DP_SLEEP_EN [2]	1b	R/W	0 – Buck3 stays on when the IC enters Deep Sleep mode 1 – Buck3 turns off when the IC enters Deep Sleep mode	-
	B3_FORCEPWM [0]	0b	R/W	0 – Buck3 enters LPM at light load 1 – Buck3 forced into PWM at light load	-
0xA1h	LDO1_VSET [7:0]	01010000b	R/W	1V-2.5V	12.5mV
0xA2h	LDO1_ON [7]	1b	R/W	0 – LDO1 Disable. 1 – LDO1 Enable.	-
	LDO1_SLEEP_EN [4]	0b	R/W	0 – LDO1 stays on when the IC enters Sleep mode 1 – LDO1 turns off when the IC enters Sleep mode	-
	LDO1_DP_SLEEP_EN [3]	0b	R/W	0 – LDO1 stays on when the IC enters Deep Sleep mode 1 – LDO1 turns off when the IC enters Deep Sleep mode	-

Address	Bit	Default (Binary)	Type	Range	Resolution
0xA7h	LDO2_VSET [7:0]	00000000b	R/W	1.6V-3.3V	12.5mV
0xA8h	LDO2_ON [7]	1b	R/W	0 – LDO2 Disable. 1 – LDO2 Enable.	-
	LDO2_SLEEP_EN [4]	0b	R/W	0 – LDO2 stays on when the IC enters Sleep mode 1 – LDO2 turns off when the IC enters Sleep mode	-
	LDO2_DP_SLEEP_EN [3]	0b	R/W	0 – LDO2 stays on when the IC enters Deep Sleep mode 1 – LDO2 turns off when the IC enters Deep Sleep mode	-
0xADh	LDO2_ILIM_SHUT-DOWN_DIS [1]	0b	R/W	0 – Shut down LDO2 after current limit 1 – Disable LDO2 Shut down function after current limit	-
	LDO1_ILIM_SHUT-DOWN_DIS [0]	0b	R/W	0 – Shut down LDO1 after current limit 1 – Disable LDO1 Shut down function after current limit	-
0xECh	LDO2_LSW_MODE [4]	1b	RO	0 – LDO2 operates as LDO 1 – LDO2 operates as a load switch	-

nRESET Delay Time Adjustment

Address – 0x03h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TRST_DLY			x	x	x	x	x
READ/WRITE	RO	RO	RO	R/W	R/W	R/W	R/W	R/W

Description: Set nRESET Delay Time [7:5]. Configuration by vendor ONLY.

Code	Delay Time
001h	4ms
010h	8ms
011h	12ms
100h	16ms
101h	20ms
110h	24ms
111h	28ms

Buck1 Operating Mode and OVUV Fault Adjustment

Address – 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	x	ENB1BYP MODE	x	x	x	x	DISOVUV SHDN	x
READ/WRITE	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W

Description: Set Buck1 Buck or Bypass Mode [6]. Configuration by vendor ONLY.

Code	Buck1 Bypass Mode
00h	Disable
01h	Enable

Set OVUV Fault [1]

Code	UVUV Fault
00h	Enable hiccup mode or OVUVFLT state.
01h	Disable hiccup mode or OVUVFLT state

OTP Adjustment

Address – 0x09h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	x	x	DIS_OTP	x	x	x	x	x
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description: Set OTP [5]

Code	OTP
00h	Enable
01h	Disable

VIN OVP Adjustment

Address – 0x0Eh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	x	x	x	Reserved	x	x	x	x
READ/WRITE	R/W	R/W	R/W	RO	R/W	R/W	R/W	R/W

Description	Reserved [5] Reserved bit for function expansion.

Sleep Mode and Deep Sleep Mode Adjustment

Address – 0x15h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	x	x	x	x	SLEEP	SLEEP_EN	x	DPSLP_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Sleep Mode [3]

Code	Sleep Mode
00h	PMIC operates in power on state
01h	PMIC enters into Sleep state

Set Sleep Mode EN[2]

Code	Sleep EN
00h	Sleep mode is disable
01h	Sleep mode is enable

Set Deep Sleep Mode EN [0]

Code	Deep Sleep EN
00h	Deep sleep mode is disable
01h	Deep sleep mode is enable

Buck1 Output Voltage VSET0 Adjustment

Address – 0x32h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B1_VSET0							
READ/WRITE	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Output Voltage VSET0 [7:0]

If B1_VSET0[7]=1, the output voltage is equal to B1_VSET0*0.0125+0.5V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
80h	2.1V	A0h	2.5V	C0h	2.9V	E0h	3.3V
81h	2.1125V	A1h	2.5125V	C1h	2.9125V	E1h	3.3V
82h	2.125V	A2h	2.525V	C2h	2.925V	E2h	3.3V
83h	2.1375V	A3h	2.5375V	C3h	2.9375V	E3h	3.3V
84h	2.15V	A4h	2.55V	C4h	2.95V	E4h	3.3V
85h	2.1625V	A5h	2.5625V	C5h	2.9625V	E5h	3.3V
86h	2.175V	A6h	2.575V	C6h	2.975V	E6h	3.3V
87h	2.1875V	A7h	2.5875V	C7h	2.9875V	E7h	3.3V
88h	2.2V	A8h	2.6V	C8h	3V	E8h	3.3V
89h	2.2125V	A9h	2.6125V	C9h	3.0125V	E9h	3.3V
8Ah	2.225V	AAh	2.625V	CAh	3.025V	EAh	3.3V
8Bh	2.2375V	ABh	2.6375V	CBh	3.0375V	EBh	3.3V
8Ch	2.25V	ACh	2.65V	CCh	3.05V	ECh	3.3V
8Dh	2.2625V	ADh	2.6625V	CDh	3.0625V	EDh	3.3V
8Eh	2.275V	AEh	2.675V	CEh	3.075V	EEh	3.3V
8Fh	2.2875V	AFh	2.6875V	CFh	3.0875V	EFh	3.3V
90h	2.3V	B0h	2.7V	D0h	3.1V	F0h	3.3V
91h	2.3125V	B1h	2.7125V	D1h	3.1125V	F1h	3.3V
92h	2.325V	B2h	2.725V	D2h	3.125V	F2h	3.3V
93h	2.3375V	B3h	2.7375V	D3h	3.1375V	F3h	3.3V
94h	2.35V	B4h	2.75V	D4h	3.15V	F4h	3.3V
95h	2.3625V	B5h	2.7625V	D5h	3.1625V	F5h	3.3V
96h	2.375V	B6h	2.775V	D6h	3.175V	F6h	3.3V
97h	2.3875V	B7h	2.7875V	D7h	3.1875V	F7h	3.3V
98h	2.4V	B8h	2.8V	D8h	3.2V	F8h	3.3V
99h	2.4125V	B9h	2.8125V	D9h	3.2125V	F9h	3.3V
9Ah	2.425V	BAh	2.825V	DAh	3.225V	FAh	3.3V
9Bh	2.4375V	BBh	2.8375V	DBh	3.2375V	FBh	3.3V
9Ch	2.45V	BCh	2.85V	DCh	3.25V	FCh	3.3V
9Dh	2.4625V	BDh	2.8625V	DDh	3.2625V	FDh	3.3V
9Eh	2.475V	BEh	2.875V	DEh	3.275V	FEh	3.3V
9Fh	2.4875V	BFh	2.8875V	DFh	3.2875V	FFh	3.3V

Buck1 Output Voltage VSET1 Adjustment

Address – 0x33h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B1_VSET1							
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Output Voltage VSET1 [7:0]

If B1_VSET1[7]=1, the output voltage is equal to B1_VSET1*0.0125+0.5V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
80h	2.1V	A0h	2.5V	C0h	2.9V	E0h	3.3V
81h	2.1125V	A1h	2.5125V	C1h	2.9125V	E1h	3.3V
82h	2.125V	A2h	2.525V	C2h	2.925V	E2h	3.3V
83h	2.1375V	A3h	2.5375V	C3h	2.9375V	E3h	3.3V
84h	2.15V	A4h	2.55V	C4h	2.95V	E4h	3.3V
85h	2.1625V	A5h	2.5625V	C5h	2.9625V	E5h	3.3V
86h	2.175V	A6h	2.575V	C6h	2.975V	E6h	3.3V
87h	2.1875V	A7h	2.5875V	C7h	2.9875V	E7h	3.3V
88h	2.2V	A8h	2.6V	C8h	3V	E8h	3.3V
89h	2.2125V	A9h	2.6125V	C9h	3.0125V	E9h	3.3V
8Ah	2.225V	AAh	2.625V	CAh	3.025V	EAh	3.3V
8Bh	2.2375V	ABh	2.6375V	CBh	3.0375V	EBh	3.3V
8Ch	2.25V	ACh	2.65V	CCh	3.05V	ECh	3.3V
8Dh	2.2625V	ADh	2.6625V	CDh	3.0625V	EDh	3.3V
8Eh	2.275V	AEh	2.675V	CEh	3.075V	EEh	3.3V
8Fh	2.2875V	AFh	2.6875V	CFh	3.0875V	EFh	3.3V
90h	2.3V	B0h	2.7V	D0h	3.1V	F0h	3.3V
91h	2.3125V	B1h	2.7125V	D1h	3.1125V	F1h	3.3V
92h	2.325V	B2h	2.725V	D2h	3.125V	F2h	3.3V
93h	2.3375V	B3h	2.7375V	D3h	3.1375V	F3h	3.3V
94h	2.35V	B4h	2.75V	D4h	3.15V	F4h	3.3V
95h	2.3625V	B5h	2.7625V	D5h	3.1625V	F5h	3.3V
96h	2.375V	B6h	2.775V	D6h	3.175V	F6h	3.3V
97h	2.3875V	B7h	2.7875V	D7h	3.1875V	F7h	3.3V
98h	2.4V	B8h	2.8V	D8h	3.2V	F8h	3.3V
99h	2.4125V	B9h	2.8125V	D9h	3.2125V	F9h	3.3V
9Ah	2.425V	BAh	2.825V	DAh	3.225V	FAh	3.3V
9Bh	2.4375V	BBh	2.8375V	DBh	3.2375V	FBh	3.3V
9Ch	2.45V	BCh	2.85V	DCh	3.25V	FCh	3.3V
9Dh	2.4625V	BDh	2.8625V	DDh	3.2625V	FDh	3.3V
9Eh	2.475V	BEh	2.875V	DEh	3.275V	FEh	3.3V
9Fh	2.4875V	BFh	2.8875V	DFh	3.2875V	FFh	3.3V

Buck1 Config Adjustment

Address – 0x34h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B1_ON	x	x	B1_SLEEP_EN	x	B1_DP_SLEEP_EN	x	B1_FORCEPWM
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Enable/Disable [7]

Code	Buck1 ON/OFF
00h	Buck1 is disable
01h	Buck1 is enable

Set Buck1 ON/OFF in Sleep Mode [4]

Code	Buck1 ON/OFF in Sleep Mode
00h	Buck1 stays on when IC enters sleep mode
01h	Buck1 turns off when IC enters sleep mode

Set Buck1 ON/OFF in Deep Sleep Mode [2]

Code	Buck1 ON/OFF in Deep Sleep Mode
00h	Buck1 stays on when IC enters deep sleep mode
01h	Buck1 turns off when IC enters deep sleep mode

Set Buck1 LPM/FCCM [0]

Code	Buck1 LPM/FCCM Selection
00h	Buck1 enters LPM at light load
01h	Buck1 forced into PWM at light load

Buck2 Output Voltage VSET0 Adjustment

Address – 0x42h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Reserved	B2_VSET0						
READ/WRITE	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck2 Output Voltage VSET0 [6:0]

The output voltage is equal to B2_VSET0*0.009375+0.6V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.6000V	1Ah	0.8438V	34h	1.0875V	4Eh	1.3313V
01h	0.6094V	1Bh	0.8531V	35h	1.0969V	4Fh	1.3406V
02h	0.6188V	1Ch	0.8625V	36h	1.1063V	50h	1.3500V
03h	0.6281V	1Dh	0.8719V	37h	1.1156V	51h	1.3594V
04h	0.6375V	1Eh	0.8813V	38h	1.1250V	52h	1.3688V
05h	0.6469V	1Fh	0.8906V	39h	1.1344V	53h	1.3781V
06h	0.6563V	20h	0.9000V	3Ah	1.1438V	54h	1.3875V
07h	0.6656V	21h	0.9094V	3Bh	1.1531V	55h	1.3969V
08h	0.6750V	22h	0.9188V	3Ch	1.1625V	56h	1.4063V
09h	0.6844V	23h	0.9281V	3Dh	1.1719V	57h	1.4156V
0Ah	0.6938V	24h	0.9375V	3Eh	1.1813V	58h	1.4250V
0Bh	0.7031V	25h	0.9469V	3Fh	1.1906V	59h	1.4344V
0Ch	0.7125V	26h	0.9563V	40h	1.2000V	5Ah	1.4438V
0Dh	0.7219V	27h	0.9656V	41h	1.2094V	5Bh	1.4531V
0Eh	0.7313V	28h	0.9750V	42h	1.2188V	5Ch	1.4625V
0Fh	0.7406V	29h	0.9844V	43h	1.2281V	5Dh	1.4719V
10h	0.7500V	2Ah	0.9938V	44h	1.2375V	5Eh	1.4813V
11h	0.7594V	2Bh	1.0031V	45h	1.2469V	5Fh	1.4906V
12h	0.7688V	2Ch	1.0125V	46h	1.2563V	60h	1.5000V
13h	0.7781V	2Dh	1.0219V	47h	1.2656V	61h	1.5000V
14h	0.7875V	2Eh	1.0313V	48h	1.2750V	62h	1.5000V
15h	0.7969V	2Fh	1.0406V	49h	1.2844V	63h	1.5000V
16h	0.8063V	30h	1.0500 V	4Ah	1.2938V	64h	1.5000V
17h	0.8156V	31h	1.0594V	4Bh	1.3031V	65h	1.5000V
18h	0.8250V	32h	1.0688V	4Ch	1.3125V	…	…
19h	0.8344V	33h	1.0781V	4Dh	1.3219V	7Fh	1.5000V

Buck2 Output Voltage VSET1 Adjustment

Address – 0x43h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Reserved	B2_VSET1						
READ/WRITE	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck2 Output Voltage VSET1 [6:0]

The output voltage is equal to B2_VSET1*0.009375+0.6V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.6000V	1Ah	0.8438V	34h	1.0875V	4Eh	1.3313V
01h	0.6094V	1Bh	0.8531V	35h	1.0969V	4Fh	1.3406V
02h	0.6188V	1Ch	0.8625V	36h	1.1063V	50h	1.3500V
03h	0.6281V	1Dh	0.8719V	37h	1.1156V	51h	1.3594V
04h	0.6375V	1Eh	0.8813V	38h	1.1250V	52h	1.3688V
05h	0.6469V	1Fh	0.8906V	39h	1.1344V	53h	1.3781V
06h	0.6563V	20h	0.9000V	3Ah	1.1438V	54h	1.3875V
07h	0.6656V	21h	0.9094V	3Bh	1.1531V	55h	1.3969V
08h	0.6750V	22h	0.9188V	3Ch	1.1625V	56h	1.4063V
09h	0.6844V	23h	0.9281V	3Dh	1.1719V	57h	1.4156V
0Ah	0.6938V	24h	0.9375V	3Eh	1.1813V	58h	1.4250V
0Bh	0.7031V	25h	0.9469V	3Fh	1.1906V	59h	1.4344V
0Ch	0.7125V	26h	0.9563V	40h	1.2000V	5Ah	1.4438V
0Dh	0.7219V	27h	0.9656V	41h	1.2094V	5Bh	1.4531V
0Eh	0.7313V	28h	0.9750V	42h	1.2188V	5Ch	1.4625V
0Fh	0.7406V	29h	0.9844V	43h	1.2281V	5Dh	1.4719V
10h	0.7500V	2Ah	0.9938V	44h	1.2375V	5Eh	1.4813V
11h	0.7594V	2Bh	1.0031V	45h	1.2469V	5Fh	1.4906V
12h	0.7688V	2Ch	1.0125V	46h	1.2563V	60h	1.5000V
13h	0.7781V	2Dh	1.0219V	47h	1.2656V	61h	1.5000V
14h	0.7875V	2Eh	1.0313V	48h	1.2750V	62h	1.5000V
15h	0.7969V	2Fh	1.0406V	49h	1.2844V	63h	1.5000V
16h	0.8063V	30h	1.0500 V	4Ah	1.2938V	64h	1.5000V
17h	0.8156V	31h	1.0594V	4Bh	1.3031V	65h	1.5000V
18h	0.8250V	32h	1.0688V	4Ch	1.3125V	…	…
19h	0.8344V	33h	1.0781V	4Dh	1.3219V	7Fh	1.5000V

Buck2 Config Adjustment

Address – 0x44h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B2_ON	x	x	B2_SLEEP_EN	x	B2_DP_SLEEP_EN	x	B2_FORCEPWM
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck2 Enable/Disable [7]

Code	Buck2 ON/OFF
00h	Buck2 is disable
01h	Buck2 is enable

Set Buck2 ON/OFF in Sleep Mode [4]

Code	Buck2 ON/OFF in Sleep Mode
00h	Buck2 stays on when IC enters sleep mode
01h	Buck2 turns off when IC enters sleep mode

Set Buck2 ON/OFF in Deep Sleep Mode [2]

Code	Buck2 ON/OFF in Deep Sleep Mode
00h	Buck2 stays on when IC enters deep sleep mode
01h	Buck2 turns off when IC enters deep sleep mode

Set Buck2 LPM/FCCM [0]

Code	Buck2 LPM/FCCM Selection
00h	Buck2 enters LPM at light load
01h	Buck2 forced into PWM at light load

Buck3 Output Voltage VSET0 Adjustment

Address – 0x52h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B3_VSET0							
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck3 Output Voltage VSET0 [7:0]

The output voltage is equal to B3_VSET0*0.0125+0.8V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	1.0000V	1Ah	1.1250V	34h	1.4500V	4Eh	1.7750V	68h	2.1000V
01h	1.0000V	1Bh	1.1375V	35h	1.4625V	4Fh	1.7875V	69h	2.1125V
02h	1.0000V	1Ch	1.1500V	36h	1.4750V	50h	1.8000V	6Ah	2.1250V
03h	1.0000V	1Dh	1.1625V	37h	1.4875V	51h	1.8125V	6Bh	2.1375V
04h	1.0000V	1Eh	1.1750V	38h	1.5000V	52h	1.8250V	6Ch	2.1500V
05h	1.0000V	1Fh	1.1875V	39h	1.5125V	53h	1.8375V	6Dh	2.1625V
06h	1.0000V	20h	1.2000V	3Ah	1.5250V	54h	1.8500V	6Eh	2.1750V
07h	1.0000V	21h	1.2125V	3Bh	1.5375V	55h	1.8625V	6Fh	2.1875V
08h	1.0000V	22h	1.2250V	3Ch	1.5500V	56h	1.8750V	70h	2.2000V
09h	1.0000V	23h	1.2375V	3Dh	1.5625V	57h	1.8875V	71h	2.2125V
0Ah	1.0000V	24h	1.2500V	3Eh	1.5750V	58h	1.9000V	72h	2.2250V
0Bh	1.0000V	25h	1.2625V	3Fh	1.5875V	59h	1.9125V	73h	2.2375V
0Ch	1.0000V	26h	1.2750V	40h	1.6000V	5Ah	1.9250V	74h	2.2500V
0Dh	1.0000V	27h	1.2875V	41h	1.6125V	5Bh	1.9375V	75h	2.2625V
0Eh	1.0000V	28h	1.3000V	42h	1.6250V	5Ch	1.9500V	76h	2.2750V
0Fh	1.0000V	29h	1.3125V	43h	1.6375V	5Dh	1.9625V	77h	2.2875V
10h	1.0000V	2Ah	1.3250V	44h	1.6500V	5Eh	1.9750V	78h	2.3000V
11h	1.0125V	2Bh	1.3375V	45h	1.6625V	5Fh	1.9875V	79h	2.3125V
12h	1.0250V	2Ch	1.3500V	46h	1.6750V	60h	2.0000V	7Ah	2.3250V
13h	1.0375V	2Dh	1.3625V	47h	1.6875V	61h	2.0125V	7Bh	2.3375V
14h	1.0500V	2Eh	1.3750V	48h	1.7000V	62h	2.0250V	7Ch	2.3500V
15h	1.0625V	2Fh	1.3875V	49h	1.7125V	63h	2.0375V	7Dh	2.3625V
16h	1.0750V	30h	1.4000V	4Ah	1.7250V	64h	2.0500V	7Eh	2.3750V
17h	1.0875V	31h	1.4125V	4Bh	1.7375V	65h	2.0625V	7Fh	2.3875V
18h	1.1000V	32h	1.4250V	4Ch	1.7500V	66h	2.0750V	80h	2.4000V
19h	1.1125V	33h	1.4375V	4Dh	1.7625V	67h	2.0875V	81h	2.4125V

Code	Voltage	Code	Voltage	Code	Voltage
82h	2.4250V	A4h	2.8500V	C6h	3.2750V
83h	2.4375V	A5h	2.8625V	C7h	3.2875V
84h	2.4500V	A6h	2.8750V	C8h	3.3000V
85h	2.4625V	A7h	2.8875V	C9h	3.3000V
86h	2.4750V	A8h	2.9000V	CAh	3.3000V
87h	2.4875V	A9h	2.9125V	CBh	3.3000V
88h	2.5000V	AAh	2.9250V	…	…
89h	2.5125V	ABh	2.9375V	FFh	3.3000V
8Ah	2.5250V	ACh	2.9500V		
8Bh	2.5375V	ADh	2.9625V		
8Ch	2.5500V	AEh	2.9750V		
8Dh	2.5625V	AFh	2.9875V		
8Eh	2.5750V	B0h	3.0000V		
8Fh	2.5875V	B1h	3.0125V		
90h	2.6000V	B2h	3.0250V		
91h	2.6125V	B3h	3.0375V		
92h	2.6250V	B4h	3.0500V		
93h	2.6375V	B5h	3.0625V		
94h	2.6500V	B6h	3.0750V		
95h	2.6625V	B7h	3.0875V		
96h	2.6750V	B8h	3.1000V		
97h	2.6875V	B9h	3.1125V		
98h	2.7000V	BAh	3.1250V		
99h	2.7125V	BBh	3.1375V		
9Ah	2.7250V	BCh	3.1500V		
9Bh	2.7375V	BDh	3.1625V		
9Ch	2.7500V	BEh	3.1750V		
9Dh	2.7625V	BFh	3.1875V		
9Eh	2.7750V	C0h	3.2000V		
9Fh	2.7875V	C1h	3.2125V		
A0h	2.8000V	C2h	3.2250V		
A1h	2.8125V	C3h	3.2375V		
A2h	2.8250V	C4h	3.2500V		
A3h	2.8375V	C5h	3.2625V		

Buck3 Output Voltage VSET1 Adjustment

Address – 0x53h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B3_VSET1							
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck3 Output Voltage VSET1 [7:0]

The output voltage is equal to B3_VSET1*0.0125+0.8V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	1.0000V	1Ah	1.1250V	34h	1.4500V	4Eh	1.7750V	68h	2.1000V
01h	1.0000V	1Bh	1.1375V	35h	1.4625V	4Fh	1.7875V	69h	2.1125V
02h	1.0000V	1Ch	1.1500V	36h	1.4750V	50h	1.8000V	6Ah	2.1250V
03h	1.0000V	1Dh	1.1625V	37h	1.4875V	51h	1.8125V	6Bh	2.1375V
04h	1.0000V	1Eh	1.1750V	38h	1.5000V	52h	1.8250V	6Ch	2.1500V
05h	1.0000V	1Fh	1.1875V	39h	1.5125V	53h	1.8375V	6Dh	2.1625V
06h	1.0000V	20h	1.2000V	3Ah	1.5250V	54h	1.8500V	6Eh	2.1750V
07h	1.0000V	21h	1.2125V	3Bh	1.5375V	55h	1.8625V	6Fh	2.1875V
08h	1.0000V	22h	1.2250V	3Ch	1.5500V	56h	1.8750V	70h	2.2000V
09h	1.0000V	23h	1.2375V	3Dh	1.5625V	57h	1.8875V	71h	2.2125V
0Ah	1.0000V	24h	1.2500V	3Eh	1.5750V	58h	1.9000V	72h	2.2250V
0Bh	1.0000V	25h	1.2625V	3Fh	1.5875V	59h	1.9125V	73h	2.2375V
0Ch	1.0000V	26h	1.2750V	40h	1.6000V	5Ah	1.9250V	74h	2.2500V
0Dh	1.0000V	27h	1.2875V	41h	1.6125V	5Bh	1.9375V	75h	2.2625V
0Eh	1.0000V	28h	1.3000V	42h	1.6250V	5Ch	1.9500V	76h	2.2750V
0Fh	1.0000V	29h	1.3125V	43h	1.6375V	5Dh	1.9625V	77h	2.2875V
10h	1.0000V	2Ah	1.3250V	44h	1.6500V	5Eh	1.9750V	78h	2.3000V
11h	1.0125V	2Bh	1.3375V	45h	1.6625V	5Fh	1.9875V	79h	2.3125V
12h	1.0250V	2Ch	1.3500V	46h	1.6750V	60h	2.0000V	7Ah	2.3250V
13h	1.0375V	2Dh	1.3625V	47h	1.6875V	61h	2.0125V	7Bh	2.3375V
14h	1.0500V	2Eh	1.3750V	48h	1.7000V	62h	2.0250V	7Ch	2.3500V
15h	1.0625V	2Fh	1.3875V	49h	1.7125V	63h	2.0375V	7Dh	2.3625V
16h	1.0750V	30h	1.4000V	4Ah	1.7250V	64h	2.0500V	7Eh	2.3750V
17h	1.0875V	31h	1.4125V	4Bh	1.7375V	65h	2.0625V	7Fh	2.3875V
18h	1.1000V	32h	1.4250V	4Ch	1.7500V	66h	2.0750V	80h	2.4000V
19h	1.1125V	33h	1.4375V	4Dh	1.7625V	67h	2.0875V	81h	2.4125V

Description

Code	Voltage	Code	Voltage	Code	Voltage
82h	2.4250V	A4h	2.8500V	C6h	3.2750V
83h	2.4375V	A5h	2.8625V	C7h	3.2875V
84h	2.4500V	A6h	2.8750V	C8h	3.3000V
85h	2.4625V	A7h	2.8875V	C9h	3.3000V
86h	2.4750V	A8h	2.9000V	CAh	3.3000V
87h	2.4875V	A9h	2.9125V	CBh	3.3000V
88h	2.5000V	AAh	2.9250V	…	…
89h	2.5125V	ABh	2.9375V	FFh	3.3000V
8Ah	2.5250V	ACh	2.9500V		
8Bh	2.5375V	ADh	2.9625V		
8Ch	2.5500V	AEh	2.9750V		
8Dh	2.5625V	AFh	2.9875V		
8Eh	2.5750V	B0h	3.0000V		
8Fh	2.5875V	B1h	3.0125V		
90h	2.6000V	B2h	3.0250V		
91h	2.6125V	B3h	3.0375V		
92h	2.6250V	B4h	3.0500V		
93h	2.6375V	B5h	3.0625V		
94h	2.6500V	B6h	3.0750V		
95h	2.6625V	B7h	3.0875V		
96h	2.6750V	B8h	3.1000V		
97h	2.6875V	B9h	3.1125V		
98h	2.7000V	BAh	3.1250V		
99h	2.7125V	BBh	3.1375V		
9Ah	2.7250V	BCh	3.1500V		
9Bh	2.7375V	BDh	3.1625V		
9Ch	2.7500V	BEh	3.1750V		
9Dh	2.7625V	BFh	3.1875V		
9Eh	2.7750V	C0h	3.2000V		
9Fh	2.7875V	C1h	3.2125V		
A0h	2.8000V	C2h	3.2250V		
A1h	2.8125V	C3h	3.2375V		
A2h	2.8250V	C4h	3.2500V		
A3h	2.8375V	C5h	3.2625V		

Buck3 Config Adjustment

Address – 0x54h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B3_ON	x	x	B3_SLEEP_EN	x	B3_DP_SLEEP_EN	x	B3_FORCEPWM
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck3 Enable/Disable [7]

Code	Buck3 ON/OFF
00h	Buck3 is disable
01h	Buck3 is enable

Set Buck3 ON/OFF in Sleep Mode [4]

Code	Buck3 ON/OFF in Sleep Mode
00h	Buck3 stays on when IC enters sleep mode
01h	Buck3 turns off when IC enters sleep mode

Set Buck3 ON/OFF in Deep Sleep Mode [2]

Code	Buck3 ON/OFF in Deep Sleep Mode
00h	Buck3 stays on when IC enters deep sleep mode
01h	Buck3 turns off when IC enters deep sleep mode

Set Buck3 LPM/FCCM [0]

Code	Buck3 LPM/FCCM Selection
00h	Buck3 enters LPM at light load
01h	Buck3 forced into PWM at light load

LDO1 Output Voltage Adjustment

Address – 0xA1h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO1_VSET							
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO1 Output Voltage [7:0]

The output voltage is equal to LDO1_VSET*0.0125+0.8V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	1.0000V	1Ah	1.1250V	34h	1.4500V	4Eh	1.7750V	68h	2.1000V	82h	2.4250V
01h	1.0000V	1Bh	1.1375V	35h	1.4625V	4Fh	1.7875V	69h	2.1125V	83h	2.4375V
02h	1.0000V	1Ch	1.1500V	36h	1.4750V	50h	1.8000V	6Ah	2.1250V	84h	2.4500V
03h	1.0000V	1Dh	1.1625V	37h	1.4875V	51h	1.8125V	6Bh	2.1375V	85h	2.4625V
04h	1.0000V	1Eh	1.1750V	38h	1.5000V	52h	1.8250V	6Ch	2.1500V	86h	2.4750V
05h	1.0000V	1Fh	1.1875V	39h	1.5125V	53h	1.8375V	6Dh	2.1625V	87h	2.4875V
06h	1.0000V	20h	1.2000V	3Ah	1.5250V	54h	1.8500V	6Eh	2.1750V	88h	2.5000V
07h	1.0000V	21h	1.2125V	3Bh	1.5375V	55h	1.8625V	6Fh	2.1875V	89h	2.5000V
08h	1.0000V	22h	1.2250V	3Ch	1.5500V	56h	1.8750V	70h	2.2000V	8Ah	2.5000V
09h	1.0000V	23h	1.2375V	3Dh	1.5625V	57h	1.8875V	71h	2.2125V	8Bh	2.5000V
0Ah	1.0000V	24h	1.2500V	3Eh	1.5750V	58h	1.9000V	72h	2.2250V	…	…
0Bh	1.0000V	25h	1.2625V	3Fh	1.5875V	59h	1.9125V	73h	2.2375V	FFh	2.5000V
0Ch	1.0000V	26h	1.2750V	40h	1.6000V	5Ah	1.9250V	74h	2.2500V		
0Dh	1.0000V	27h	1.2875V	41h	1.6125V	5Bh	1.9375V	75h	2.2625V		
0Eh	1.0000V	28h	1.3000V	42h	1.6250V	5Ch	1.9500V	76h	2.2750V		
0Fh	1.0000V	29h	1.3125V	43h	1.6375V	5Dh	1.9625V	77h	2.2875V		
10h	1.0000V	2Ah	1.3250V	44h	1.6500V	5Eh	1.9750V	78h	2.3000V		
11h	1.0125V	2Bh	1.3375V	45h	1.6625V	5Fh	1.9875V	79h	2.3125V		
12h	1.0250V	2Ch	1.3500V	46h	1.6750V	60h	2.0000V	7Ah	2.3250V		
13h	1.0375V	2Dh	1.3625V	47h	1.6875V	61h	2.0125V	7Bh	2.3375V		
14h	1.0500V	2Eh	1.3750V	48h	1.7000V	62h	2.0250V	7Ch	2.3500V		
15h	1.0625V	2Fh	1.3875V	49h	1.7125V	63h	2.0375V	7Dh	2.3625V		
16h	1.0750V	30h	1.4000V	4Ah	1.7250V	64h	2.0500V	7Eh	2.3750V		
17h	1.0875V	31h	1.4125V	4Bh	1.7375V	65h	2.0625V	7Fh	2.3875V		
18h	1.1000V	32h	1.4250V	4Ch	1.7500V	66h	2.0750V	80h	2.4000V		
19h	1.1125V	33h	1.4375V	4Dh	1.7625V	67h	2.0875V	81h	2.4125V		

LDO1 Config Adjustment

Address – 0xA2h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO1_ON	x	x	LDO1_SLEEP_EN	LDO1_DP_SLEEP_EN	x	x	x
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO1 Enable/Disable [7]

Code	LDO1 ON/OFF
00h	LDO1 is disable
01h	LDO1 is enable

Set LDO1 ON/OFF in Sleep Mode [4]

Code	LDO1 ON/OFF in Sleep Mode
00h	LDO1 stays on when IC enters sleep mode
01h	LDO1 turns off when IC enters sleep mode

Set LDO1 ON/OFF in Deep Sleep Mode [3]

Code	LDO1 ON/OFF in Deep Sleep Mode
00h	LDO1 stays on when IC enters deep sleep mode
01h	LDO1 turns off when IC enters deep sleep mode

LDO2 Output Voltage Adjustment

Address – 0xA7h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO2_VSET							
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO2 Output Voltage [7:0]

The output voltage is equal to LDO2_VSET*0.0125+0.8V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	1.6000V	54h	1.8500V	6Eh	2.1750V	88h	2.5000V	A2h	2.8250V	BCh	3.1500V
01h	1.6000V	55h	1.8625V	6Fh	2.1875V	89h	2.5125V	A3h	2.8375V	BDh	3.1625V
02h	1.6000V	56h	1.8750V	70h	2.2000V	8Ah	2.5250V	A4h	2.8500V	BEh	3.1750V
03h	1.6000V	57h	1.8875V	71h	2.2125V	8Bh	2.5375V	A5h	2.8625V	BFh	3.1875V
04h	1.6000V	58h	1.9000V	72h	2.2250V	8Ch	2.5500V	A6h	2.8750V	C0h	3.2000V
…	…	59h	1.9125V	73h	2.2375V	8Dh	2.5625V	A7h	2.8875V	C1h	3.2125V
40h	1.6000V	5Ah	1.9250V	74h	2.2500V	8Eh	2.5750V	A8h	2.9000V	C2h	3.2250V
41h	1.6125V	5Bh	1.9375V	75h	2.2625V	8Fh	2.5875V	A9h	2.9125V	C3h	3.2375V
42h	1.6250V	5Ch	1.9500V	76h	2.2750V	90h	2.6000V	AAh	2.9250V	C4h	3.2500V
43h	1.6375V	5Dh	1.9625V	77h	2.2875V	91h	2.6125V	ABh	2.9375V	C5h	3.2625V
44h	1.6500V	5Eh	1.9750V	78h	2.3000V	92h	2.6250V	ACh	2.9500V	C6h	3.2750V
45h	1.6625V	5Fh	1.9875V	79h	2.3125V	93h	2.6375V	ADh	2.9625V	C7h	3.2875V
46h	1.6750V	60h	2.0000V	7Ah	2.3250V	94h	2.6500V	AEh	2.9750V	C8h	3.3000V
47h	1.6875V	61h	2.0125V	7Bh	2.3375V	95h	2.6625V	AFh	2.9875V	C9h	3.3000V
48h	1.7000V	62h	2.0250V	7Ch	2.3500V	96h	2.6750V	B0h	3.0000V	CAh	3.3000V
49h	1.7125V	63h	2.0375V	7Dh	2.3625V	97h	2.6875V	B1h	3.0125V	CBh	3.3000V
4Ah	1.7250V	64h	2.0500V	7Eh	2.3750V	98h	2.7000V	B2h	3.0250V	CCh	3.3000V
4Bh	1.7375V	65h	2.0625V	7Fh	2.3875V	99h	2.7125V	B3h	3.0375V	…	…
4Ch	1.7500V	66h	2.0750V	80h	2.4000V	9Ah	2.7250V	B4h	3.0500V	FFh	3.3000V
4Dh	1.7625V	67h	2.0875V	81h	2.4125V	9Bh	2.7375V	B5h	3.0625V		
4Eh	1.7750V	68h	2.1000V	82h	2.4250V	9Ch	2.7500V	B6h	3.0750V		
4Fh	1.7875V	69h	2.1125V	83h	2.4375V	9Dh	2.7625V	B7h	3.0875V		
50h	1.8000V	6Ah	2.1250V	84h	2.4500V	9Eh	2.7750V	B8h	3.1000V		
51h	1.8125V	6Bh	2.1375V	85h	2.4625V	9Fh	2.7875V	B9h	3.1125V		
52h	1.8250V	6Ch	2.1500V	86h	2.4750V	A0h	2.8000V	BAh	3.1250V		
53h	1.8375V	6Dh	2.1625V	87h	2.4875V	A1h	2.8125V	BBh	3.1375V		

LDO2 Config Adjustment

Address – 0xA8h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO2_ON	x	x	LDO2_SLEEP_EN	LDO2_DP_SLEEP_EN	x	x	x
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO2 Enable/Disable [7]

Code	LDO2 ON/OFF
00h	LDO2 is disable
01h	LDO2 is enable

Set LDO2 ON/OFF in Sleep Mode [4]

Code	LDO2 ON/OFF in Sleep Mode
00h	LDO2 stays on when IC enters sleep mode
01h	LDO2 turns off when IC enters sleep mode

Set LDO2 ON/OFF in Deep Sleep Mode [3]

Code	LDO2 ON/OFF in Deep Sleep Mode
00h	LDO2 stays on when IC enters deep sleep mode
01h	LDO2 turns off when IC enters deep sleep mode

LDO1/2 Protection Adjustment

Address – 0xADh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	x	x	x	x	x	x	LDO2_ILIM_SHUTDOWN_DIS	LDO1_ILIM_SHUTDOWN_DIS
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO2 Protection [1]

Code	LDO2 Protection
00h	Shutdown LDO2 after current limit
01h	Disable LDO2 shutdown function after current limit

Set LDO1 Protection [0]

Code	LDO1 Protection
00h	Shutdown LDO1 after current limit
01h	Disable LDO1 shutdown function after current limit

LDO2 Mode Adjustment

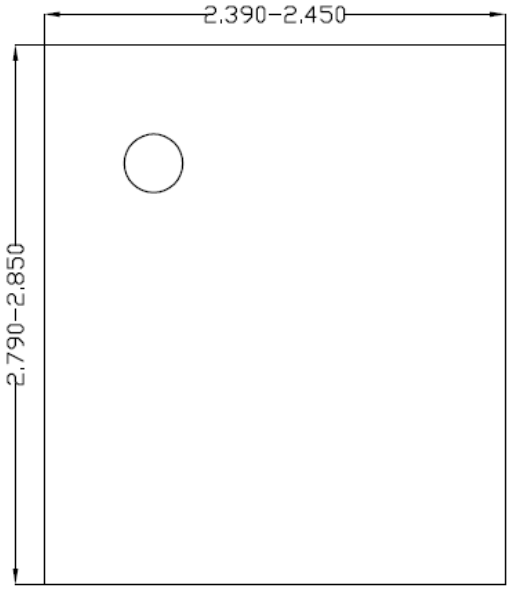
Address – 0xECh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	x	x	x	LDO2_LSW_Mode	x	x	x	x
READ/WRITE	R/W	R/W	R/W	RO	R/W	R/W	R/W	R/W

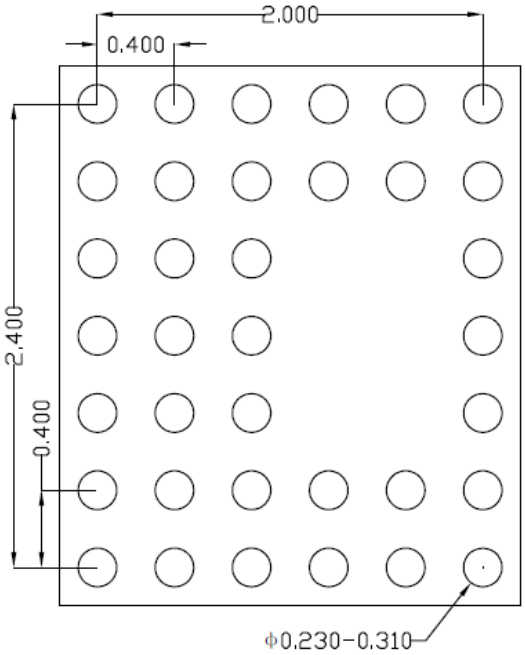
Description	Set LDO2 LDO/LSW Mode [4]. Configuration by vendor ONLY.

Code	LDO2 LDO/LSW Mode
00h	LDO2 operates as LDO
01h	LDO2 operates as a load switch

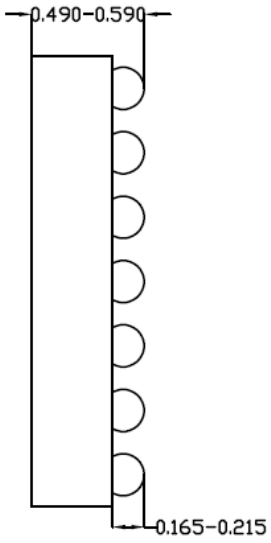
CSP2.42×2.82-36 Package Outline Drawing



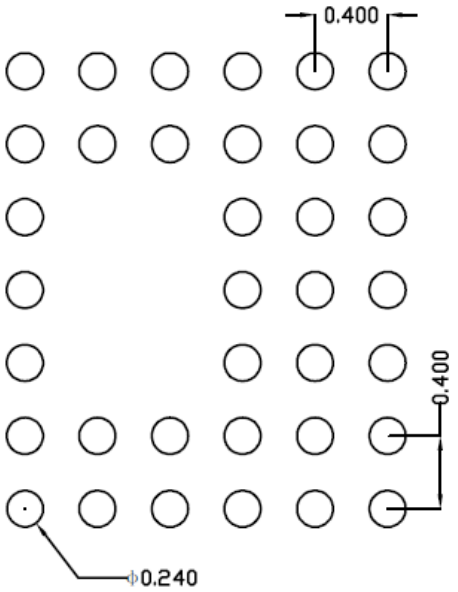
Top View



Bottom View



Side View



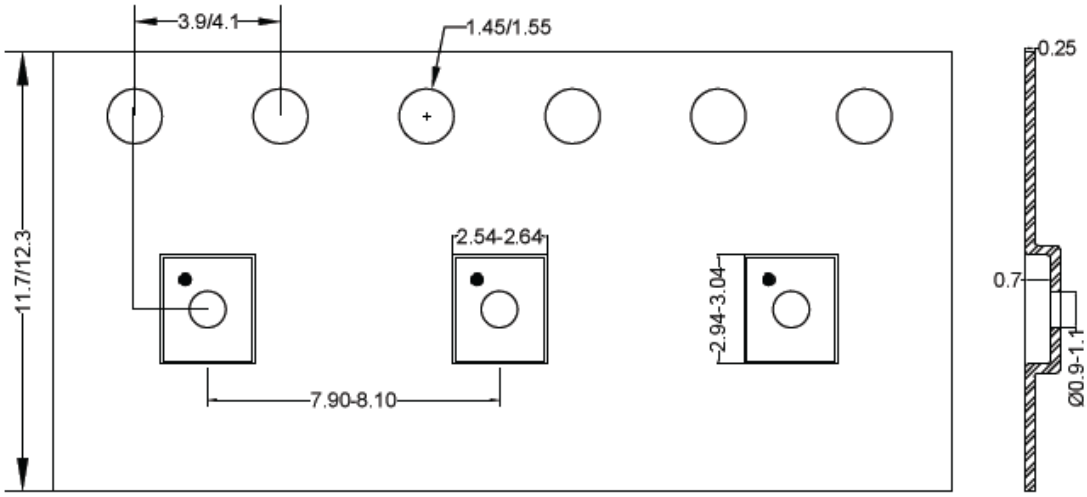
Recommended Pad Layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

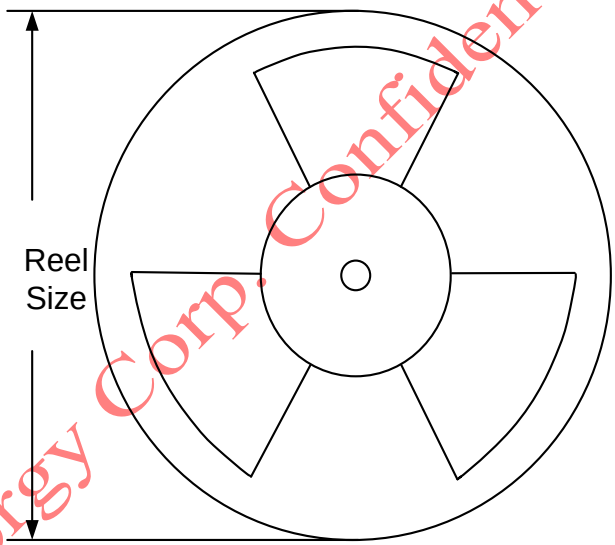
Taping & Reel Specification

1. Taping Orientation

CSP2.42×2.82-36



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
CSP2.42×2.82-36	12	8	13"	400	400	5000