General Description

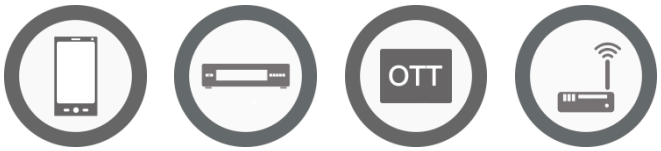
The EA3059 is a 4-CH power management IC for applications powered by one Li-Ion battery or a DC 5V adapter. It integrates four synchronous buck regulators and can provide high efficiency output at light load and heavy load operation. The internal compensation architecture simplifies the application circuit design. Besides, the independent enable control makes the designer have the greatest flexibility to optimize timing for power sequencing purposes. The EA3059 is available in a 24 pin QFN 4x4 package.

Features

- 2.7V to 5.5V Input Voltage Range
- Four Buck Converters
  - Output Voltage Range: 0.6V to Vin
  - Maximum Continuous Load Current: 2A, Maximum Peak Load Current: 4A (4CH total output power consumption must be less than 10W)
  - 180° Phases Shifted Architecture
  - Fixed 1.5MHz Switching Frequency
  - 100% Duty Cycle Low Dropout Operation
  - <1uA Shutdown Current
  - Independent Enable Control
  - Internal Compensation
  - Cycle-by-Cycle Current Limit
  - Short Circuit Protection
- Each Channel Efficiency Up to 95%
- Auto Recovery OTP Protection
- Available in 24-pin 4mm x 4mm QFN Package

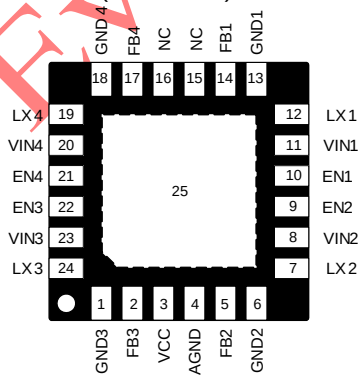
Applications

- Smart Phone
- STB
- OTT
- MiFi



Pin Configurations

(TOP VIEW)



QFN 4x4-24

Pin Description

Pin Name	Function Description	Pin No.
GND3	Power ground pin of CH3.	1
FB3	Feedback input of CH3. Connect to output voltage with a resistor divider.	2
VCC	Input supply pin for internal control circuit.	3
AGND	Analog ground pin.	4
FB2	Feedback input of CH2. Connect to output voltage with a resistor divider.	5
GND2	Power ground pin of CH2.	6
LX2	Internal MOSFET switching output of CH2. Connect LX2 pin with a low pass filter circuit to obtain a stable DC output voltage.	7
VIN2	Power input pin of CH2. Recommended to use a 10uF MLCC capacitor between VIN2 pin and PGND2 pin.	8
EN2	CH2 turns on/turns off control input. Don't leave this pin floating.	9
EN1	CH1 turns on/turns off control input. Don't leave this pin floating.	10
VIN1	Power input pin of CH1. Recommended to use a 10uF MLCC capacitor between VIN1 pin and PGND1 pin.	11
LX1	Internal MOSFET switching output of CH1. Connect LX1 pin with a low pass filter circuit to obtain a stable DC output voltage.	12
GND1	Power ground pin of CH1.	13
FB1	Feedback input of CH1. Connect to output voltage with a resistor divider.	14
NC	No connect.	15, 16
FB4	Feedback input of CH4. Connect to output voltage with a resistor divider.	17
GND4	Power ground pin of CH4.	18
LX4	Internal MOSFET switching output of CH4. Connect LX4 pin with a low pass filter circuit to obtain a stable DC output voltage.	19
VIN4	Power input pin of CH4. Recommended to use a 10uF MLCC capacitor between VIN4 pin and PGND4 pin.	20
EN4	CH4 turns on/turns off control input. Don't leave this pin floating.	21
EN3	CH3 turns on/turns off control input. Don't leave this pin floating.	22
VIN3	Power input pin of CH3. Recommended to use a 10uF MLCC capacitor between VIN3 pin and PGND3 pin.	23
LX3	Internal MOSFET switching output of CH3. Connect LX3 pin with a low pass filter circuit to obtain a stable DC output voltage.	24
Exposed Pad	The Exposed Pad must be soldered to a large PCB copper plane and connected to GND for appropriate dissipation.	25

Function Block Diagram

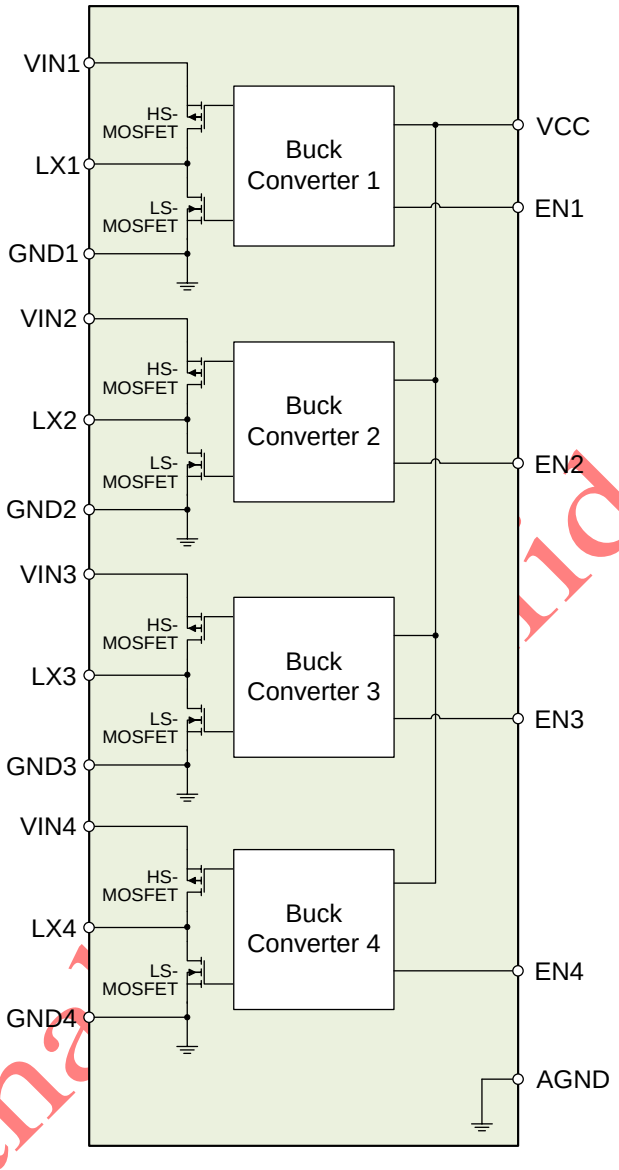


Figure 1. EA3059 internal function block diagram

Absolute Maximum Ratings

Parameter	Value
Input Voltage (V_{VIN1}, V_{VIN2}, V_{VIN3}, V_{VIN4}, V_{VCC})	-0.3V to +6.5V
LX Pin Voltage (V_{LX1}, V_{LX2}, V_{LX3}, V_{LX4})	-0.3V to V_{VINX}+0.3V
All Other Pins Voltage	-0.3V to +6.5V
Ambient Temperature operating Range (T_A)	-40°C to +85°C
Maximum Junction Temperature (T_{Jmax})	+150°C
Lead Temperature (Soldering, 10 sec)	+260°C
Storage Temperature Range (T_S)	-65°C to +150°C

Note (1): Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to "Absolute Maximum Ratings" conditions for extended periods may affect device reliability and lifetime.

Package Thermal Characteristics

Parameter	Value
QFN 4x4-24 Thermal Resistance (θ_{JC})	7.5°C/W
QFN 4x4-24 Thermal Resistance (θ_{JA})	50°C/W
QFN 4x4-24 Power Dissipation at T_A=25°C (P_{Dmax})	2.5W

Note (1): P_{Dmax} is calculated according to the formula: $P_{DMAX}=(T_{JMAX}-T_A)/\theta_{JA}$.

Recommended Operating Conditions

Parameter	Value
Input Voltage (V_{VIN1}, V_{VIN2}, V_{VIN3}, V_{VIN4}, V_{VCC})	+2.7V to +5.5V
Junction Temperature Range (T_J)	-40°C to +125°C

Electrical Characteristics

V_{VINX}=3.6V, V_{VCC}=3.6V, T_A=25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply Voltage						
Input Voltage	V_{INX}		2.7		5.5	V
Control Circuit Input Voltage	V_{VCC}		2.7		5.5	V
Buck Regulator 1, 2, 3, 4						
Shutdown Supply Current	I_{SD}	V_{EN} = 0V		0.1	1	uA
Quiescent Current	I_Q	Non-switching, No Load		40	80	uA
UVLO Threshold	V_{UVLO}	V_{VIN} Rising	1.9	2.1	2.3	V
UVLO Hysteresis	$V_{UV-HYST}$			0.1		V
Output Load Current	I_{LOAD}				2	A
Reference Voltage	V_{REF}		0.588	0.6	0.612	V
Switching Frequency	F_{SW}	I_{LOAD} = 100mA	1	1.5	2	MHz
Short Frequency	$F_{SW-SHORT}$	V_{OUT} = 0V		350		KHz
PMOS Current Limit	I_{LIM-P}		4	5		A
PMOS On-Resistance	$R_{DS(ON)-P}$	I_{LOAD} = 100mA		100		mΩ
NMOS On-Resistance	$R_{DS(ON)-N}$	I_{LOAD} = 100mA		90		mΩ
Enable Pin Input Low Voltage	V_{EN-L}				0.4	V
Enable Pin Input High Voltage	V_{EN-H}		2			V
Maximum Duty Cycle	D_{MAX}		100			%
Thermal Shutdown						
Thermal Shutdown Threshold	T_{OTP}			165		°C
Thermal Shutdown Hysteresis	T_{HYST}			30		°C

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.
(2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

Application Circuit Diagram

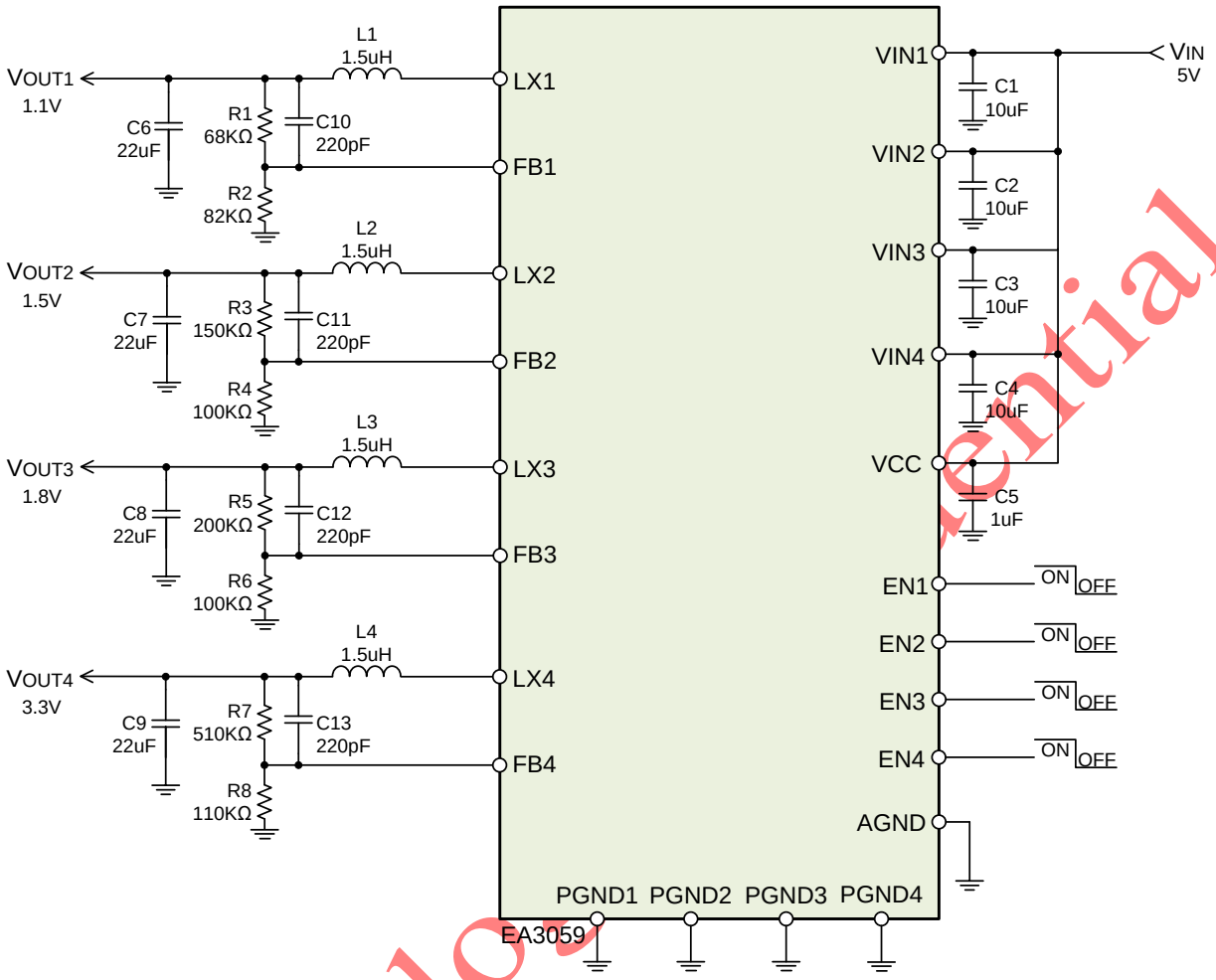


Figure 2. Typical application circuit diagram

Ordering Information

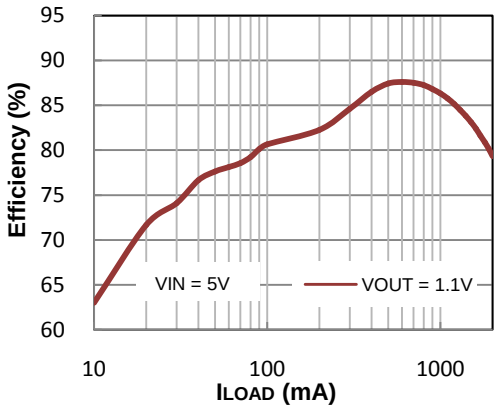
Part Number	Package Type	Packing Information
EA3059QDR	QFN 4mm x 4mm-24	Tape & Reel / 3000

Note (1):"QD": Package type code.
(2):"R": Tape & Reel.

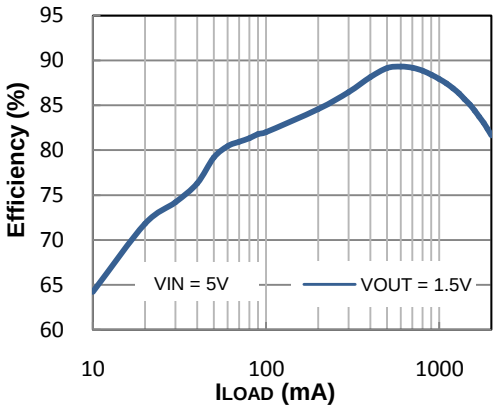
Typical Operating Characteristics

V_{IN}=5V, V_{VCC}=5V, V_{OUT1}=1.1V, V_{OUT2}=1.5V, V_{OUT3}=1.8V, V_{OUT4}=3.3V, L1=1.5uH, L2=1.5uH, L3=1.5uH, L4=1.5uH, T_A=25°C, unless otherwise noted

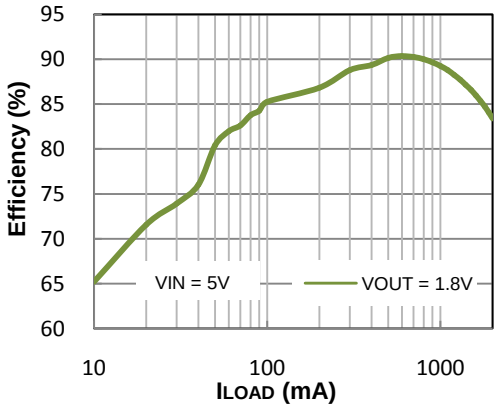
Efficiency vs. Load Current



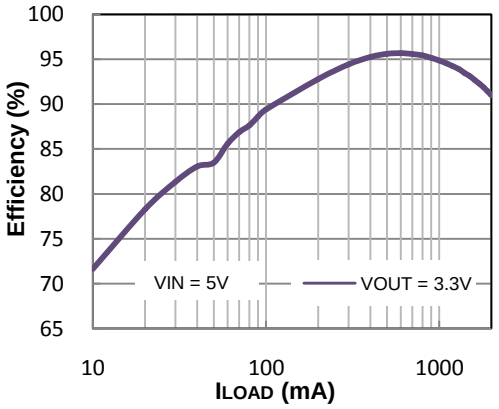
Efficiency vs. Load Current



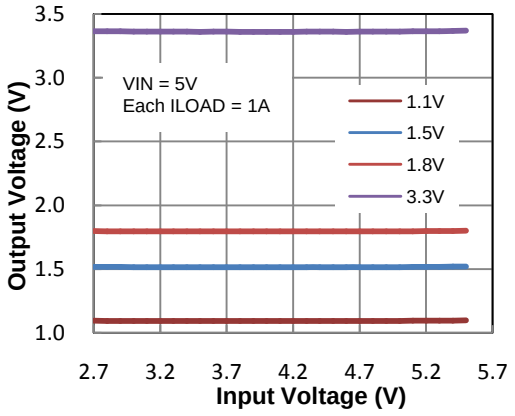
Efficiency vs. Load Current



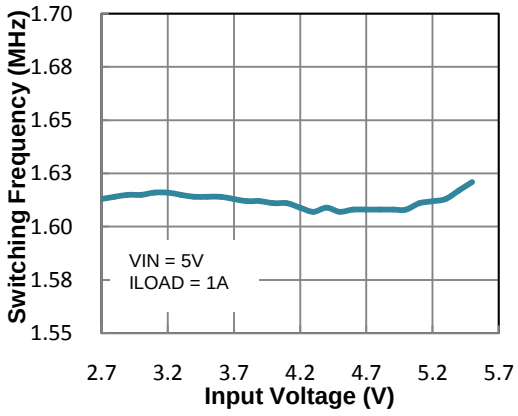
Efficiency vs. Load Current



Vout vs. Vin



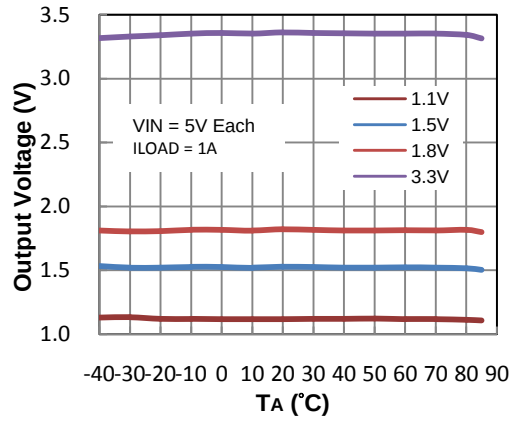
Freq. vs. Vin



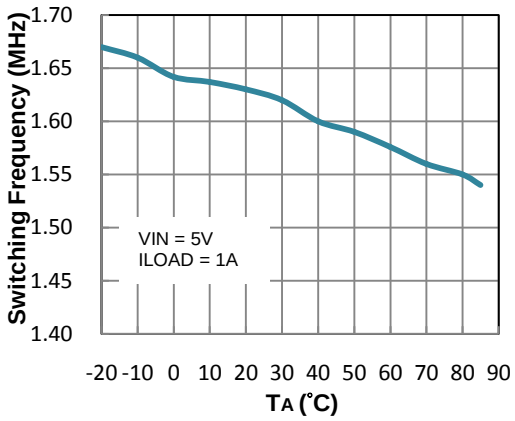
Typical Operating Characteristics

V_{IN}=5V, V_{VCC}=5V, V_{OUT1}=1.1V, V_{OUT2}=1.5V, V_{OUT3}=1.8V, V_{OUT4}=3.3V, L1=1.5uH, L2=1.5uH, L3=1.5uH, L4=1.5uH, T_A=25°C, unless otherwise noted

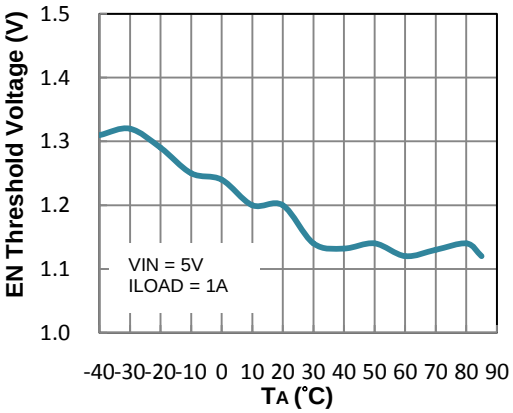
Vout vs. Ambient Temp.



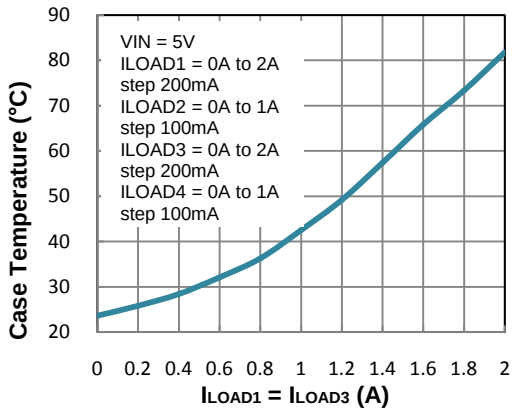
Freq. vs. Ambient Temp.

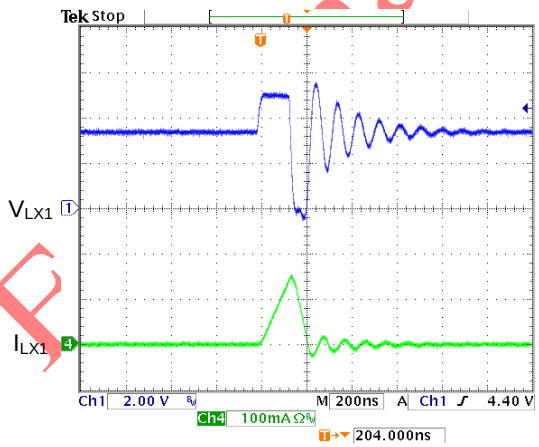


VENth vs. Ambient Temp.

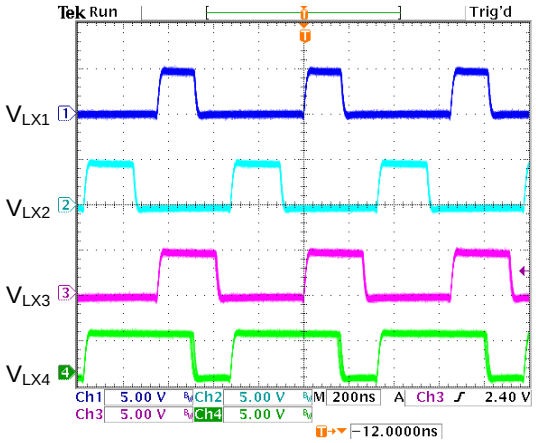


TC vs. Load Current





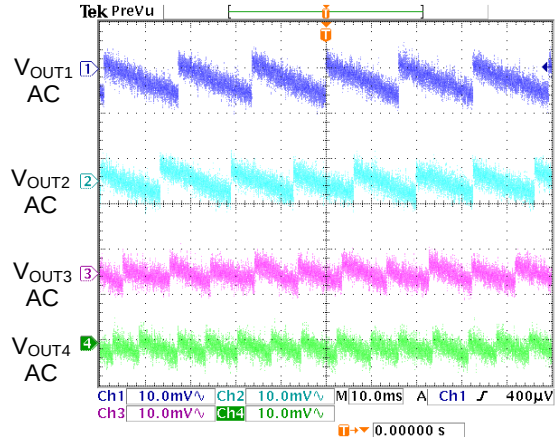
No Load LX Waveform



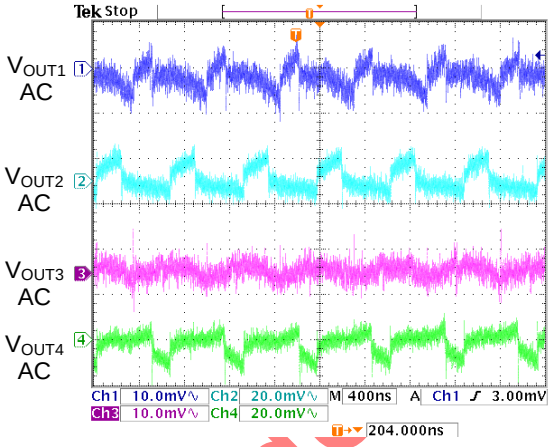
Each Channel 1A Loading LX Waveform

Typical Operating Characteristics

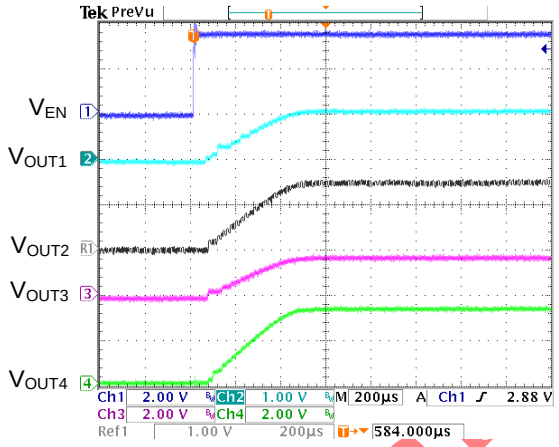
V_{IN}=5V, V_{VCC}=5V, V_{OUT1}=1.1V, V_{OUT2}=1.5V, V_{OUT3}=1.8V, V_{OUT4}=3.3V, L1=1.5uH, L2=1.5uH, L3=1.5uH, L4=1.5uH, T_A=25°C, unless otherwise noted



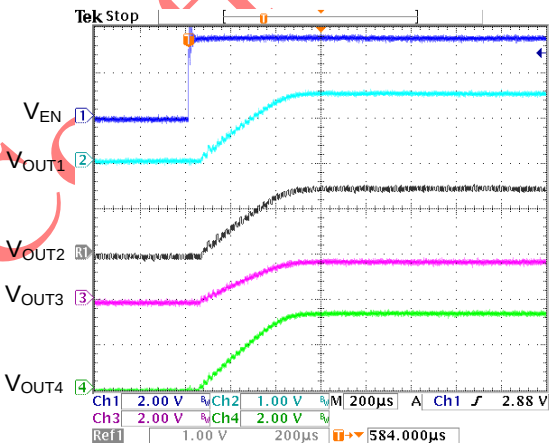
0A Loading Steady State Waveform



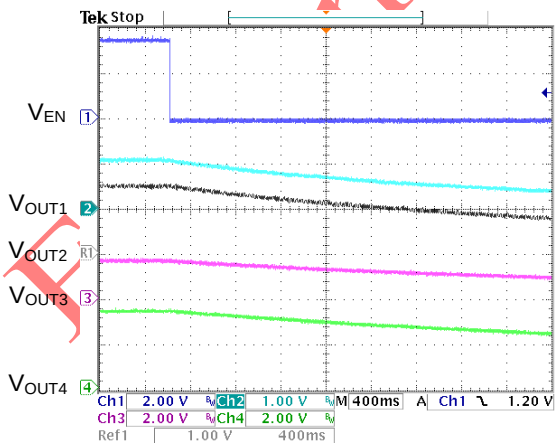
1A Loading Steady State Waveform



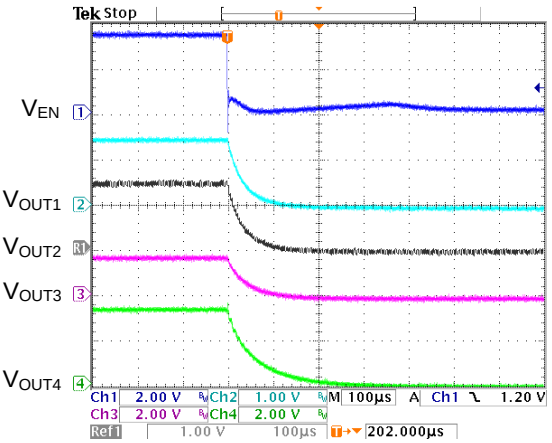
0A Loading EN Turn On Waveform



1A Loading EN Turn On Waveform



0A Loading EN Turn Off Waveform



1A Loading EN Turn Off Waveform

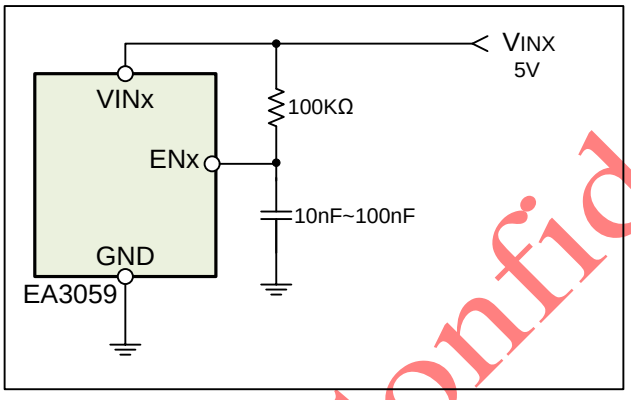
Functional Description

PFM/PWM Operation

Each of the buck regulators can be operated at PFM/PWM mode. If the output current is less than 150mA (typ.), the regulators automatically enters the PFM mode. The output voltages and output ripples at PFM mode are higher than the output voltages and output ripples at PWM mode. But at very light load, the PFM mode operation provides higher efficiency than PWM mode operation.

Enable Control

The EA3059 is a high efficiency Power Management IC which is designed for OTT applications. It incorporates four 2A synchronous buck regulators and can be controlled by individual EN pins. The start-up time for each channel can be programmed by using the circuit shown as below:



180° Phases Shifted Architecture

In order to reduce the input ripple current, the EA3059 applied 180° phases shifted architecture. Buck1 and Buck3 have the same phase and Buck2 and Buck4 are 180° out of phase. This architecture allows the system board has less ripple current, and thus can reduce EMI.

Over Current Protection

The EA3059 internal four regulators have their own cycle-by-cycle current limit circuits. When the inductor peak current exceeds the current limit threshold, the output voltage starts to drop until FB pin voltage is below the threshold, typically 30% below the reference. Once the threshold is triggered, the switching frequency is reduced to 350KHz (typ.).

Thermal Shutdown

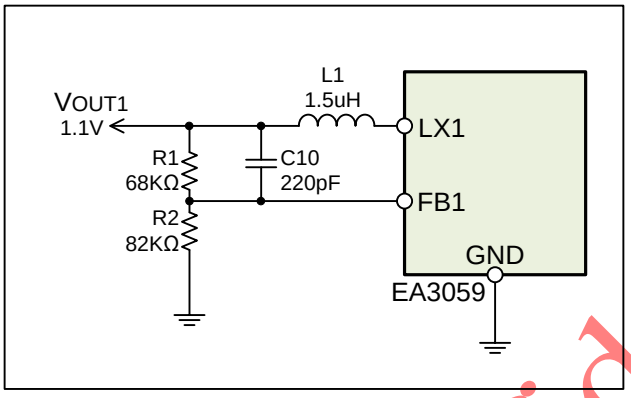
The EA3059 will automatically disabled if the die temperature is higher than the thermal shutdown threshold point. To avoid unstable operation, the hysteresis of thermal shutdown is about 30°C.

Application Information

Output Voltage Setting

Each of the regulators output voltage can be set via a resistor divider (ex. R1, R2). The output voltage is calculated by following equation:

$$V_{OUT1} = 0.6 \times \frac{R1}{R2} + 0.6\ V$$



The following table lists common output voltage and the corresponding R1, R2 resistance value for reference.

Output Voltage	R1 Resistance	R2 Resistance	Tolerance
3.3V	510KΩ	110KΩ	1%
1.8V	200KΩ	100KΩ	1%
1.5V	150KΩ	100KΩ	1%
1.1V	68KΩ	82KΩ	1%

Input / Output Capacitors Selection

The input capacitors are used to suppress the noise amplitude of the input voltage and provide a stable and clean DC input to the device. Because the ceramic capacitor has low ESR characteristic, so it is suitable for input capacitor use. It is recommended to use X5R or X7R MLCC capacitors in order to have better temperature performance and smaller capacitance tolerance. In order to suppress the output voltage ripple, the MLCC capacitor is also the best choice. The suggested part numbers of input / output capacitors are as follows:

Vendor	Part Number	Capacitance	Edc	Parameter	Size
TDK	C2012X5R1A106M	10uF	10V	X5R	0805
TDK	C3216X5R1A106M	10uF	10V	X5R	1206
TDK	C2012X5R1A226M	22uF	10V	X5R	0805
TDK	C3216X5R1A226M	22uF	10V	X5R	1206

Output Inductor Selection

The output inductor selection mainly depends on the amount of ripple current through the inductor ΔI_L. Large ΔI_L will cause larger output voltage ripple and loss, but the user can use a smaller inductor to save cost and space. On the contrary, the larger inductance can get smaller ΔI_L and

thus the smaller output voltage ripple and loss. But it will increase the space and the cost. The inductor value can be calculated as:

$$L = \frac{V_{PWR} - V_{OUT}}{\Delta I_L \times F_{SW}} \times \frac{V_{OUT}}{V_{PWR}}$$

For most applications, 1.0uH to 2.2uH inductors are suitable for EA3059.

Power Dissipation

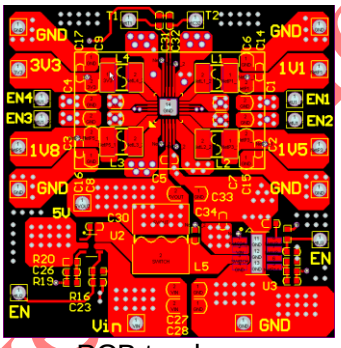
The total output power dissipation of EA3059 should not to exceed the maximum 10W range. The total output power dissipation can be calculated as:

$$P_{D\,(total)} = V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2} + V_{OUT3} \times I_{OUT3} + V_{OUT4} \times I_{OUT4}$$

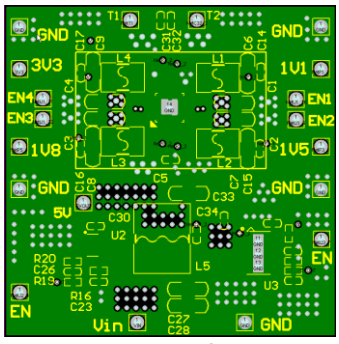
PCB Layout Recommendations

Layout is very critical for PMIC designs. For EA3059 PCB layout considerations, please refer to the following suggestions to get best performance.

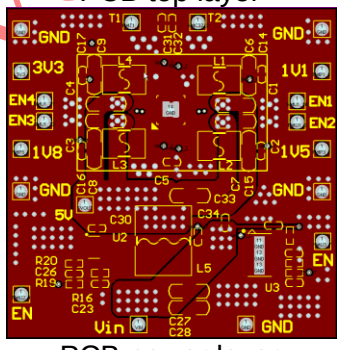
- It is suggested to use 4-layer PCB layout and place LX plane and output plane on the top layer, place VIN plane in the inner layer.
- The top layer SMD input and output capacitors ground plane should be connected to the internal ground layer and bottom ground plane individually by using vias.
- The AGND should be connected to inner ground layer directly by using via.
- High current path traces need to be widened.
- Place the input capacitors as close as possible to the VINx pin to reduce noise interference.
- Keep the feedback path (from V_{OUTX} to FBx) away from the noise node (ex. LXx). LXx is a high current noise node. Complete the layout by using short and wide traces.
- The top layer exposed pad ground plane should be connected to the internal ground layer and bottom ground plane by using a number of vias to improve thermal performance.
- Place the input capacitors as close as possible to the VINx pin to reduce noise interference.



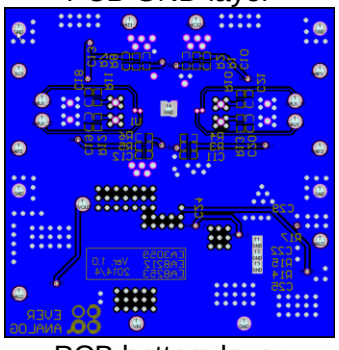
PCB top layer



PCB GND layer

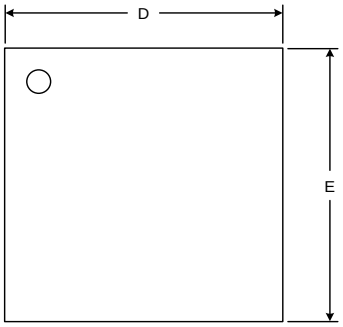


PCB power layer

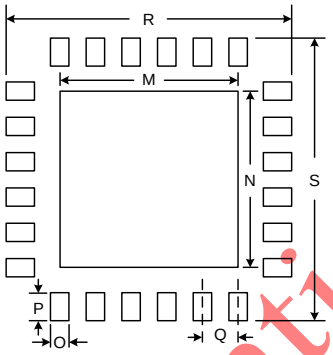

PCB bottom layer

Package Information

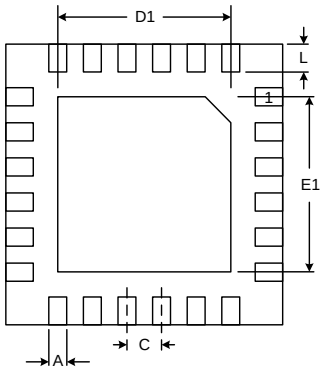
QFN 4mm x 4mm-24 Package



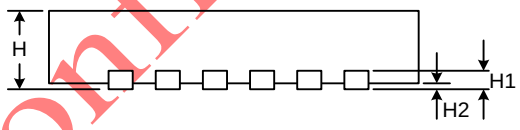
Top View



Recommended Layout Pattern



Bottom View



Side View

Unit: mm

Symbol	Dimension Min	Dimension Max	Symbol	Dimension Typ
A	0.18	0.30	M	2.60
C	0.45	0.55	N	2.60
D	3.95	4.05	O	0.30
E	3.95	4.05	P	0.80
D1	2.30	2.70	Q	0.50
E1	2.30	2.70	R	4.70
L	0.35	0.45	S	4.70
H	0.70	0.90		
H1	0.17	0.25		
H2	0.00	0.05		