TOLL Microelectronic13W 802.3af PoE Powered Device Interface with Flyback/Buck DC/DC Converter

Features

- Compatible with 802.3af Specifications
- Support 13W PoE Power Application
- 100V, 0.6Ω Integrated Pass Switch
- 150mA DC Input Current Limit
- 450mA PD Operation Current Limit
- Intelligent Maintain Power Signature (MPS)
- Integrated 160V Switching Power MOSFET
- Supports Primary-Side Regulated Flyback without Opto-Coupler Feedback
- Supports Low-side Switch Buck Converter
- 3A Programmable Switching Current Limit
- OLP, OVP, OTP and Open-Circuit Protection
- Minimal External Components
- QFN4x5-28 Package

Application

- IEEE 802.3af-Compliant Devices
- Security Camera
- VoIP Phones
- WLAN Access Points
- IoT Devices

Description

The TMI7321 is an integrated IEEE 802.3af PoE compliant Powered Device (PD) power supply solution. It includes a PD interface and an isolated/non-isolated fly-back or Buck converter.

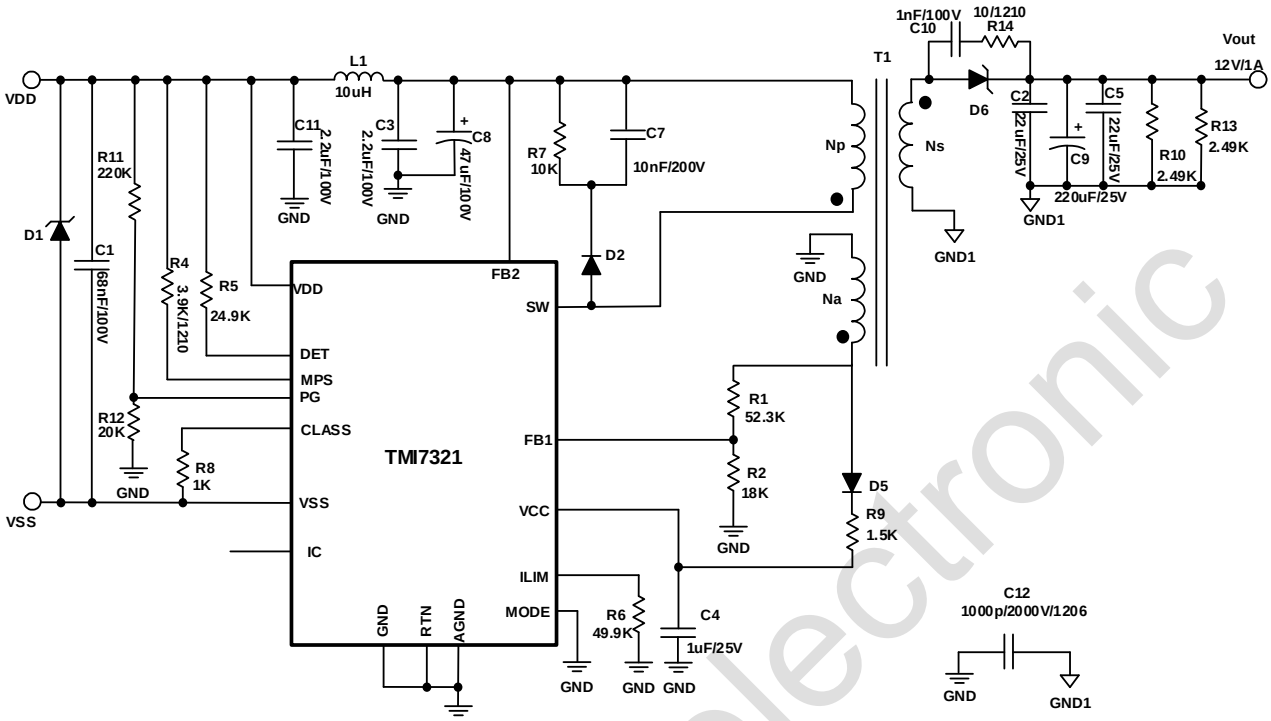
The PD interface includes detection and all the functions of IEEE 802.3af, classification, 150mA inrush current, 450mA operation current limit as well as 100V Hot-swap MOSFET.

The DC/DC converter uses fixed peak current and variable frequency discontinuous conduction mode (DCM) to regulate constant output voltage. The primary-side regulation without opto-coupler feedback in fly-back mode simplifies the design while buck mode continues minimizes the solution size for non-isolated applications. A 160V integrated power MOSFET optimizes the device for various wide voltage applications

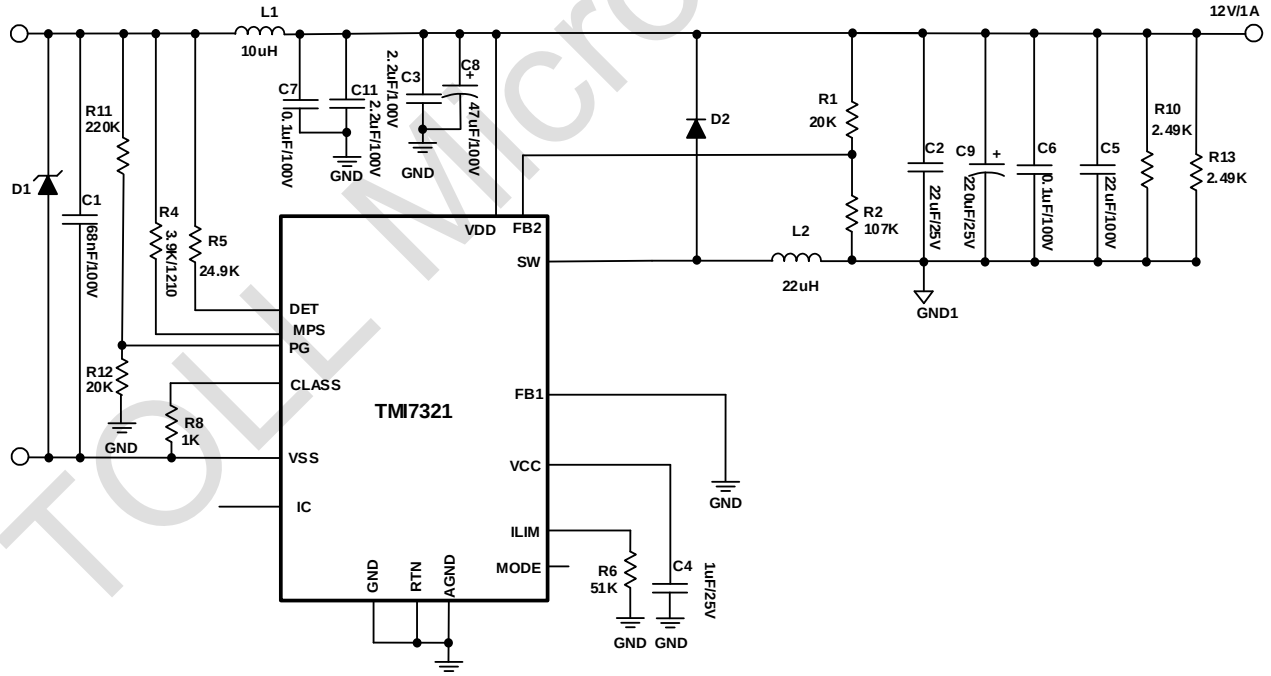
It incorporates over current, open-circuit, and over-voltage protection and thermal shutdown.

The TMI7321 supports a front-end solution for PoE-PD application with minimal external components and is available in QFN4x5-28 package.

Typical Application

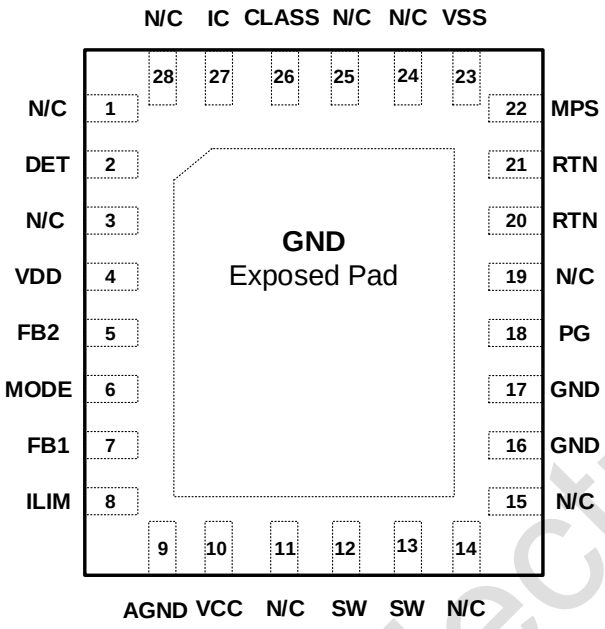


TMI7321 Flyback Typical Application Circuit



TMI7321 Buck Typical Application Circuit

Package



Top View

QFN4x5-28

Top Marking: T7321/XXXXX (T7321: Device Code, XXXXX: Inside Code)

Order Information

Part Number	Package	Top Marking	Quantity/ Reel
TMI7321	QFN4x5-28	T7321 XXXXX	3000

TMI7321 devices are Pb-free and RoHS compliant.

Pin Functions

Pin	Name	Function
2	DET	Connect 24.9kΩ resistor between VDD and DET for PoE detection.
1,3,11,14,15,19,24,25,28	N/C	Not connected internally, can be connected to GND pin and exposed thermal pad in layout.
4	VDD	Positive power supply terminal from PoE input power rail.
5	FB2	Feedback pin for non-isolated buck solution. Connect FB2 to VDD in Flyback application.
6	MODE	Buck mode or Flyback mode select pin. MODE is pulled up internally to VCC through a 1.5μA current source. Float MODE for buck application mode; connect MODE to GND forFlyback application mode.
7	FB1	Feedback for flyback solution. Connect FB1 to GND in buck application.
8	ILIM	DCDC converter switching current limit program pin. Connect ILIM to GND through a resistor to program the peak current limit.
9	AGND	Analog power return for DCDC converter control circuit. Connect to GND through single point.
10	VCC	Supply bias voltage pin, powered through internal LDO from VIN. It is recommended to connect a capacitor (no less than 1μF) between VCC and GND.
12,13	SW	Drain of converter switching MOSFET.
16,17	GND	Switching converter power return. Connect to RTN for PoE power supply. Exposed thermal pad can be connected to GND plane for heat sink.
18	PG	PD supply power good indicator. This signal will enable the DCDC converter internally. It is pulled up by internal current source in output high condition, suggest float it in application.
20,21	RTN	Drain of PD Hot-swap MOSFET, connect GND and AGND to this pin.
22	MPS	To enable MPS, connect to VDD through a resistor. Keep floating when MPS is not used
23	VSS	Negative power supply terminal from PoE input power rail.
26	CLASS	Connect resistor from CLASS to VSS to program classification current.
27	IC	Keep floating.

Absolute Maximum Ratings (Note 1)

Parameter	Min	Max	Unit
VDD, RTN, DET, MPS, GND, AGND to VSS	-0.3	100	V
CLASS to VSS	-0.3	6.5	V
VDD to GND	-0.3	100	V
SW to GND	-0.3	160	V
FB1 to GND	-0.3	5.5	V
VCC, MODE, ILIM, PG to GND	-0.3	5.5	V
FB2 to VDD	-5.5	0.3	V
VCC Sinking Current		5	mA
FB1 Sinking Current		1	mA
Continuous Power Dissipation (T_A=+25°C), PD		3.12	W
Junction Temperature	-40	150	°C
Lead Temperature		260	°C
Storage Temperature	-65	150	°C

ESD Rating (Note4)

Items	Description	Value	Unit
V_{ESD_HBM}	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2017 Classification, Class: 2	±2000	V
V_{ESD_CDM}	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2018 Classification, Class: C3	±1000	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±200	mA

JEDEC specification JS-001

Recommended Operating Conditions

Parameter	Min	TYP	Max	Unit
Supply Voltage V_{DD}	0		57	V
Switching Voltage V_{SW}	-0.5		150	V
Maximum VCC Sinking Current		3		mA
Maximum FB1 Sinking Current	-0.5		0.5	mA
Maximum Switching Frequency		300		kHz
Maximum Switching Current Limit		3		A
Operating Junction Temperature, T_J	-40		125	°C

Thermal Resistance (Note3)

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	40	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance	9	°C/W

Electrical Characteristics

VDD, CLASS, DET, and RTN voltages are referenced to VSS, and all other pin voltages are referenced to GND, GND and RTN are shorted. V_{DD} – V_{SS} = 48V, V_{SS} = 0V; R_{DET} = 24.9kΩ, R_{CLASS} = 1000 Ω, T_{J_TYP} =25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Detection						
V_{DET_ON}	Detection on	V_{VDD} Rising		1.4		V
V_{DET_OFF}	Detection off	V_{VDD} Rising	11	12	13	V
V_{DET_LK}	DET Leakage Current	V_{DET}=V_{VDD}=57V, Measure I_{DET}		0.1	5	μA
V_{DET_H}	Detection on/off Hysteresis	Falling below 12V on Threshold		1		V
I_{DET}	Detection Current	V_{VDD}=1.4V, Measure I_{SUPPLY}	55.1	56	56.9	μA
		V_{VDD}=10.1V, Measure I_{SUPPLY}	400	408	416	μA
Classification						
V_{CLASS}	VCLASS Output Voltage	13V<V_{VDD}< 21V 1mA<I_{CLASS}< 30mA	1.166	1.22	1.28	V
I_{CLASS}	Classification Current	13≤V_{VDD}≤21V, Guaranteed by V_{CLASS}				
		Class 0 R_{CLASS}=1000Ω, 13≤V_{VDD}≤21V	1	1.2	2.8	mA
		Class 1 R_{CLASS}=115Ω, 13≤V_{VDD}≤21V	10.3	10.6	11.3	
		Class 2 R_{CLASS}=66.5Ω, 13≤V_{VDD}≤21V	17.7	18.3	19.5	
		Class 3 R_{CLASS}=43Ω, 13≤V_{VDD}≤21V	27.1	28.4	29.5	
V_{CL_ON}	Classification Lower Threshold	Regulator Turns on, V_{VDD} Rising	11	12	13	V
V_{CU_OFF}	Classification Upper Threshold	Regulator Turns off, V_{VDD} Rising	21	22	23	V
V_{CL_HYS}	Classification Hysteresis	Low side Hysteresis		0.77		V
I_{IN_CLASS}	IC Supply Current during Classification	V_{DD} =17.5V, CLASS Floating	100	150	200	μA
$I_{LEAKAGE}$	Leakage Current	V_{CLASS} =0 V, V_{VDD} =57V			1	μA
PD UVLO						
$V_{DD\text{-}VSS\text{-}R}$	VDD Turn on Threshold	VDD Rising	37.5	38.6	40	V
$V_{DD\text{-}VSS\text{-}F}$	VDD Turn off Threshold	VDD Falling		31		V
I_{IN}	IC Supply Current during Operation	V_{VDD} = 48V, Pins 5, 6 Floating Measure I_{VDD}		240	450	μA
Pass Device and Current Limit						
$R_{ON\text{-}RTN}$	On Resistance	I_{RTN}=600mA		0.6		Ω
$I_{RTN\text{-}LK}$	Leakage Current	V_{DD}=VRTN=57V		1	15	μA
I_{LIMIT}	Current Limit	V_{RTN}=1V	400	450	500	mA
I_{LIMIT}	Inrush Current Limit	V_{RTN}=2V	120	150	200	mA

Electrical Characteristics

VDD, CLASS, DET, and RTN voltages are referenced to VSS, and all other pin voltages are referenced to GND, GND and RTN are shorted. V_{DD} – V_{SS} = 48V, V_{SS} = 0V; R_{DET} = 24.9kΩ, R_{CLASS} = 1000Ω, T_{J_TYP} =25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DELAY}	Inrush to Operation Mode Delay		80	94	110	ms
V_{FOLD}	Current Fold-back Threshold	V_{RTN} Rising	9.5	10	105	V
t_{FOLD}	Fold-back Deglitch Time	V_{RTN} Rising to Inrush Current Fold-back		345		µs
MPS						
I_{MPS_TH}	Automatic MPS falling current threshold	Startup has completed, IRTN falling threshold to generate MPS pulses		35		mA
I_{MPS_HYS}	HYS	Hysteresis on RTN current		3		mA
D_{MPS}	MPS pulsed mode duty cycle	MPS pulsed current ON time	75	80	95	ms
		MPS pulsed current OFF time	225	240	255	ms
		MPS pulsed current duty cycle	24.7%	25%	25.3%	
PG						
I_{PG_Sink}	PG Sink Current	VRTN = 1.5V, VPG = 0.8V, during inrush period	130	230	330	µA
I_{PG_LKG}	PG Off -leakage Current	VPG = 48V		0.1	1	µA
PD Thermal Shutdown						
T_{PD-SD}	Thermal Shut down Temperature(5)		140	152	160	°C
T_{PD-HYS}	Thermal Shut down Hysteresis(5)			20		°C
Converter Power Supply and UVLO						
$V_{DD-RTN-R}$	Converter VDD UVLO Rising Threshold	VIN rising	10.5	11.5	12.8	V
$V_{DD-RTN-F}$	Converter VDD UVLO Falling Threshold	VIN falling	7.4	8.1	9	V
V_{CC}	VCC Regulation (Note9)	Load = 0mA to 10mA	4.3	4.5	4.7	V
V_{CC-R}	VCC UVLO Rising Threshold (Note9)	VDD is higher than UVLO, VCC rising	3.4	3.6	3.8	V
V_{CC-F}	VCC UVLO Falling Threshold (Note9)	VDD is higher than UVLO, VCC falling		3.5		V
I_Q	Quiescent Current	VFB1 = 2.2 V, VFB2 = VDD, Test supply from VDD to VSS		388		µA
V_{EN_H}	EN high-level voltage			1.66		V
V_{EN_L}	EN low-level voltage			0.9		V
I_{EN}	EN input current			1	10	µA

Electrical Characteristics

VDD, CLASS, DET, and RTN voltages are referenced to VSS, and all other pin voltages are referenced to GND, GND and RTN are shorted. V_{DD} – V_{SS} = 48V, V_{SS} = 0V; R_{DET} = 24.9kΩ, R_{CLASS} = 1000 Ω, T_{J_TYP} =25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Voltage Feedback						
V_{REF1}	FB1 Reference Voltage	Respect to GND, T_J = -40°C to +125°C	1.93	1.99	2.05	V
I_{FB1}	FB1 Leakage Current	Respect to GND, VFB1 = 2V		10	50	nA
V_{DCM1}	Flyback Mode DCM Detect Threshold on FB1	Respect to GND	25	50	75	mV
$V_{FB1OPEN}$	FB1 Open-circuit Threshold		-80	-50	-20	mV
V_{FB1OVP}	FB1 OVP Threshold		120%	125%	130%	V_{REF1}
T_{SAMPLE}	Minimum Diode Conduction Time for FB1 Sample		0.95	1.4	2.04	μs
V_{REF2}	FB2 Reference Voltage	Respect to VDD, T_J = 25°C	-1.96	-1.88	-1.8	V
I_{FB2}	FB2 Leakage Current	Respect to VDD, VFB2 = -2V		10	50	nA
V_{DCM2}	Buck Mode DCM Detect Threshold on SW	Respect to VDD	0.04	0.06	0.23	V
Switching Power Device						
R_{ON-SW}	On Resistance	V_{CC} = 4.5V		0.8		Ω
Current Sense						
I_{LIMIT}	Switching Current Limit	R_{ILIM} = 52.4kΩ, L = 16.4μH		2.3		A
T_{LEB}	Switching Current Leading edge Blanking Time			280		ns
DCDC Converter Thermal Shutdown						
T_{SD}	Thermal Shutdown Temperature (Note5)			150		°C
T_{HYS}	Thermal Shutdown Hysteresis (Note5)			20		°C

Notes 1: Exceeding these ratings may damage the device.

Notes 2: GND and AGND must be connected to RTN

Notes 3: Refer to the “Converter Output Voltage Setting” section.

Notes 4: VCC voltage can be pulled higher than this rating, but the external pull-up current should be limited. Refer to “VCC sinking current” rating and “VCC Power Supply Setting” section.

Notes 5: The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J(MAX)}$, the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $PD_{(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Notes 6: The device is not guaranteed to function outside of its operating conditions.

Notes 7: Measured on JESD51-7, 4-layer PCB.

Notes 8: Guaranteed by characterization, not tested in production.

Notes 9: The maximum VCC UVLO rising threshold is higher than the minimum VCC regulation in the EC table due to production distribution. However, for one unit, VCC regulation is higher than the VCC UVLO rising threshold. The VCC UVLO rising threshold is about 87 percent of the VCC regulation voltage, and the VCC UVLO falling threshold is about 83 percent of the VCC regulation voltage in one unit.

Block Diagram

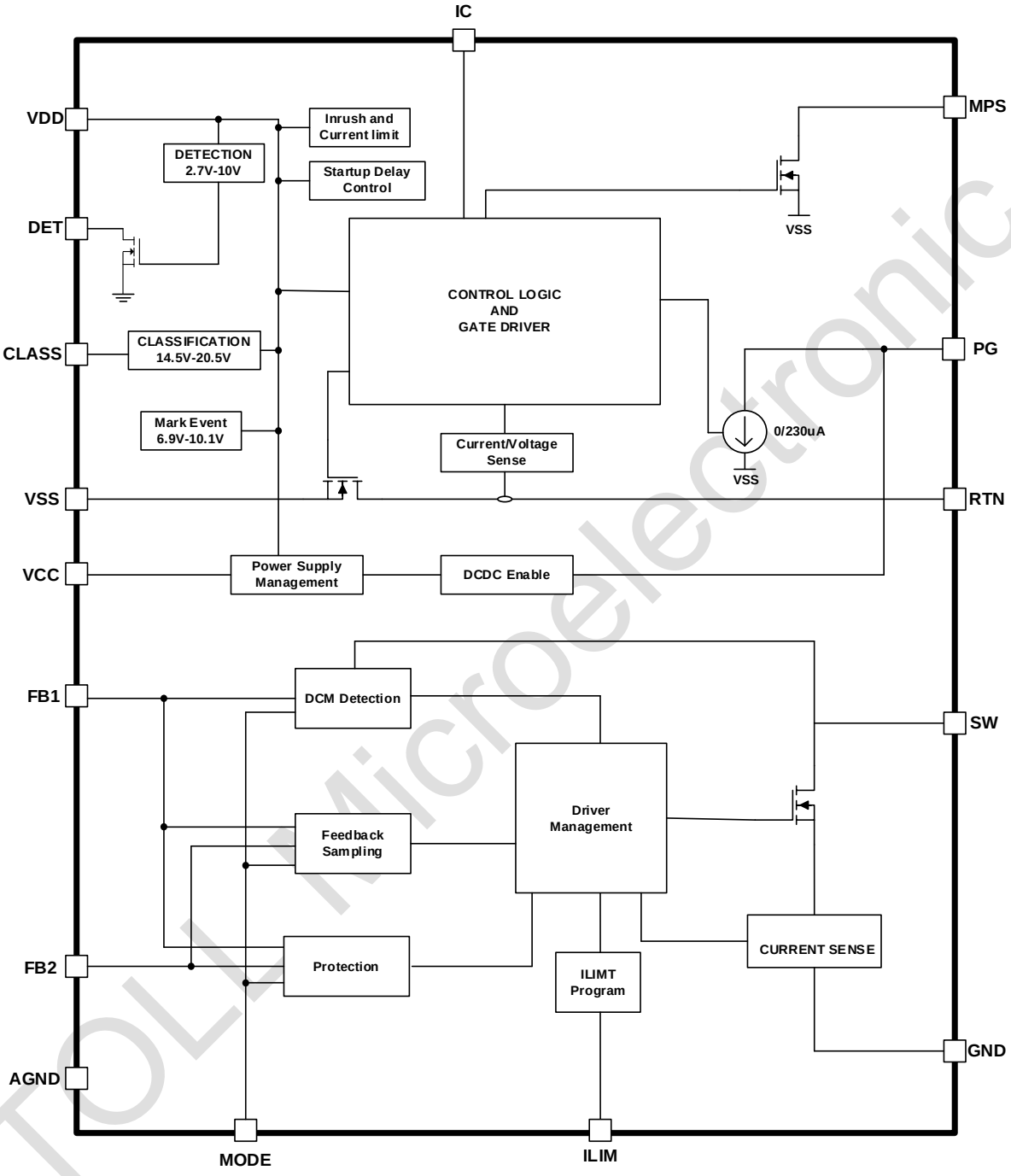


Figure 2 TMI7321 Block Diagram

Operation Description

Overview

Compared with IEEE802.3af, the IEE802.3at standard establishes a higher power allocation for Power-over-Ethernet while maintaining backwards compatibility with the existing IEEE802.3af systems. Power Sourcing Equipment (PSE) and Powered Devices (PD) are distinguished as Type-1 complying with the IEEE 802.3af power levels, or Type-2 complying with the IEEE 802.3at power levels. IEEE802.3af/at standard establishes a method of communication between PD and PSE with detection, classification and mark event.

The TMI7321 is one integrated PoE solution with IEEE 802.3af PD interface and 13W DCDC converter, so TMI7321 is only used for 802.3af power design. Along with the PSE it operates as a safety device to supply voltage only when the power sourcing equipment recognizes a unique, tightly specified resistance at the end of an unknown length of Ethernet cable. After powered from PSE, the TMI7321 will regulate the output voltage based on application with isolated or non-isolated topology. Figure 1 shows the function diagram of this device, and Figure 3 shows typical PD interface power operation sequence.

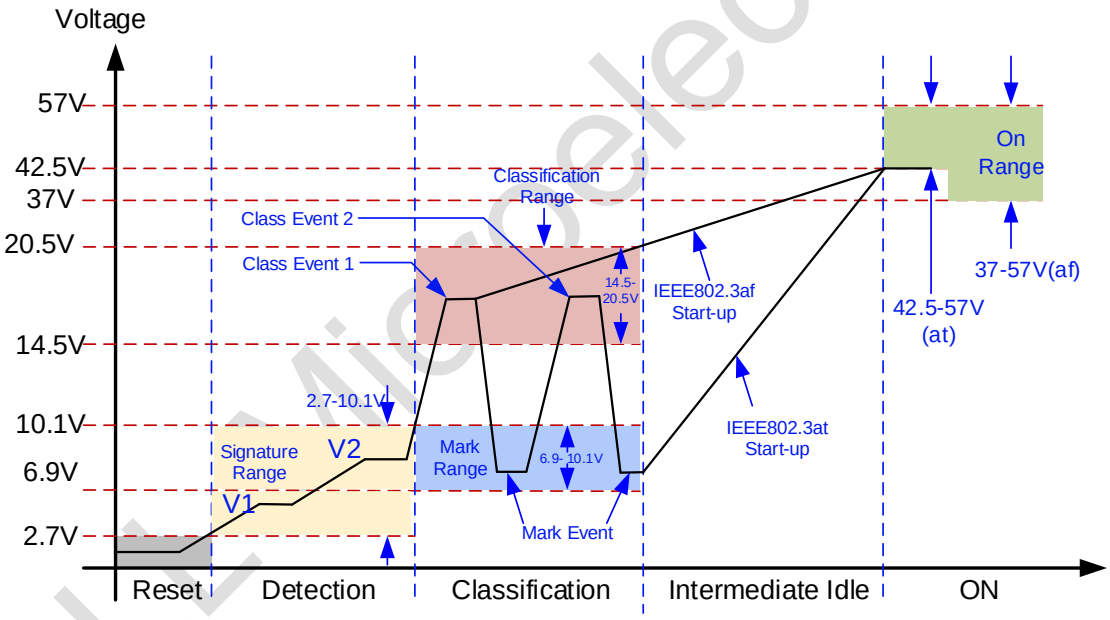


Figure 3 PD Interface Operation Description

Detection

In detection mode, PSE applies two voltages in the range of 1.4V to 10.1V (minimum step size is 1V) to VIN, and records the current measurement values at these two points. Then, PSE calculates DV/DI to ensure that the 24.9kΩ characteristic resistor is connected. Connect a characteristic resistor (R_{DET}) between VDD and DET to ensure correct feature detection. In detection mode, TMI7321 pulls DET low. When the input voltage exceeds 12.5V, DET becomes high impedance. In detection mode, most of the internal circuits of TMI7321 are in the off state, and the bias current is less than 10μA.

Classification

In the classification mode, the PSE classifies the PD according to the power consumption required by the PD, so that the PSE can effectively manage the power allocation. Connect an external resistor (R_{CLS}) between CLS and VSS to set the classification current. The PSE determines the PD level by applying a voltage to the PD input and measuring the current output by the PSE. When the voltage applied by the PSE is between 12.6V and 20V, the TMI7321 feeds back the classification current. PSE uses classification current information to classify PD power requirements. The classification current includes the current drawn by RCLS and the power supply current of TMI7321, so the total current drawn by PD is within the index range of IEEE 802.3 af standard. When the device is in power mode, the classification current is turned off.

Power Mode

When VIN rises above the undervoltage lockout threshold (V_{ON}), TMI7321 enters the power supply mode. When VIN rises above V_{ON}, TMI7321 turns on the internal n-channel isolation MOSFET, connects VSS to RTN, and the internal inrush current limit is set to 150mA. When the voltage at RTN approaches VSS and the inrush current falls below the inrush threshold, the isolation MOSFET is fully turned on. Once the isolation MOSFET is fully turned on, TMI7321 changes the current limit to 450mA. Before the power MOSFET is fully turned on, the power-good open-drain output remains turned off for a duration of at least t_{DELAY} to prohibit subsequent DC-DC converters during the surge.

Undervoltage Lockout

The working voltage of TMI7321 is as high as 57V, the UVLO threshold (V_{ON}) of the circuit is 38.6V; the UVLO threshold (V_{OFF}) of the circuit is 31V. When the input voltage is higher than V_{ON}, TMI7321 enters the power supply mode and the internal MOSFET turns on. When the input voltage is lower than VOFF for more than t_{OFF_DLY}, the MOSFET turns off. The power-good output uses an open-drain output to disable subsequent DC-DC converters before the n-channel isolation MOSFET is fully turned on. Before the internal isolation MOSFET is fully turned on, the PG switch is off, and the hold time is t_{DELAY}. When exiting the thermal shutdown state, the PG switch is also off.

Power Good Indicator (PG)

PG is an active high output that is pulled to VSS when the device is in inrush phase. It remains in a high impedance state at all other times

Maintain Power Signature

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. For IEEE802.3af/at PD, a valid MPS consists of a minimum dc current of 10mA, or a 10mA pulsed current for at least 75ms every 325ms, and an AC impedance lower than 26.3kΩ in parallel with 0.05μF. The TMI7321 has 2 pins can generate MPS pulses, selectable through the MODE input pin. If the current through the RTN-to-VSS path is below ~28mA, the TMI7321 automatically generates the MPS pulsed current through the MPS output pin, the current amplitude being adjustable with an external resistor. MPS is an active low output that is pulled to VSS when the device is in the steady-state power mode. It remains in a high impedance state at all other times.

DCDC Converter Startup and Power Supply

Once PD input overrides its UVLO, it will charge DCDC converter's input capacitor (between VDD and RTN) with PD inrush current limit. DCDC converter has an internal start-up circuit. When voltage between VDD and GND is higher than 3.4V, the capacitor at VCC is charged through the internal LDO. Normally VCC is regulated at 4.5 V (if VDD is high enough). With the exception of PD interface UVLO, the DCDC converter has an additional VIN UVLO (11.5V) and VCC UVLO (3.6V). When VDD-GND is higher than the 11.5V UVLO, VCC is charged higher than the 3.6V UVLO, and PG pin is pulled high by PD interface, DCDC converter starts switching.

VCC can be powered from the transformer auxiliary winding to save IC power loss. Refer to the "VCC Power Supply Setting" section for more details.

Flyback and Buck Mode Converter

The DCDC converter supports both flyback and buck topology applications. Connect MODE to GND to set the DCDC converter in flyback mode, and float MODE to set the DCDC converter in buck mode. MODE is pulled up internally to VCC through a 1.5μA current source. Do not connect MODE to VDD externally in buck mode, and do not place a resistor between MODE and GND in flyback mode.

Converter Switching Work Principle

After startup, DCDC converter works in discontinuous conduction mode (DCM). The second switching cycle will not start until the inductor current drops to 0A. In each cycle, the internal MOSFET is turned on, and the current sense circuit senses the current IP(t) internally.

Use Equation (1) to calculate the rate at which the current rises linearly in flyback mode:

$$\frac{dI_{P(t)}}{dt} = \frac{V_{IN}}{L_M} \quad \text{Equation (1)}$$

When $I_{P(t)}$ rises up to IPK, the internal MOSFET turns off (see Figure 4). The energy stored in the primary-side inductance transfers to the secondary-side through the transformer.

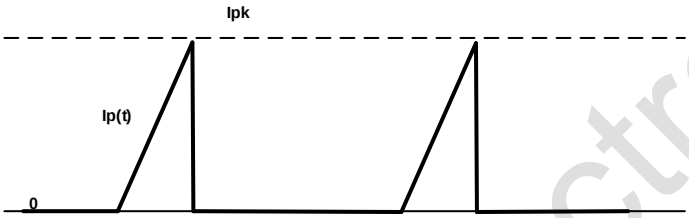


Figure 4 Primary-side current waveform

The primary-side inductance (L_M) stores energy in each cycle as a function of Equation (2):

$$E = \frac{1}{2} L_M I_{PK}^2 \quad \text{Equation (2)}$$

Calculate the power transferred from the input to the output with Equation (3):

$$E = \frac{1}{2} L_M I_{PK}^2 F_S \quad \text{Equation (3)}$$

Where F_S is the switching frequency. When I_{PK} is constant, the output power depends on F_S and L_M.

Use Equation (4) to calculate the rate at which the current rises linearly in buck mode:

$$\frac{dI_{p(t)}}{dt} = \frac{V_{IN} - V_{OUT}}{L_M} \quad \text{Equation (4)}$$

The internal MOSFET turns off when $I_{P(t)}$ rises to I_{PK} (see Figure 5). The output current is calculated with Equation (5):

$$I_{OUT} = \frac{1}{2} D I_{PK} \quad \text{Equation (5)}$$

Where, D is the inductor current conducting duty cycle.

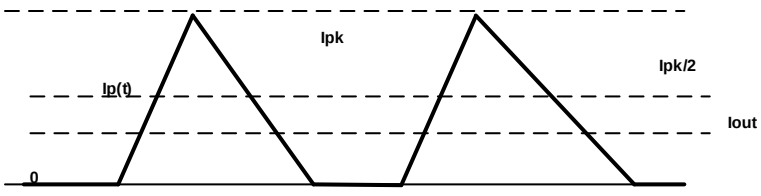


Figure 5 Inductor current waveform

Converter Light-Load Control

In flyback mode (if the load decreases), DCDC converter stretches down the frequency automatically to reduce the power transferring while keeping the same I_{PK} in each cycle. An approximate 10 kHz minimum frequency is applied to detect the output voltage even at a very light load. During this condition, the switching I_{PK} jumps between 20 percent of the normal I_{PK} and 100 percent of the normal I_{PK} to reduce the power transferring. The DCDC converter still transfers some energy to the output even if there is no load on the output due to the 10 kHz minimum frequency. This means that some load is required to keep the output voltage in regulation, or else V_{OUT} will rise and trigger OVP.

In buck mode, the DCDC converter has no minimum frequency limit, so it stretches down to a very low frequency and regulates the output automatically even there is no load on the output.

Frequency Control

By monitoring the auxiliary winding voltage in flyback mode or monitoring the SW voltage in buck mode, the DCDC converter detects and regulates the inductor current in DCM. The frequency is controlled by the peak current, the current ramp slew rate, and the load current. The maximum frequency occurs when the DCDC converter runs in critical conduction mode, providing the maximum load power. The DCDC converter switching frequency should be lower than 300kHz in the design.

Output Voltage Control

In flyback application, the DCDC converter detects the auxiliary winding voltage from FB1 during the secondary-side diode conduction period.

Assume the secondary winding is the master, and the auxiliary winding is the slave. When the secondary-side diode conducts, the FB1 voltage is calculated with Equation (6):

$$V_{FB1} = \frac{N_A}{N_S} \times (V_{OUT} + V_F) \times \frac{R_2}{R_1 + R_2} \quad \text{Equation (6)}$$

Where:

V_F is the output diode forward-drop voltage.

V_{OUT} is the output voltage.

N_A and N_S are the turns of the auxiliary winding and the secondary-side winding, respectively.

R1 and R2 are the resistor dividers for sampling.

The output voltage differs from the secondary winding voltage due to the current-dependant diode forward voltage drop. If the secondary winding voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary-winding voltage is a fixed VD1F. DCDC converter starts sampling the auxiliary-winding voltage after the internal power MOSFET turns off for 0.48μs and finishes the sampling after the secondary-side diode conducts for 1.85μs. This provides good regulation when the load changes. However, the secondary diode conducting period must be longer than 2μs in each cycle, and the FB1 signal must be smooth in 0.48μs after the switch turns off.

With a buck solution, there is one FB2 pin referred to VDD. It can be used as the reference voltage for the buck application. The output voltage is referred to VDD and does not have the same GND as the input power.

Programming the Switching Current Limit

The switching converter current limit is set by an external resistor (R6 in schematic on page 1) from I_{LIM} to ground. The value of R6 can be estimated with Equation (7):

$$I_{LIM} = \frac{118}{R6} + \frac{V_L \times 0.016}{L}$$ Equation (7)

Where I_{LIM} is the current limit in A, V_L is the voltage applied on the inductor when the MOSFET turns on, R6 is the setting resistor in kΩ, and L is the inductor in μH.

The current limit cannot be programmed higher than 3A.

If Input voltage is very low, the inductor current may increase slowly, it will take a long time to meet the setting current limit. TMI7321 integrates a ~7μs max on time. After the max on time, MOSFET will turn off, even the inductor current doesn't meet the setting current limit.

Converter Leading-Edge Blanking

Transformer parasitic capacitance induces a current spike on the switching power FET when the power switch turns on. The DCDC converter includes a 280 ns leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current sense comparator is disabled, and the gate driver cannot switch off.

DCDC Converter DCM Detection

The DCDC switching regulator operates in discontinuous conduction mode in both flyback and buck modes.

In flyback mode, the DCDC converter detects the falling edge of the FB1 voltage in each cycle. The second cycle switching will not start unless the chip detects a 50mV falling edge on FB1.

In buck mode, the DCDC converter detects the falling edge of the SW voltage in each cycle. The second cycle switching will not start unless the chip detects 0.23V falling edge between VSW-VDD.

Over-Voltage & Open-Circuit Protection

In flyback mode, the DCDC converter includes over-voltage protection (OVP) and open-circuit protection. If the voltage at FB1 exceeds 125 percent of V_{REF1}, or FB1's -50mV falling edge cannot be detected because the feedback resistor is removed, immediately the DCDC converter shuts off the driving signal and enters hiccup mode by re-charging the internal capacitor. The DCDC converter resumes normal operation when the fault is removed.

In buck mode, if the voltage at FB2 is higher than the reference voltage, the DCDC converter stops switching immediately.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermally running away. TMI7321 has separated temperature monitor circuit for PD and switching devices, DC converter thermal protection won't affect PD interface but PD temperature protection will turn off both PD and DC converter. When the temperature is lower than its recovery threshold, thermal shutdown is gone and the chip is enabled.

APPLICATION INFORMATION

Detection Resistor

In the Detection Mode, a resistor connected between DET and VDD pin is needed as a load to the PSE. The resistance is calculated as a ΔV/ΔI, with an acceptable range of 23.7kΩ to 26.3kΩ. Use a typical value of 24.9kΩ as detection resistor.

Classification Resistor

In order to distribute power to as many loads as possible from PSE, a resistor between CLASS and VSS pins is used to classify the PD power level, which draws a fixed current set by classification resistor. Typical voltage on CLASS pin is 1.16V in classification range, and it produces about 33mW power loss on class resistor in Class 3 condition.

Protection TVS

To limit input transient voltage within the absolute maximum rating, a TVS across the rectified voltage (VDD-VSS) must be used. A SMAJ58A, or equivalent, is recommended for general indoor applications. Outdoor transient levels or special applications require additional protection.

PD Input Capacitor

An input bypass capacitor (from VDD to VSS) of 0.05μF to 0.12μF is needed for IEEE 802.3af/at standard specification. Typically, a 0.1μF, 100V ceramic capacitor is used.

VCC Power Supply Setting

The VCC voltage is charged through the internal LDO by VDD. Normally, VCC is regulated at 5.4V, typically. A capacitor no less than 1μF is recommended for decoupling between VCC and GND. In flyback mode, VCC can be powered from the transformer auxiliary winding to save the high voltage LDO power loss.

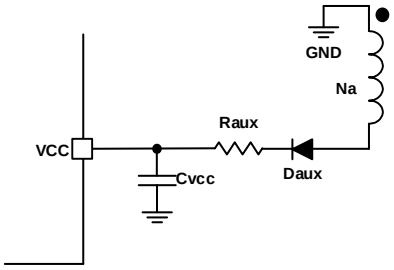


Figure 6 Supply VCC from auxiliary winding

The auxiliary winding supply voltage can be calculated with Equation (8):

$$V_{CC} = \frac{N_A}{N_S} \times (V_{OUT} + V_{D1F}) - V_{DAUXF} \quad \text{Equation (8)}$$

Where N_A and N_S are the turns of the auxiliary winding and the output winding, V_{D1F} is the output rectifier diode voltage drop, and V_{DAUXF} is the DAUX voltage drop in Figure 9.

VCC voltage is clamped at about 6.2V by one internal Zener diode. The clamp current capability is about 1.2mA. If the auxiliary winding power voltage is higher than 6.2V (especially in a heavy-load condition), a series resistor (RAUX) is necessary to limit the current to VCC. For simple application, supply the VCC power through the internal LDO directly.

Converter Output Voltage Setting

In DCDC converter, there are two feedback pins for different application modes.

In flyback mode, the converter detects the auxiliary winding voltage from FB1. R1 and R2 are the resistor dividers for the feedback sampling (see Figure 7)

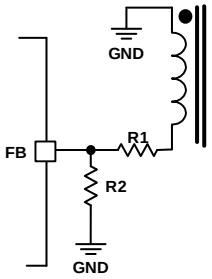


Figure 7 Feedback in isolation application

When the primary-side power MOSFET turns off, the auxiliary-winding voltage is sampled.

The output voltage is estimated:

$$V_{OUT} = \frac{V_{REF1} \times (R_1 + R_2)}{R_2} \times \frac{N_S}{N_A} - V_{D1F} \quad \text{Equation (9)}$$

Where, N_S is the transformer secondary-side winding turns.

N_A is the transformer auxiliary winding turns.

V_{D1F} is the rectifier diode forward drop.

$V_{REF}1$ is the reference voltage of FB1 (1.99V, typically).

When the primary-side power MOSFET turns on, the auxiliary winding forces a negative voltage to FB1. The FB1 voltage is clamped to less than -0.7V internally, but the clamp current should be limited to less than -0.5mA by R1. For example, if the auxiliary winding forces -11V to R1, to make the current flowing from FB1 to R1 lower than -0.5mA, R1 resistance must be higher than 22kΩ (if ignoring R2 current). Generally, select R2 with a 10kΩ to 50kΩ resistor to limit noise and provide an appropriate R1 for the -0.5mA negative current limit.

In buck application, the feedback pin is FB2. The output voltage can be estimated:

$$V_{OUT} = -\frac{R_1 + R_2}{R_2} \times V_{REF2} \quad \text{Equation (10)}$$

Where, V_{REF2} is the reference voltage of FB2 -1.88V, typically.

Maximum Switching Frequency

When DCDC converter works in DCM, the frequency reaches its maximum value during a full-load condition. The maximum frequency is affected by the peak current limit, the inductance, and the input/output voltage. Generally, design the maximum frequency must be lower than 300kHz.

In buck mode, the maximum frequency occurs when the buck runs in critical continuous conduction mode. The frequency can be calculated:

$$F_{SW-MAX} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{I_{LIM} \times L \times V_{IN}}$$ Equation (11)

Where, I_{LIM} is the IPK set by the current limit resistor.

With a lighter load, the frequency is lower than the maximum frequency above.

In flyback mode, design the maximum frequency with the minimum input voltage and the maximum load condition. Calculate the frequency with Equation (12):

$$F_{SW} \le \frac{1}{T_{ON} + T_{CON} + T_{DELAY}}$$ Equation (12)

Where:

T_{ON} is the MOSFET one pulse turn-on time determined with Equation (13):

$$T_{ON} = \frac{I_{LIM} \times L_M}{V_{IN}}$$ Equation (13)

L_M is the transformer primary-winding inductance.

T_{CON} is the rectifier diode current conducting time and can be calculated:

$$T_{CON} = \frac{N_S \times I_{LIM} \times L_M}{N_P \times (V_{OUT} + V_{D1F})}$$ Equation (14)

Where, N_S is the transformer secondary-side winding turns. N_P is the transformer primary side winding turns.

T_{DELAY} is the resonant delay time from the rectifier diode current drop to 0A to the auxiliary-winding voltage drop to 0V. The resonant time can be tested on the board (estimate around 0.5μs).

In flyback mode, the DCDC converter samples the feedback signal within 3μs after the primary-side MOSFET turns off. The secondary-side diode conduction time in Equation (14) should be higher than 3μs. This time period, combined with the duty cycle, determines the maximum frequency.

Converter Input Capacitor Selection

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low ESR capacitor is required to keep the noise to the IC at a minimum. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors will suffice. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The ripple will be the worst at light load. The required input capacitance can be estimated:

$$C_1 = \frac{0.5 \times I_{LIM} \times T_{ON}}{V_{INP\_P}}$$ Equation (15)

Where C1 is the DCDC converter input bulk capacitor value, V_{INP-P} is the expected input ripple, and T_{ON} is the MOSFET turn-on time.

In an isolated application, T_{ON} is calculated:

$$T_{ON} = \frac{I_{LIM} \times L_M}{V_{IN}}$$ Equation (16)

In a non-isolation application, T_{ON} is calculated:

$$T_{ON} = \frac{I_{LIM} \times L}{V_{IN} - V_{OUT}}$$ Equation (17)

Where L is the buck`s inductor value.

Converter Output Capacitor Selection

The output capacitor maintains the DC output voltage. For best results, use ceramic capacitors or low ESR capacitors to minimize the output voltage ripple. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency.

In flyback application, the worst output ripple occurs under a light-load condition; the worst output ripple can be estimated:

$$V_{OUTP\_P} = \frac{0.5 \times N_P \times I_{LIM} \times T_{CON}}{N_S \times C2}$$ Equation (18)

Where, C2 is the output capacitor value. V_{OUTP-P} is the output ripple.

Normally, a 44μF or higher ceramic capacitor is recommended as the output capacitor. This allows a small Vo ripple and stable operation.

In buck application, the worst V_{OUT} ripple can be estimated with Equation (19):

$$V_{OUTP\_P} = \frac{0.5 \times I_{LIM}^2 \times L \times (V_{IN} + V_{D1F})}{C2 \times (V_{IN} - V_{OUT}) \times (V_{IN} + V_{D1F})}$$ Equation (19)

Leakage Inductance

The transformer's leakage inductance decreases system efficiency and affects the output current and voltage precision. Optimize the transformer structure to minimize the leakage inductance. Aim for a leakage inductance less than 3 percent of the primary winding inductance.

RCD Snubber for Flyback

The transformer leakage inductance causes spikes and excessive ringing on the MOSFET drain voltage waveform, affecting the output voltage sampling 0.7μs after the MOSFET turns off. The RCD snubber circuit limits the SW voltage spike (see Figure 8)

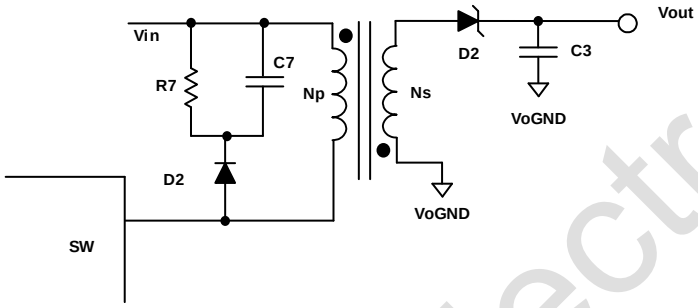


Figure 8 RCD snubber

The power dissipation in the snubber circuit is estimated with Equation (20):

$$P_{SN} = \frac{1}{2} \times L_K \times I_{LIM}^2 \times F_S \quad \text{Equation (20)}$$

Where, L_K is the leakage inductance.

Since R7 consumes the majority of the power, R7 is estimated with Equation (21):

$$R_7 = \frac{V_{SN}^2}{P_{SN}} \quad \text{Equation (21)}$$

Where, V_{SN} is the expected snubber voltage on C7.

The snubber capacitor C47 can be designed to get appropriate voltage ripple on the snubber using Equation (22):

$$\Delta V_{SN} = \frac{V_{SN}}{R_7 \times C_7 \times F_S} \quad \text{Equation (22)}$$

Generally, a 15 percent ripple is acceptable.

Buck Inductor Selection

The inductor is required to transfer the energy between the input source and the output capacitors. Unlike normal application where inductors determine the inductor ripple, the DCDC converter always works in DCM while V_{IN}, V_{OUT}, and I_{LIM} are constant. The inductor only determines the speed of the current rising and falling, which determines the switching period. The expected maximum frequency can determine the inductor value using Equation (23):

$$L \approx \frac{(V_{IN} - V_{OUT}) \times (V_{OUT} - V_{D1F})}{(V_{IN} + V_{D1F}) \times I_{PEAK}} \times \frac{1}{F_{SW}} \quad \text{Equation (23)}$$

F_{SW} is the expected maximum switching frequency, which should be lower than 300kHz in general setting.

Converter Output Diode Selection

The output rectifier diode supplies current to the output capacitor when the internal MOSFET is off. Use a schottky diode to reduce loss due to the diode forward voltage and recovery time.
In isolation application, the diode should be rated for a reverse voltage greater than Equation (24):

$$V_{D1} = V_{OUT} + \frac{V_{IN} \times N_S}{N_P} + V_{PD1} \quad \text{Equation (24)}$$

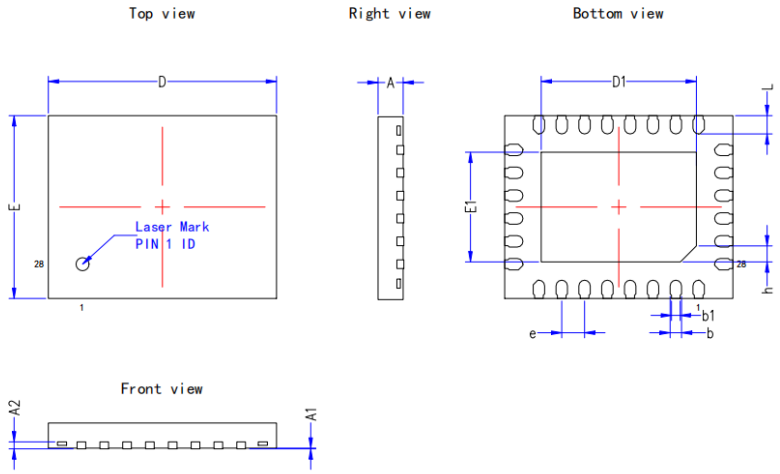
V_{PD1} can be selected at 40 percent to 100 percent of V_{OUT} + V_{IN} x N_S/N_P. An RC or RCD snubber circuit for the output diode D1 is recommended.
In buck mode, the diode reverse voltage equates to the input voltage. A 20 percent ~ 40 percent margin is recommended.
In both applications, the current rating should be higher than the maximum output current.

Converter Dummy Load

When the system operates without a load in flyback mode, the output voltage rises above the normal operation voltage because of the minimum switching frequency limitation. Use a dummy load for good load regulation. A large dummy load decreases efficiency, so the dummy load is a tradeoff between efficiency and load regulation.

Package Information

QFN4x5-28



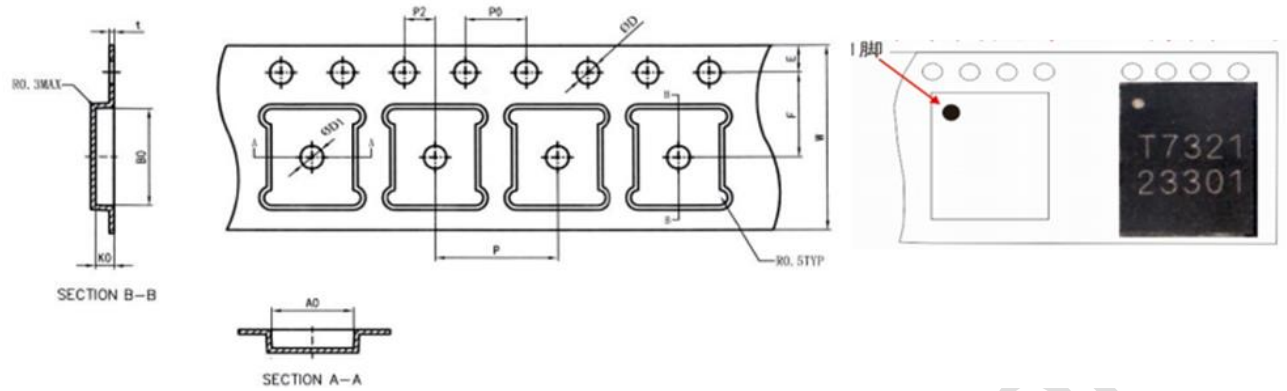
	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.70	0.75	0.80
STAND OFF	A1	0.00	0.02	0.05
L/F THICKNESS	A2		0.203REF	
LEAD WIDTH	b	0.20	0.25	0.30
LEAD REAR WIDTH	b1		0.19REF	
BODY SIZE X	D	4.90	5.00	5.10
EP SIZE X	D1	3.50	3.65	3.80
BODY SIZE Y	E	3.90	4.00	4.10
EP SIZE Y	E1	2.5	2.65	2.80
LEAD PITCH	e		0.50BSC	
LEAD LENGTH	L	0.35	0.40	0.45
CHAMFER	h	0.30	0.35	0.40
LF PAD SIZE	X	3.90	Y	2.90

Note:

1) All dimensions are in millimeters.
2) 2) Package length does not include mold flash, protrusion or gate burr.
3) 3) Package width does not include inter lead flash or protrusion.

Tape And Reel Information

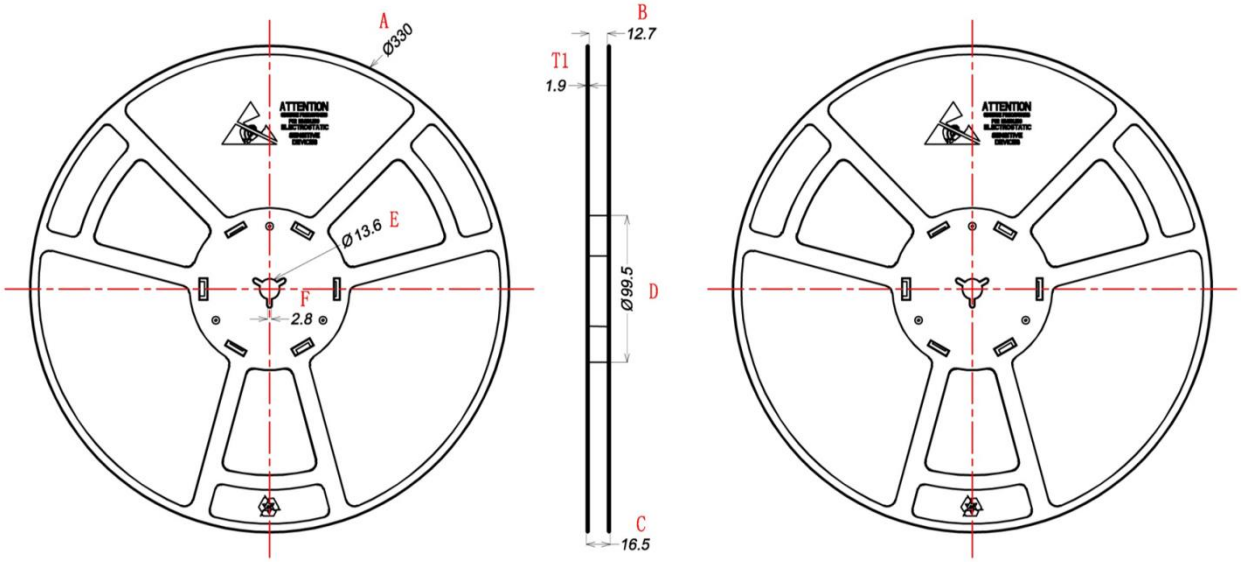
TAPE DIMENSIONS:QFN 4*5-28



Unit: mm

E	F	P2	D	D1	P0
1.7±0.10	5.50±0.05	2.00±0.05	$1.50^{+0.20}_{-0}$	1.50MIN2	4.00±0.10
W	P	A0	B0	K0	t
$12.0^{+0.20}_{-0.10}$	8.0±0.10	4.3±0.10	5.3±0.10	1.2±0.10	0.3±0.05

REEL DIMENSIONS:



Unit: mm

A	B	C	D	E	F	T1
Ø 330±1	12.7±0.5	16.5±0.3	Ø 99.5±0.5	Ø 13.6±0.2	2.8±0.2	1.9±0.2

Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 5000
3) MSL level is level 3.

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