MSQ30P07D

Dual P-Channel 30-V (D-S) MOSFET

Description

The device is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The device meets the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- $R_{DS(ON)}$ =28mΩ@ V_{GS} =-10V
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

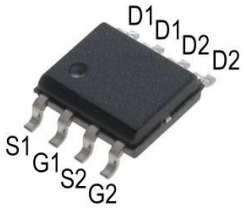
Typical Applications

- MB / VGA / Vcore
- POL Applications
- Load Switch
- LED Applications

Package type：SOP-8

Packing & Order Information

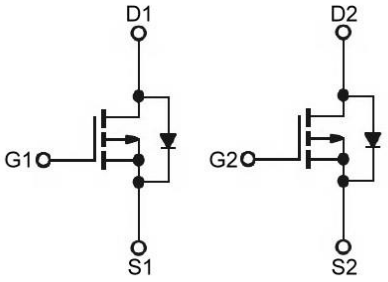
3,000/Reel



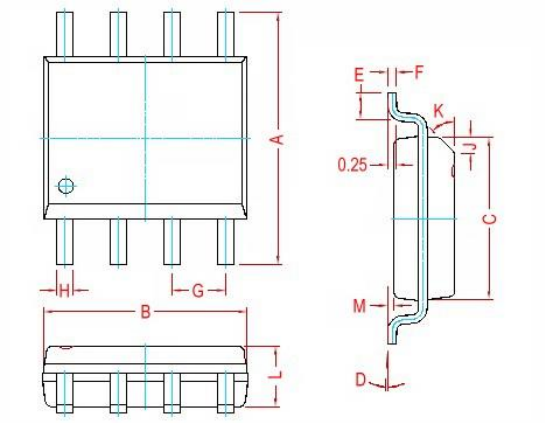
AEC-Q101
Qualification Available

RoHS Compliant

Graphic Symbol

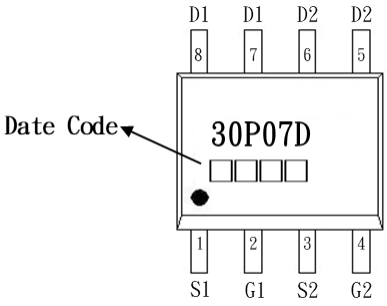


Package Dimension



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.51
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.40 Ref.	
E	0.40	0.90	K	45° Ref.	
F	0.19	0.26	G	1.27 Typ.	

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current[1] (T_A=25°C)	-6.5	A
	Continuous Drain Current[1] (T_A=70°C)	-5.2	A
I_{DM}	Pulsed Drain Current[1,2]	-26	A
I_{AS}	Single Pulse Avalanche Current, L =0.1mH[3]	-38	A
E_{AS}	Single Pulse Avalanche Energy, L =0.1mH[3]	72	mJ
P_D	Power Dissipation[4] (T_A=25°C)	1.5	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	°C

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient[1]	85	°C/W
$R_{\theta JC}$	Maximum Junction-to-Case[1]	25	°C/W

Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.0	-	-2.5	V
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30	-	-	V
g_{fs}	Forward Transconductance	V_{DS}=-5V, I_D=-6A	-	17	-	S
I_{GSS}	Gate-Source Leakage Current	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V, V_{GS}=0V, T_J=25°C	-	-	-1	μA
		V_{DS}=-24V, V_{GS}=0V, T_J=55°C			-5	
$R_{DS\ (on)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-6A	-	-	28	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	-	35	
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=-25V, L =0.1mH, I_{AS}=-13A	8.4		-	mJ
V_{SD}	Diode Forward Voltage[2]	I_S=-6.5A, V_{GS}=0V, T_J=25°C	-	-	-1.2	V
I_S	Continuous Source Current[1,6]	V_G=V_D=0V, Force Current	-	-	-6.5	A
I_{SM}	Pulsed Source Current[2,6]		-	-	-26	

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Dynamic						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Q_g	Total Gate Charge[2]	V_{DS} =-15V I_D =-6A V_{GS} =-4.5V	--	12.6	--	nC
Q_{gs}	Gate-Source Charge		--	4.8	--	
Q_{gd}	Gate-Drain Charge		--	4.8	--	
$t_{d(on)}$	Turn-On Delay Time[2]	V_{DS} =-15V I_D =-6A V_{GS} =-10V R_G =3.3Ω	--	4.6	--	ns
t_r	Rise Time		--	14.8	--	
$t_{d(off)}$	Turn-Off Delay Time		--	41	--	
t_f	Fall Time		--	19.6	--	
C_{iss}	Input Capacitance	V_{DS} =-15V V_{GS} =0V f =1.0MHz	--	1345	--	pF
C_{oss}	Output Capacitance		--	194	--	
C_{rss}	Reverse Transfer Capacitance		--	158	--	
Rg	Gate Resistance	V_{GS} =V_{DS} =0V, f =1.0MHz	--	13	--	Ω

Notes

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows maximum rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-38A.
4. The power dissipation is limited by 150℃ junction temperature.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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- **Typical Electrical Characteristics**

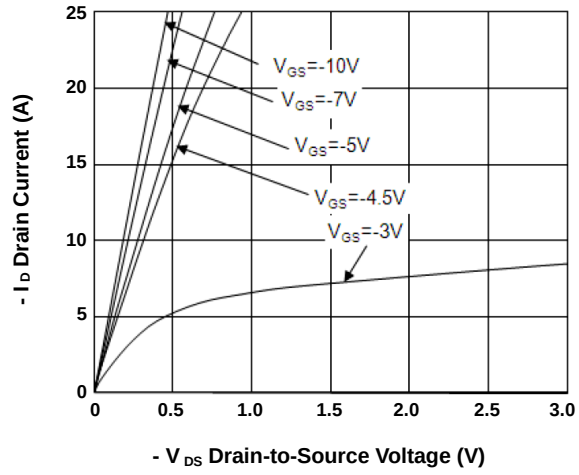

FIG.1-Typical Output Characteristics

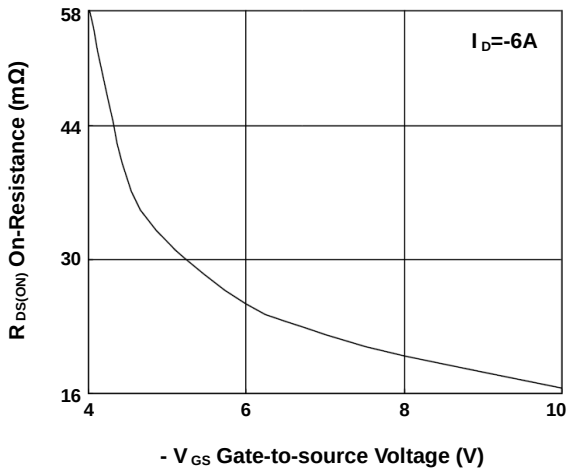

FIG.2-On-Resistance vs. G-S Voltage

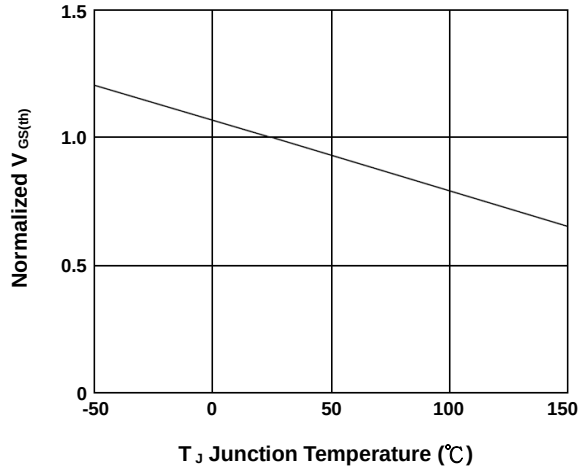

FIG.3-Normalized $V_{GS(th)}$ vs. T_J

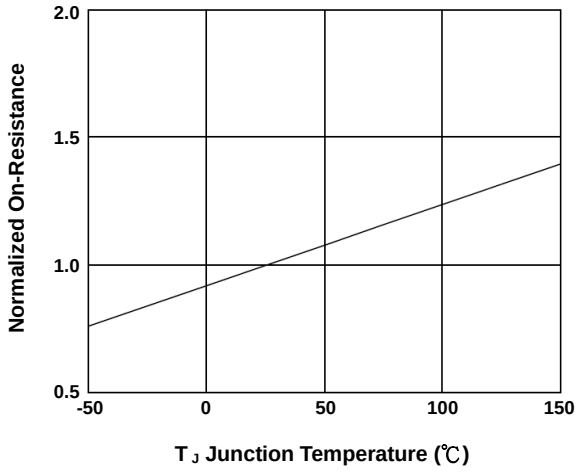

FIG.4-Normalized R_{DSON} vs. T_J

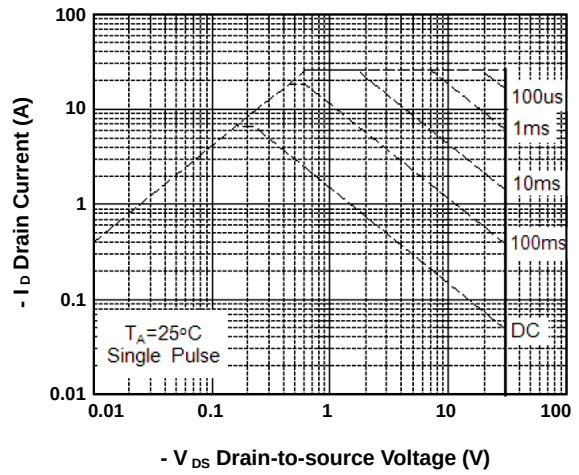

FIG.5-Safe Operating Area

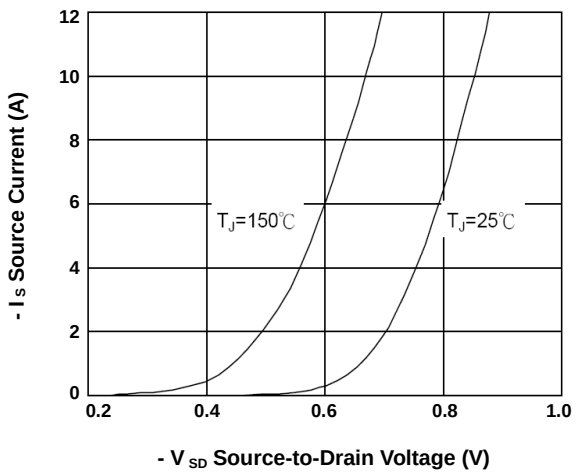

FIG.6-Forward Characteristics of Reverse

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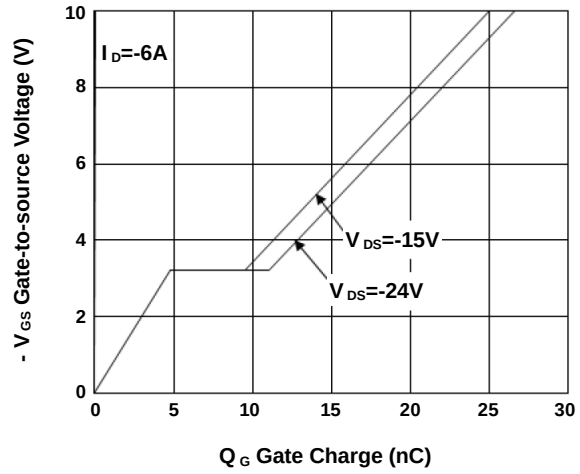

FIG.7-Gate Charge Characteristics

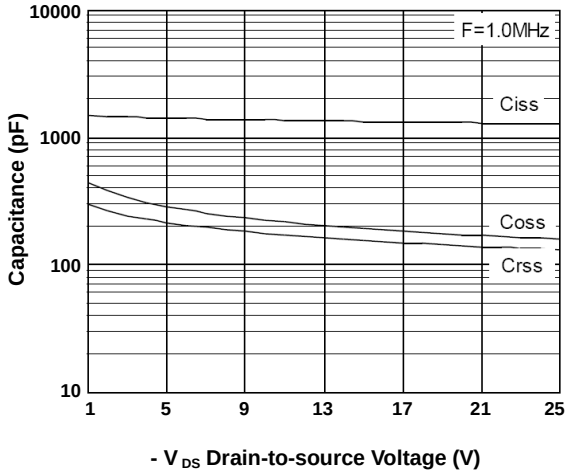

FIG.8-Capacitance Characteristics

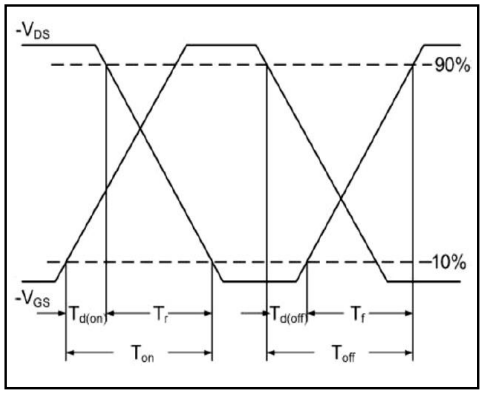

FIG.9-Switching Time Waveform

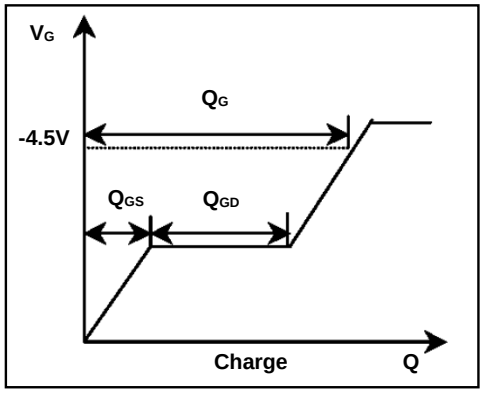

FIG.10-Gate Charge Waveform

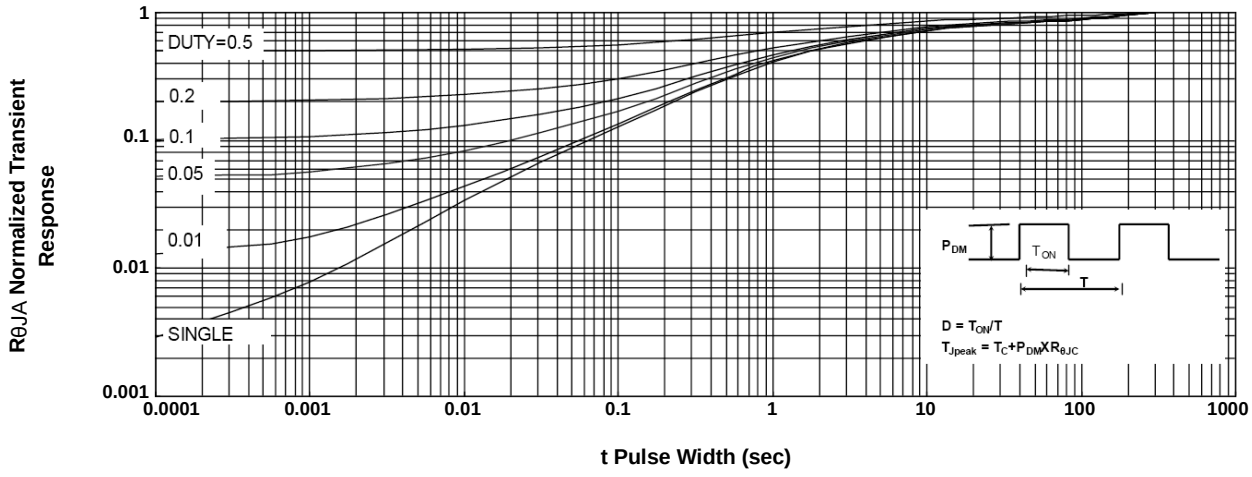

FIG.11-Normalized Maximum Transient Thermal Impedance

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