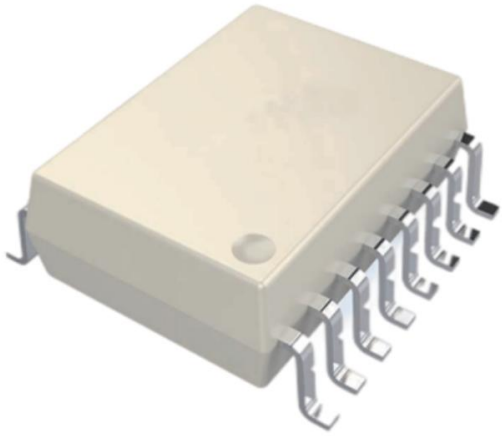
AOTE
SEMICONDUCTOR



栅极驱动光耦
Gate Drive Optocoupler

AT332J

Product Data Sheet

AOTE DCC
RELEASE

台湾奥特半导体科技有限公司

TAIWAN AOTE SEMICONDUCTOR TECHNOLOGY CO.,LTD

www.aotesemi.com

概述 Description

AT332J 具有一个 AlGaAs LED。 LED 与具有功率输出级的集成电路光学耦合。AT332J 非常适合驱动电机控制逆变器应用中的功率 IGBTs 和 MOSFETs。这些光电耦合器提供的电压和电流使其非常适合直接驱动额定值高达 1200 V 和 150 A 的 IGBTs。对于更高功率等级的 IGBTs，AT332J 可用于驱动由分离器件构成的 IGBTs 门极驱动器。AT332J 的绝缘电压 V_{IORM}=1230V_{PEAK}。

The AT332J contains a AlGaAs LED. The LED is optically coupled to an integrated circuit with a power output stage. AT332J are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTs with ratings up to 1200 V and 150 A. For IGBTs with higher ratings, the AT332J can be used to drive a discrete power stage which drives the IGBT gate. The AT332J has an insulation voltage of V_{IORM} = 1230V_{PEAK}.

特性 Features

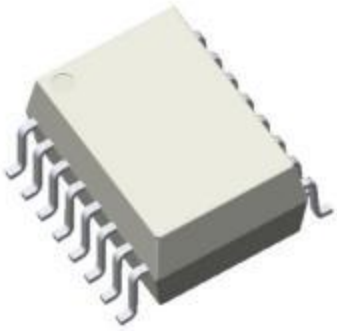
- 最大输出峰值电流: 2.5A
  2.5A maximum peak output current
- 最小输出峰值电流: 2.0A
  2.0A minximum peak output current
- 最大传播延迟: 250ns
  250ns maximum propagation delay
- 饱和度侦测
  Desaturation Detection
- 米勒钳位
  Miller clamping
- 1.7A 的米勒钳位， 该脚不用时必须和 V_{EE} 短接
  1.7A Miller Clamp, clamp pin short to V_{EE} if not used
- 滞后的欠压锁定保护 （UVLO)
  Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- 隔离的开路集电极故障反馈
  Open Collector Isolated fault feedback
- SO-16 封装
  Available in SO-16 package
- 100ns 最大脉宽失真 （PWD)
  100ns maximum pulse width distortion (PWD)
- 最小共模抑制比(CMR)： 50kV/μs （V_{CM} = 1500V)
  50kV/μs minimum common mode rejection (CMR) at V_{CM} = 1500V
- 最大供电电流 $I_{CC(max)}$< 4.5mA
  $I_{CC(max)}$ < 4.5mA maximum supply current
- V_{CC} 工作范围: 15 V ~ 30 V
  Wide V_{CC} operating range: 15 V to 30 V
- 工作温度: –40°C ~ +110°C
  Operating Temperature: –40°C to +110°C
- IGBT 软关断
  “Soft” IGBT Turn-off
- 符合 AEC-Q101 车规标准
  Meet AEC-Q101 vehicle regulation level standard

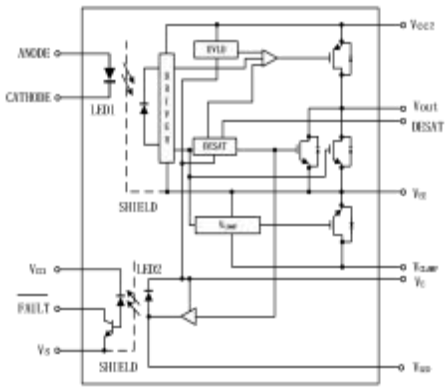
- 安全和监管批准
  Safety and regulatory approvals
  —CQC 认证： GB 4943.1-2022（编号： CQC22001352993)
  CQC approved: GB 4943.1-2022（NO: CQC22001352993)
  —UL 认证： UL1577(编号： UL-US-2236520-0)
  UL approved: UL1577（NO: UL-US-2236520-0)
  —VDE 认证： DIN EN IEC 60747-5-5 (VDE 0884-5): 2021-10; EN IEC 60747-5-5: 2020（编号： 40051490)
  VDE approved: DIN EN IEC 60747-5-5 (VDE 0884-5): 2021-10; EN IEC 60747-5-5: 2020（NO: 40051490)

应用 Applications

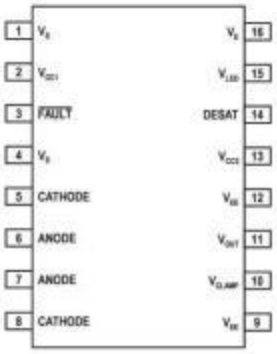
- 隔离型 IGBT 或隔离型功率 MOSFET 的栅极驱动
  Isolated IGBT/ Power MOSFET gate drive
- 交流和直流无刷电机驱动器
  AC and brushless DC motor drives
- 工业逆变器
  Industrial inverter
- 不间断电源
  Uninterruptible Power Supply (UPS)

封装和原理图 Package and Schematic Diagram





引脚说明 Pin Description



引脚 Pin	符号 Symbol	描述 Description	
1	V_S	输入地	Input Ground
2	V_{CC1}	正向输入电源电压 (3.3V ~ 5.5V)	Positive input supply voltage (3.3V to 5.5V)
3	$\overline{FAULT}$	故障输出。当 DESAT 脚超出内部参考电压 7V 时，FAULT 脚将输出一个开路集电极的信号， 在 5us 内 FAULT 脚将从高阻状态转变成一个逻辑低电平。在同一电路的单个的 FAULT 脚以“或”逻辑连接成一条母线到单片机。	Fault output. $\overline{FAULT}$ changes from a high impedance State to a logic low output within 5 μs of the voltage on The DESAT pin exceeding an internal reference voltage of 7V. $\overline{FAULT}$ output is an open collector which allows the $\overline{FAULT}$ outputs from all AT332J in a circuit to be connected together in a “wired OR” forming a single fault bus for inter facing directly to the micro-controller.
4	V_S	输入地	Input Ground
5	CATHODE	阴极	Cathode
6	ANODE	阳极	Anode
7	ANODE	阳极	Anode
8	CATHODE	阴极	Cathode
9	V_{EE}	输出电源电压	Output supply voltage.
10	V_{CLAMP}	米勒钳位	Miller clamp
11	V_{OUT}	栅极驱动电压输出	Gate drive voltage output
12	V_{EE}	输出电源电压。	Output supply voltage.
13	V_{CC2}	正向输出电源电压	Positive output supply voltage
14	DESAT	去饱和电压输入引脚。当 DESAT 脚电压在 IGBT 导通时超过内部参考电压 6.5V 时， 故障输出端将在 5us 内从高阻状态转变成一个逻辑低电平	Desaturation voltage input. When the voltage on DESAT exceeds an internal reference voltage of 6.5V while the IGBT is on, $\overline{FAULT}$ output is changed from a high impedance state to a logic low state within 5 μs.
15	V_{LED}	LED 阳极。为了保证数据表性能， 此引脚必须保持不连接。(仅用于光耦测试)	LED anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only)
16	V_E	通用(IGBT 发射极)输出电源电压	Common (IGBT emitter) output supply voltage.

产品型号命名规则 Order Code

AT 332J - UN Y - W (V) (ZZ)

① ② ③ ④ ⑤ ⑥ ⑦

① 公司代码 Company Code（AT: 奥特 Aote）

② 产品系列 Product Series（332J: 332J）

③ 框架类型 Lead Frame（Cu: 铜框架 Copper）

④ 树脂类型 Epoxy（H: 无卤 Halogen-free, L: 有卤/无铅 Halogen/Lead-free）

⑤ 封装形式 Package（S: SOP）

⑥ 器件工作温度范围 Device Operating Temperature Range（特殊范围需填或者空白 Special Range or None）

⑦ 内部补充代码 Internal Supplementary Code（数字或者空白 Number or None）

印字信息 Marking Information

- 印字中“ ”为奥特品牌 LOGO
  “ ” denotes LOGO
- 印字中“Y”代表年份： A(2018), B(2019), C(2020) … ...
  “Y” denotes YEAR： A(2018), B(2019), C(2020) … ...
- 印字中“WW”代表周号
  ‘WW’ denotes Week’ s number
- 印字中“E”代表内部代码
  “E” denotes Internal code
- 第二行印字中的“H”代表无卤， 而当产品有卤/无铅时， 此处空白
  In the second line, “H” denotes Halogen-free, when the product has halogen/lead-free, leave this blank.

绝缘和安规信息 Insulation and Safety related specifications

项目 Item	符号 Symbol	数值 Value	单位 Unit	备注 Note
爬电距离 Creepage Distance	L	8.3	mm	从输入端到输出端， 沿本体最短距离路径 Measured from input terminals to output terminals, shortest distance path along body.
电气间隙 Clearance Distance	L	8.3	mm	从输入端到输出端， 通过空气的最短距离 Measured from input terminals to output terminals, shortest distance through air.
绝缘距离 Insulation Thickness	DTI	0.5	mm	发射器和探测器之间的绝缘厚度 Insulation thickness between emitter and detector.
峰值隔离电压 Maximum Working Insulation Voltage	V_{IORM}	1500	V_{peak}	IEC/EN/DIN EN60747-5-5.
瞬态隔离电压 Highest Allowable Overvoltage	V_{IOTM}	8000	V_{peak}	IEC/EN/DIN EN60747-5-5.
隔离电压 Isolation Voltage	V_{ISO}	5000	V_{rms}	For 1 minute.

极限参数 Absolute Maximum Ratings

参数 Parameter	符号 Symbol	最小值 Min	最大值 Max	单位 Unit
储存温度 Storage Temperature	T_S	-55	+125	°C
工作环境温度 Operating Temperature	T_A	-40	+110	
IC 结温 Output IC Junction Temperature	T_J	-40	+125	
输出峰值电流 Peak Output Current	I_{OP}	2.5		A
平均输入电流 Average Input Current	$I_{F(AVG)}$	-	25	mA
瞬态输入峰值电流 (< 1 μs 脉冲宽度， 300pps) Peak Transient Input Current, (<1 μs pulse width, 300pps)	$I_{F(TRAN)}$	-	1.0	A
反向输入电压 Reverse Input Voltage	V_R	-	5	V
高电平输出峰值电流 “High” Peak Output Current	$I_{OH(PEAK)}$	-	2.5	A
低电平输出峰值电流 “Low” Peak Output Current	$I_{OL(PEAK)}$	-	2.5	A
正向输入电源电压 Positive Input Supply Voltage	V_{CC1}	-0.5	7.0	V
故障输出电流 FAULT Output Current	$I_{\overline{FAULT}}$	-	8.0	mA
故障端电压 FAULT Pin Voltage	$V_{\overline{FAULT}}$	-0.5	V_{CC1}	V

参数 Parameter	符号 Symbol	最小值 Min	最大值 Max	单位 Unit
总输出电源电压 Total Output Supply Voltage	(V_{CC2} - V_{EE})	-0.5	35	V
总输出电源电压(T_A ≥90℃) Total Output Supply Voltage		-0.5	30	V
负输出电源电压 Negative Output Supply Voltage	(V_E - V_{EE})	-0.5	15	V
正输出电源电压 Positive Output Supply Voltage	(V_{CC2} - V_E)	-0.5	30	V
栅极驱动输出电压 Gate Drive Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC2}	V
钳位峰值电流 Peak Clamping Sinking Current	I_{Clamp}	-	1.7	A
米勒钳位引脚电压 Miller Clamping Pin Voltage	V_{Clamp}	-0.5	V_{CC2}	V
DESAT 电压 DESAT Voltage	V_{DESAT}	V_E	V_E+10	V
IC 输出功耗 Output IC Power Dissipation	P_O	-	600	mW
IC 输入功耗 Input IC Power Dissipation	P_I	-	150	mW

推荐的操作条件 Recommended Operating Conditions

参数 Parameter	符号 Symbol	最小值 Min	最大值 Max	单位 Unit
工作温度 Operating Temperature	T_A	-40	+110	°C
输入电压 (OFF) Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V
输入电流 (ON) Input Current (ON)	$I_{F(ON)}$	7	16	mA
总输出电源电压 Total Output Supply Voltage	(V_{CC2} - V_{EE})	15	30	V
负输出电源电压 Negative Output Supply Voltage	(V_E - V_{EE})	-0.5	15	V
正输出电源电压 Positive Output Supply Voltage	(V_{CC2} - V_E)	-0.5	30 - (V_E - V_{EE})	A

产品特性参数 Electro-optical Characteristics

除非另有说明， 典型值测量值在 T_A =25°C, V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V 测得； 所有的最小/最大规格遵照推荐工作条件。

Unless otherwise noted, all typical values at T_A =25°C, V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V; All Minimum/Maximum specifications are at Recommended Operating Conditions.

参数 Parameter	符号 Symbol	条件 Condition	最小 Min.	典型 Typ.	最大 Max.	单位 Unit	备注 Note
故障逻辑低输出电压 $\overline{FAULT}$ Logic Low Output Voltage	$V_{\overline{FAULTL}}$	$I_{\overline{FAULT}}$ = 1.1mA, V_{CC1} = 5.5V	-	0.1	0.4	V	-
		$I_{\overline{FAULT}}$ = 1.1mA, V_{CC1} = 3.3V	-	0.1	0.4	V	-
故障逻辑高输出电流 $\overline{FAULT}$ Logic High Output Current	$I_{\overline{FAULTH}}$	$V_{\overline{FAULT}}$ = 5.5V, V_{CC1} = 5.5V	-	0.02	0.5	μA	-
		$V_{\overline{FAULT}}$ = 3.3 V, V_{CC1} = 3.3V	-	0.002	0.3	μA	-
高电平输出电流 High Level Output Current	I_{OH}	V_O = V_{CC2} – 4	-0.5	-1.5	-	A	2,4,21
		V_O = V_{CC2} –15	-2.0	-	-	A	
低电平输出电流 Low Level Output Current	I_{OL}	V_O = V_{EE} + 2.5	0.5	1.5	-	A	3,5,22
		V_O = V_{EE} + 15	2.0	-	-	A	
故障条件下低电平输出电流 Low Level Output Current During Fault Condition	I_{OLF}	V_{OUT} - V_{EE} = 14V	90	140	230	mA	-
高电平输出电压 High Level Output Voltage	V_{OH}	I_O = -650μA	V_{CC}-0.3	V_{CC}-0.1	-	V	4,6,23
低电平输出电压 Low Level Output Voltage	V_{OL}	I_O = 100mA	-	0.17	0.5	V	5,7,24
钳位端阈值电压 Clamp Pin Threshold Voltage	V_{tClamp}	-	-	-	2.5	V	-
低电平钳位电流 Clamp Low Level Sinking Current	I_{CL}	V_O = V_{EE} + 2.5	0.5	1.1	-	A	8

参数 Parameter	符号 Symbol	条件 Condition	最小 Min.	典型 Typ.	最大 Max.	单位 Unit	备注 Note
高电平电源电流 High Level Supply Current	I_{CC2H}	I_O = 0mA	-	2.4	4.5	mA	9, 10 25, 26
低电平电源电流 Low Level Supply Current	I_{CC2L}	I_O = 0mA	-	2.4	4.5	mA	
极间耦合电容充电电流 Blanking Capacitor Charging Current	I_{CHG}	V_{DESAT} = 2V	-0.13	-0.24	-0.33	mA	11, 27
极间耦合电容放电电流 Blanking Capacitor Discharge Current	I_{DSCHG}	V_{DESAT} = 7.0V	10	30	-	mA	28
DESAT 阈值 DESAT Threshold	V_{DESAT}	V_{CC2} -V_E >V_{UVLO-}	6	6.5	7.5	V	12
UVLO 阈值 UVLO Threshold	V_{UVLO+}	I_F = 10mA , V_O > 5 V	10.5	11.6	12.5	V	-
	V_{UVLO-}	I_F = 10mA , V_O < 5 V	9.2	10.3	11.1	V	-
UVLO 迟滞 UVLO Hysteresis	(V_{UVLO+} - V_{UVLO-})	-	-	1.3	-	V	-
由低至高的输入阈值电流 Threshold Input Current Low to High	I_{FLH}	I_O = 0mA, V_O > 5 V	-	2.0	5.0	mA	-
由高到低的输入阈值电压 Threshold Input Voltage High to Low	V_{FHL}	I_O = 0mA, V_O < 5 V	0.8	-	-	V	-
输入正向电压 Input Forward Voltage	V_F	I_F = 10mA	1.2	1.6	1.95	V	-
正向输入电压的温度系数 Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	-	-	-1.3	-	mV/°C	-
反向输入击穿电压 Input Reverse Breakdown Voltage	B_{VR}	I_R = 10A	5		-	V	-
输入电容 Input Capacitance	C_{IN}	f = 1MHz, V_F = 0V	-	70	-	pF	-

开关规格 Switching Specifications

除非另有说明， 典型值测量值在 T_A =25℃, V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V 测得； 所有的最小/最大规格遵照推荐工作条件。

Unless otherwise noted, all typical values at T_A =25℃, V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V; All Minimum/Maximum specifications are at Recommended Operating Conditions.

参数 Parameter	符号 Symbol	条件 Condition	最小 Min.	典型 Typ.	最大 Max.	单位 Unit	备注 Note
高电平输出的传输延迟时间 Propagation Delay Time to High Output Level	t_{PLH}	Rg = 10 Ω, Cg = 10nF, f = 10 kHz, Duty Cycle = 50%, I_F = 10mA, V_{CC2} = 30 V	50	180	250	ns	1,13,14, 15,16,29
低电平输出的传输延迟时间 Propagation Delay Time to Low Output Level	t_{PHL}		50	180	250	ns	
脉冲宽度失真 Pulse Width Distortion	PWD		-80	30	80	ns	-
任意两个部件或信道之间的传输延迟差 Propagation Delay Difference Between Any Two Parts or Channels	P_{DD}		-100	-	100	ns	-
上升时间 Rise Time	t_r		-	50	-	ns	-
下降时间 Fall Time	t_f		-	50	-	ns	
DESAT 翻转到 VO 降至 90%之间的延迟时间 DESAT Sense to 90% VO Delay	$t_{DESAT\ (90\%)}$	C_{DESAT} = 100pF, Rg = 10 Ω, Cg = 10nF, V_{CC2} = 30 V	-	0.25	0.5	μs	17,30 35
DESAT 翻转到 VO 降至 10%之间的延迟时间 DESAT Sense to 10% VO Delay	$t_{DESAT\ (10\%)}$	C_{DESAT} = 100pF, Rg = 10 Ω, Cg = 10nF, V_{CC2} = 30 V	-	2	3	μs	18,19 20,30 35
DESAT 翻转到低电平故障信号输出的延迟时间 DESAT Sense to Low Level FAULT Signal Delay	$t_{DESAT\ (FAULT)}$	C_{DESAT} = 100pF, R_F = 2.1kΩ, C_F = Open, Rg = 10 Ω, Cg = 10nF, V_{CC2} = 30 V	-	0.25	0.5	μs	30,35
DESAT 翻转到 DESAT 低电平传播延迟时间 DESAT Sense to DESAT Low Propagation Delay	$t_{DESAT\ (LOW)}$	C_{DESAT} = 100pF, R_F = 2.1kΩ, Rg = 10 Ω, Cg = 10nF, V_{CC2} = 30 V	-	0.25	-	μs	30,35
DESAT 输入静音时间 DESAT Input Mute	$t_{RESET\ (MUTE)}$	-	5	15	-	μs	35
故障信号复位至高电平的延迟时间 RESET to High Level FAULT Signal Delay	$t_{RESET\ (FAULT)}$	C_{DESAT} = 100pF, R_F = 2.1kΩ, Rg = 10 Ω, Cg = 10nF, V_{CC1} = 5.5V, V_{CC2} = 30 V	-	1	2.0	μs	-

参数 Parameter	符号 Symbol	条件 Condition	最小 Min.	典型 Typ.	最大 Max.	单位 Unit	备注 Note
高电平输出的共模抑制能力 Output High Level Common Mode Transient Immunity	$\|CM_H\|$	T_A = 25°C, I_F = 10mA V_{CM} = 1500 V, V_{CC2} = 30 V, R_F = 2.1kΩ, C_F = 15pF	15	25	-	kV/μs	31,32 33,34
		T_A = 25°C, I_F = 10mA V_{CM} = 1500 V, V_{CC2} = 30 V, R_F = 2.1kΩ, C_F = 1nF	50	60	--		
低电平输出的共模抑制能力 Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	T_A = 25°C, V_F = 0 V V_{CM} = 1500 V, V_{CC2} = 30V, R_F = 2.1kΩ, C_F = 15pF	15	25	-	kV/μs	31,32, 33,34
		T_A = 25°C, V_F = 0 V V_{CM} = 1500 V, V_{CC2} = 30 V, R_F = 2.1kΩ, C_F = 1nF	50	60	-		

典型光电特性曲线 Typical Characteristics Curves

Fig.1 V_{OUT} Propagation Delay Waveforms

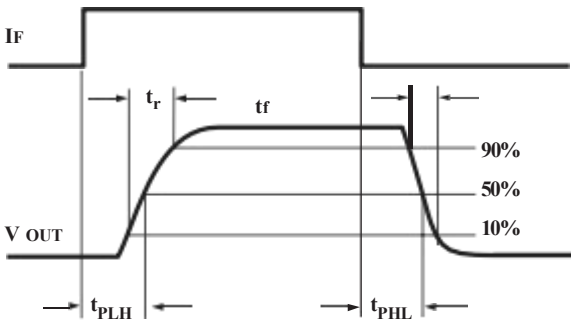


Fig.2 Output High Current vs. Ambient Temperature

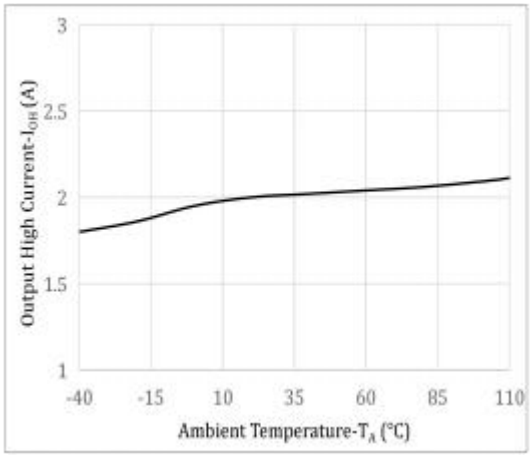


Fig.3 Output Low Current vs. Ambient Temperature

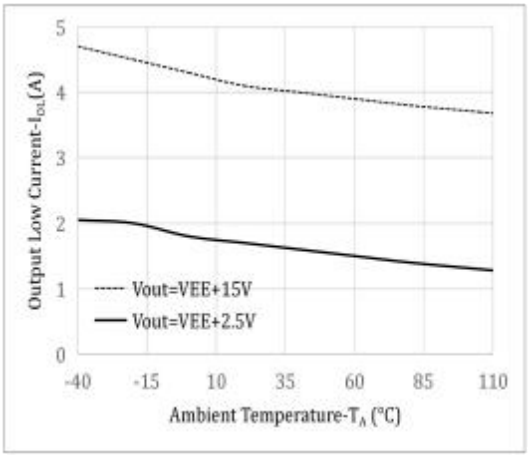


Fig.4 High Output Voltage Drop vs. Ambient Temperature

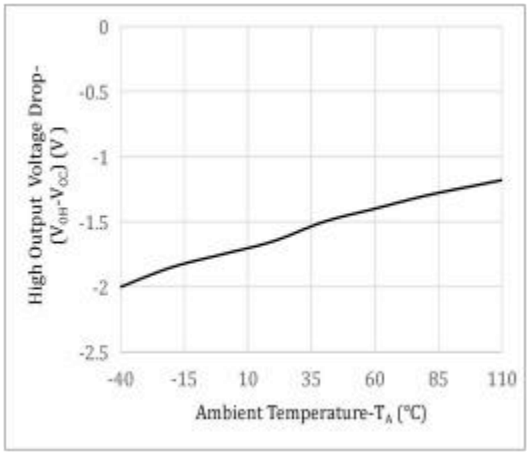


Fig.5 Output Low Voltage vs. Ambient Temperature

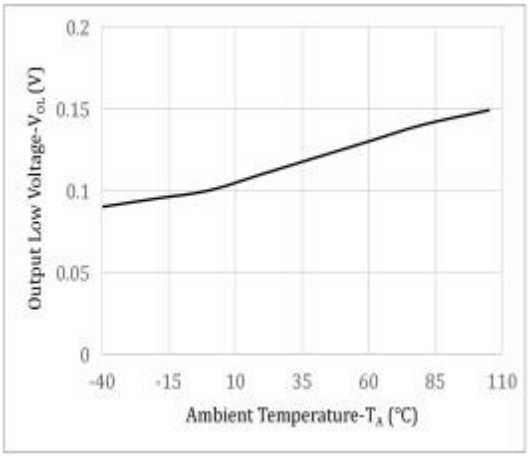


Fig.6 High Output Voltage vs. Output High Current

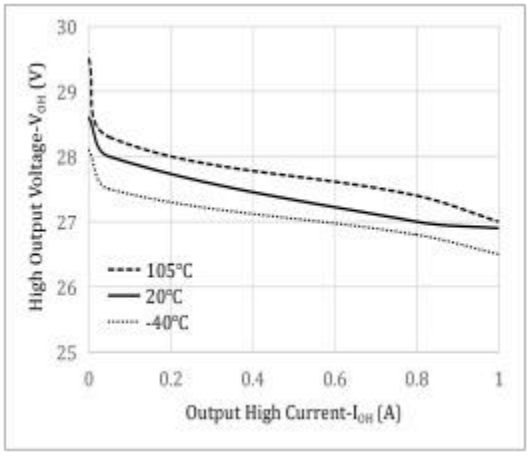


Fig.7 Low Output Voltage vs. Output Low Current

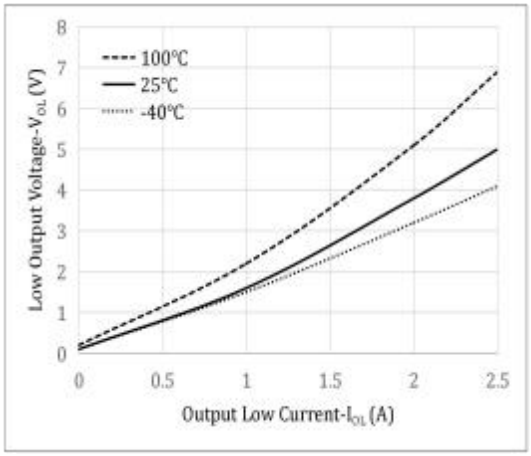


Fig.8 Clamp Low Level Sinking Current vs. Ambient Temperature

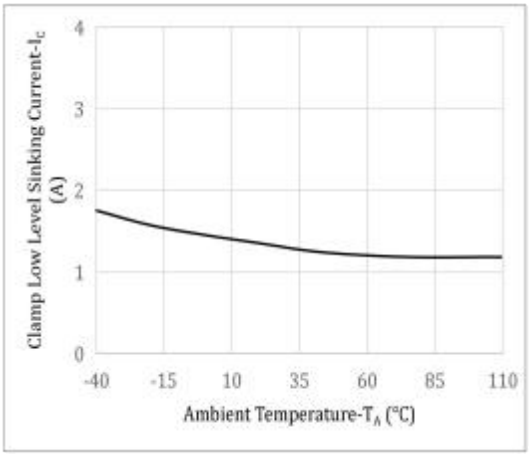


Fig.9 Output Supply Current vs. Ambient Temperature

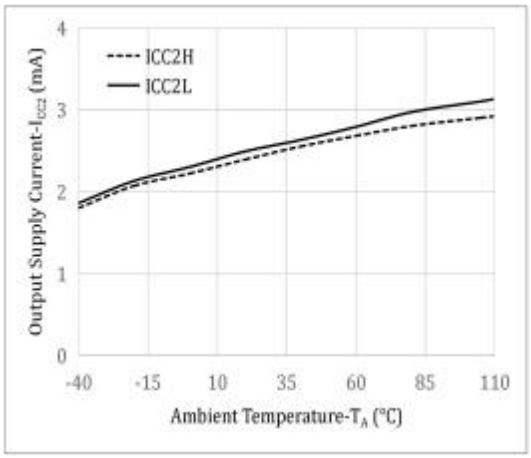


Fig.10 Output Supply Current vs. Output Supply Voltage

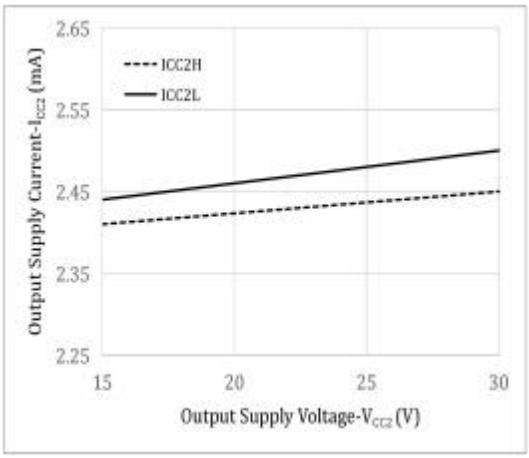


Fig.11 Blanking Capacitor Charging Current vs. Ambient Temperature

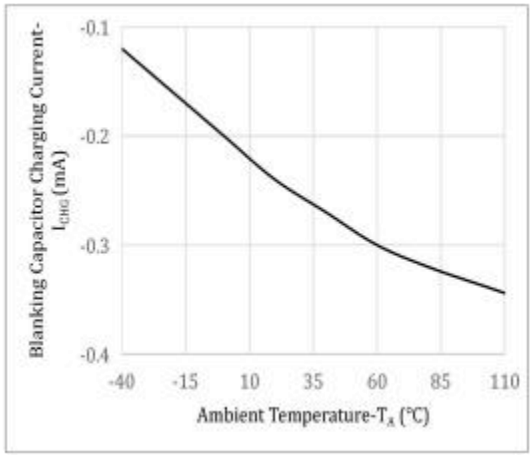


Fig.12 DESAT Voltage vs. Ambient Temperature

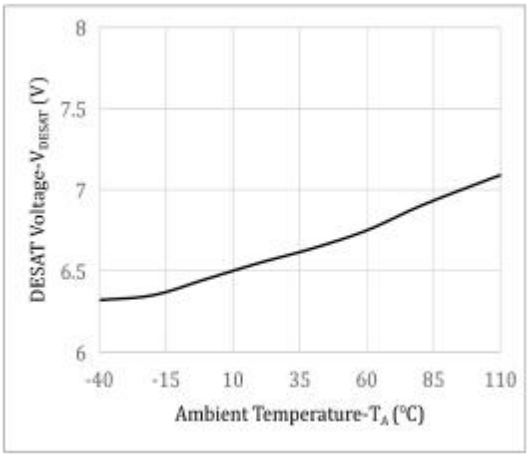


Fig.13 Propagation Delay vs. Ambient Temperature

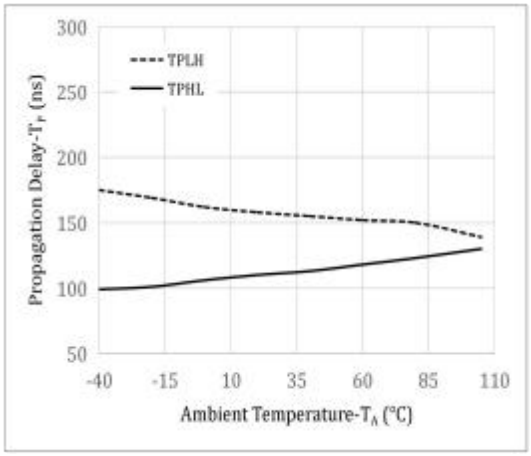


Fig.14 Propagation Delay vs. Supply Voltage

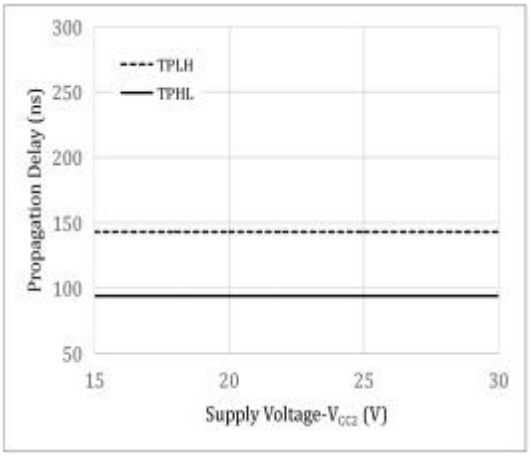


Fig.15 Propagation Delay vs. Load Resistance

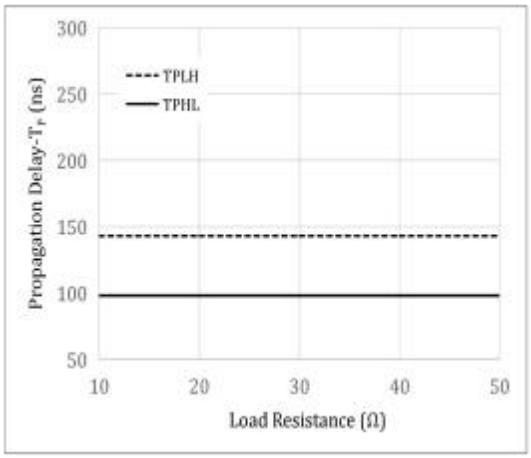


Fig.16 Propagation Delay vs. Load Capacitance

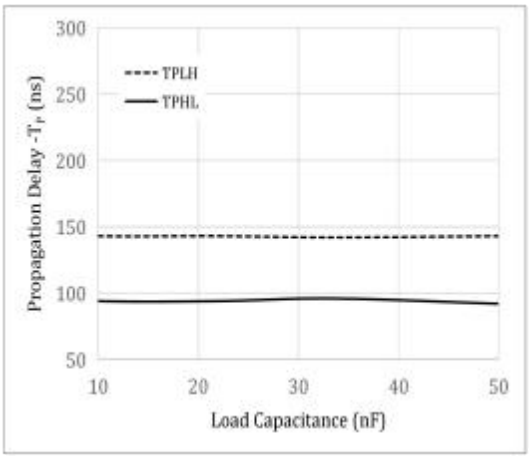


Fig.17 DESAT Sense to 90% V_O Delay vs. Ambient Temperature

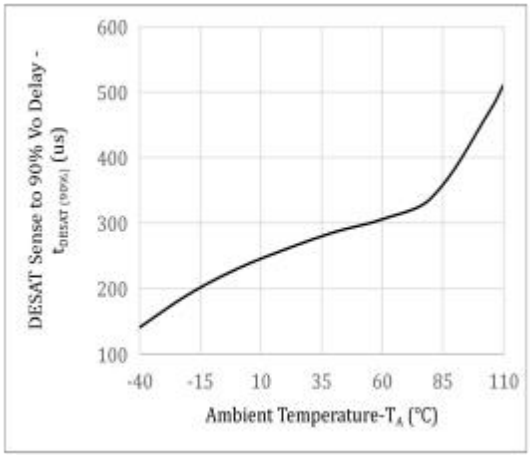


Fig.18 DESAT Sense to 10% V_O Delay vs. Ambient Temperature

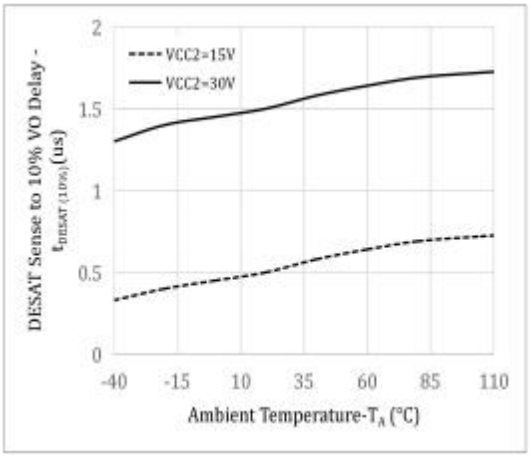


Fig.19 DESAT Sense to 10% V_O Delay vs. Load Resistance

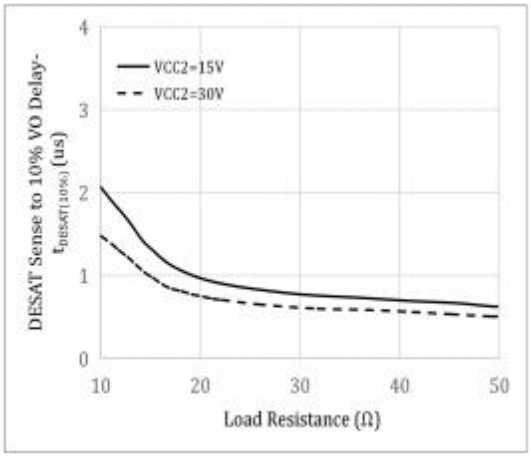
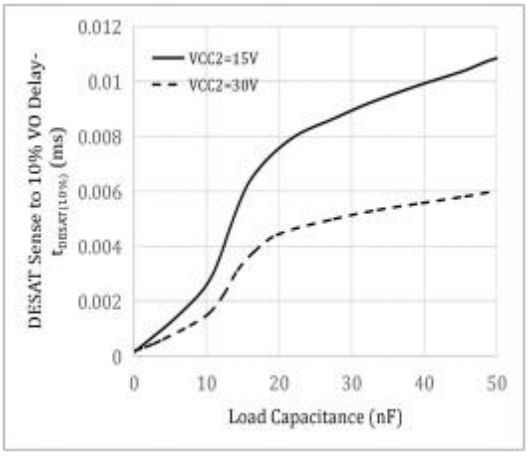


Fig.20 DESAT Sense to 10% V_O Delay vs. Load Capacitance



测试电路图 Test Circuits Diagrams

Figure 21. I_{OH} Pulsed Test Circuit

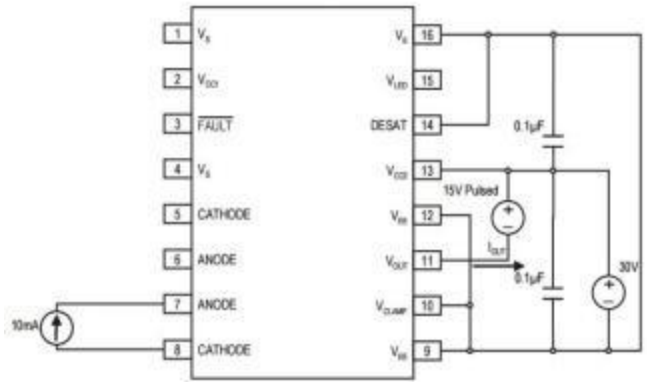


Figure 22. I_{OL} Pulsed Test Circuit

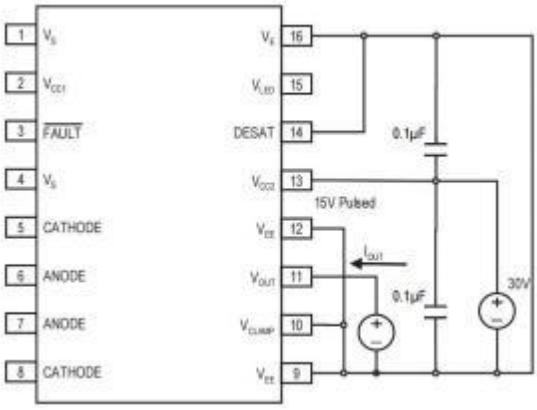


Figure 23. V_{OH} Pulsed Test Circuit

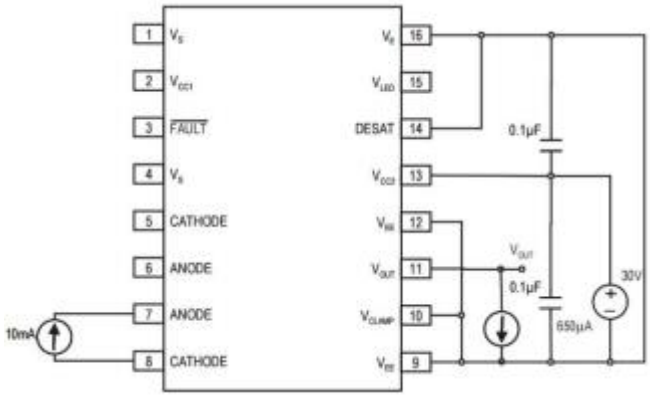


Figure 24. V_{OL} Pulsed Test Circuit

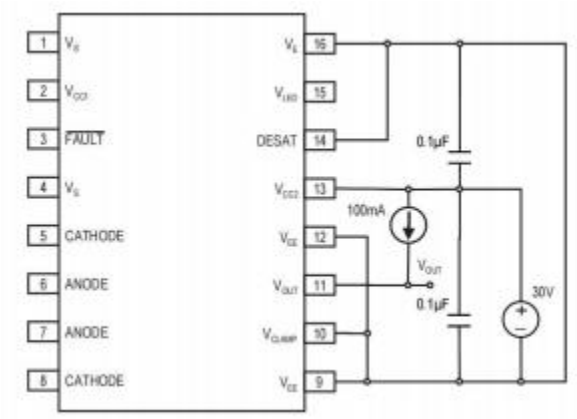


Figure 25. I_{CC2H} Test Circuit

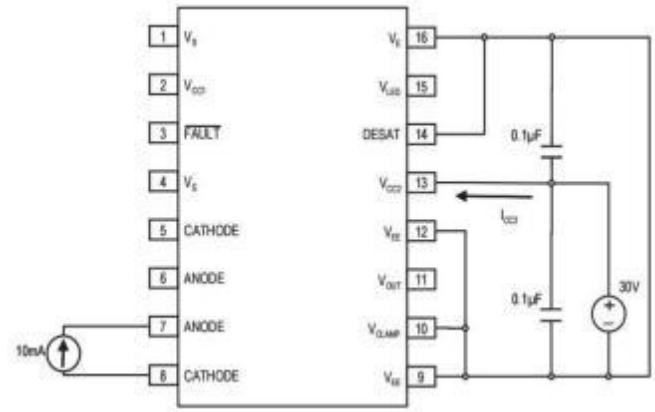


Figure 26. I_{CC2L} Test Circit

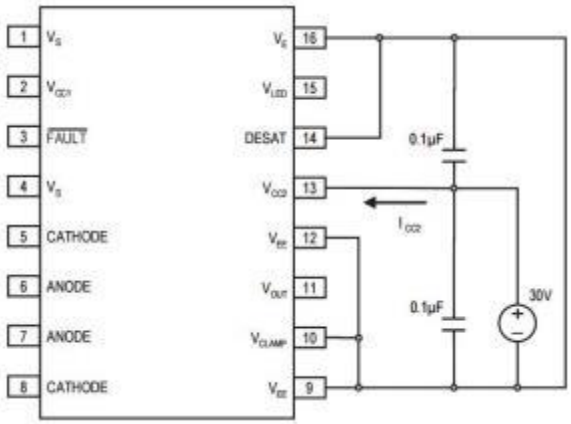


Figure 27. I_{CHG} Pulsed Test Circuit

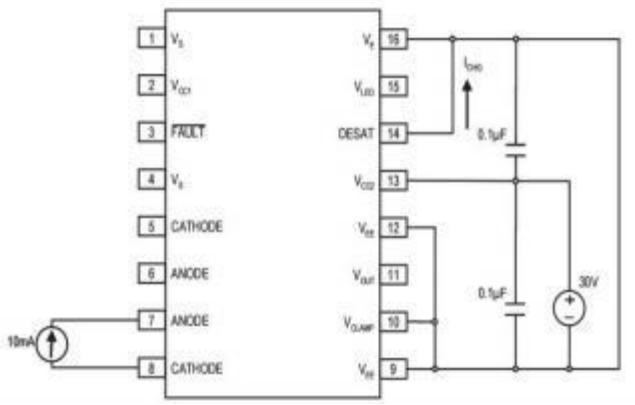


Figure 28. I_{DSCHG} Test Circuit

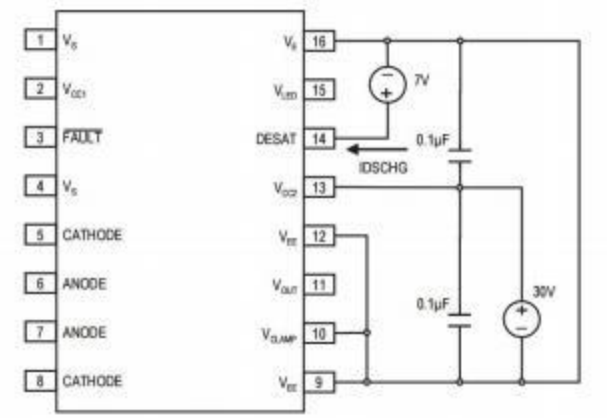


Figure 29. T_{PLH}, T_{PHL}, T_f, T_r, Test Circuit

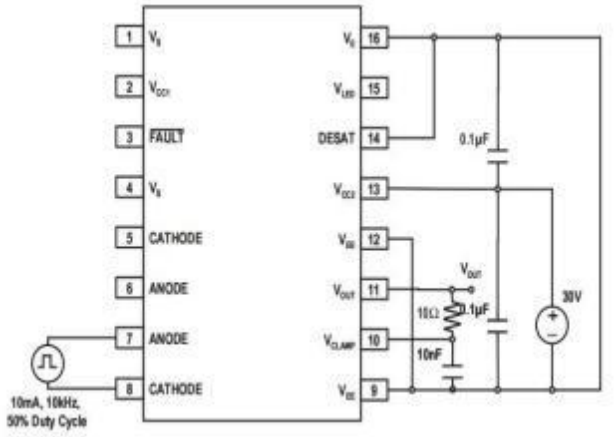


Figure 30. T_{DESAT} Fault Test Circuit

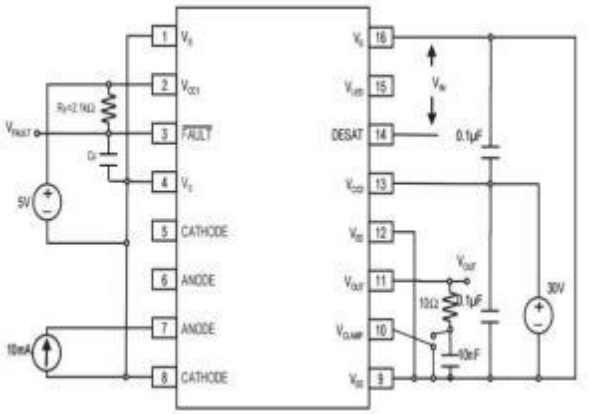


Figure 31. CMR Test Circuit LED2 Off

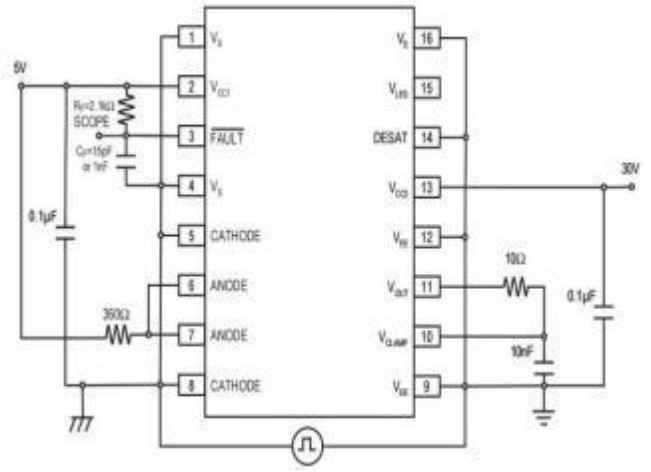


Figure 32. CMR Test Circuit LED2 On

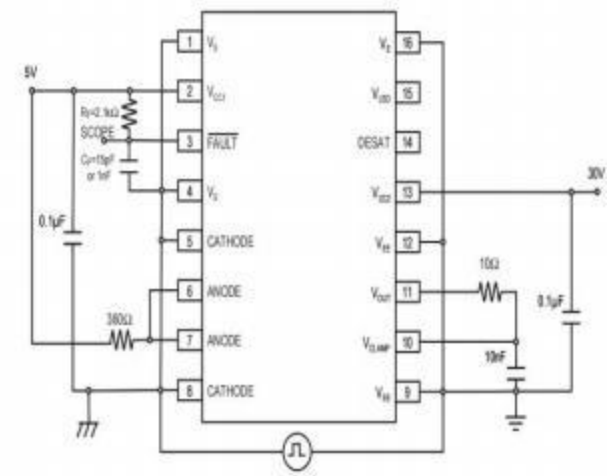


Figure 33. CMR Test Circuit LED1 On

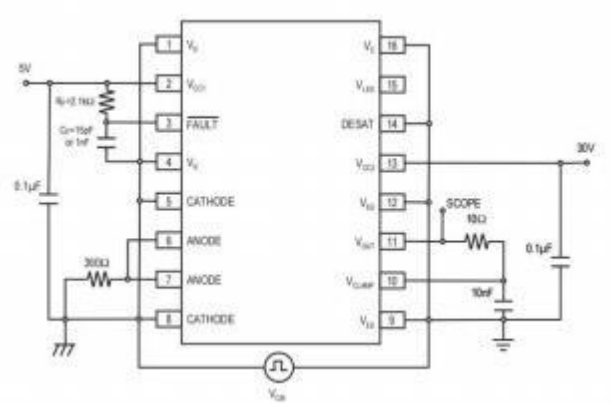
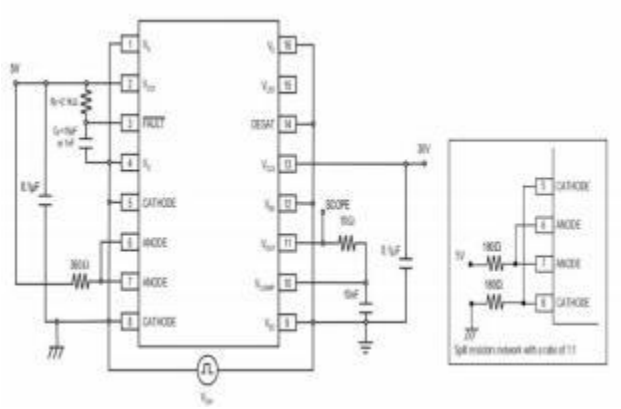


Figure 34. CMR Test Circuit LED1 Off



应用信息 Application Information

1. 产品概述说明 Product Overview Description

AT332J 是高度集成的功率控制器件， 将完整、 隔离型 IGBT/MOSFET 栅极驱动电路与故障保护和反馈电路所必须的元件集成到一个 SO-16 封装中。有源米勒钳位功能消除了大多数应用中对负极栅极驱动的需求， 并允许高压侧驱动器使用简单的自举电路产生电源。光隔离功率输出级可驱动 150A/1200V 的 IGBTs。高速内部光链路最大限度地降低了微控制器和 IGBT 之间的传播延迟， 同时允许两个系统在非常大的共模电压差下运行， 这在工业电机驱动和其他电源开关应用中很常见。输出 IC 为 IGBT 提供局部保护以防止过电流期间产生损坏， 第二光链路为微控制器提供了一个完全隔离的故障状态反馈信号。 内置“看门狗”电路， UVLO 和监控供电电源电压， 以防止 IGBT 出现栅极驱动电压不足的现象。这款集成式 IGBT 栅极驱动器旨在提高电机驱动器的性能和可靠性， 而不增加成本、体积和复杂的分立设计。

The AT332J are highly integrated power control devices that incorporates all the necessary components for a complete, isolated IGBT / MOSFET gate drive circuit with fault protection and feedback into one SO-16 package. Active Miller clamp function eliminates the need of negative gate drive in most application and allows the use of simple bootstrap supply for high side driver. An optically isolated power output stage drives IGBTs with power ratings of up to 150A and 1200V. A high speed internal optical link minimizes the propagation delays between the microcontroller and the IGBT while allowing the two systems to operate at very large common mode voltage differences that are common in industrial motor drives and other power switching applications. An output IC provides local protection for the IGBT to prevent damage during over current, and a second optical link provides a fully isolated fault status feedback signal for the microcontroller. A built in “watchdog” circuit, UVLO monitors the power stage supply voltage to prevent IGBT caused by insufficient gate drive voltages. This integrated IGBT gate driver is designed to increase the performance and reliability of a motor drive without the cost, size, and complexity of a discrete design.

在同一封装 SO-16 中封装了两个发光二极管和两个集成电路， 提供输入控制电路、输出功率级和两个光学通道。输出检测器 IC 采用高压 BiCMOS/功率 DMOS 工艺设计制造。如 LED1 所示， 在光信号的正向传输路径传输门极控制信号。如 LED2 所示， 在光信号的反馈传输路径传输故障状态的反馈信号。

Two light emitting diodes and two integrated circuits housed in the same SO-16 package provide the input control circuitry, the output power stage, and two optical channels. The output Detector IC is designed manufactured on a high voltage BiCMOS/Power DMOS process. The forward optical signal path, as indicated by LED1, transmits the gate control signal. The return optical signal path, as indicated by LED2, transmits the fault status feedback signal.

在正常操作下， LED1 通过隔离输出检测器 IC 直接控制 IGBT 门极， LED2 保持关闭。 当检测到 IGBT 故障时， 输出检测器 IC 立即开始“软”关断， 以可控的方式将 IGBT 电流降低至零， 以避免感应的高压对 IGBT 产生潜在损坏。 同时， 该故障状态通过 LED2 传输回输入端， 故障闩锁使得门极控制输入信号失效， 自动输出低电平故障信号向微控制器发出警报。

Under normal operation, the LED1 directly controls the IGBT gate through the isolated output detector IC, and LED2 remains off. When an IGBT fault is detected, the output detector IC immediately begins a “soft” shutdown sequence, reducing the IGBT current to zero in a controlled manner to avoid potential IGBT damage from inductive over voltages. Simultaneously, this fault status is transmitted back to the input via LED2, where the fault latch disables the gate control input and the active low fault output alerts the microcontroller.

上电期间， 通过强制 AT332J 输出低电平信号， 欠压锁定(UVLO)功能可防止 IGBT 栅极电压不足的现象。一旦输出处于高电平状态， AT332J 的 DESAT (V_{CE})检测功能就会提供 IGBT 保护。 因此， UVLO 和 DESAT 协同工作， 为 IGBT 提供恒定保护。

During power-up, the Under Voltage Lockout (UVLO) feature prevents the application of insufficient gate voltage to the IGBT, by forcing the AT332J’ s output low. Once the output is in the high state, the DESAT (V_{CE}) detection feature

of the AT332J provides IGBT protection. Thus, UVLO and DESAT work in conjunction to provide constant IGBT protection.

2. 推荐应用电路 Recommended Application Circuit

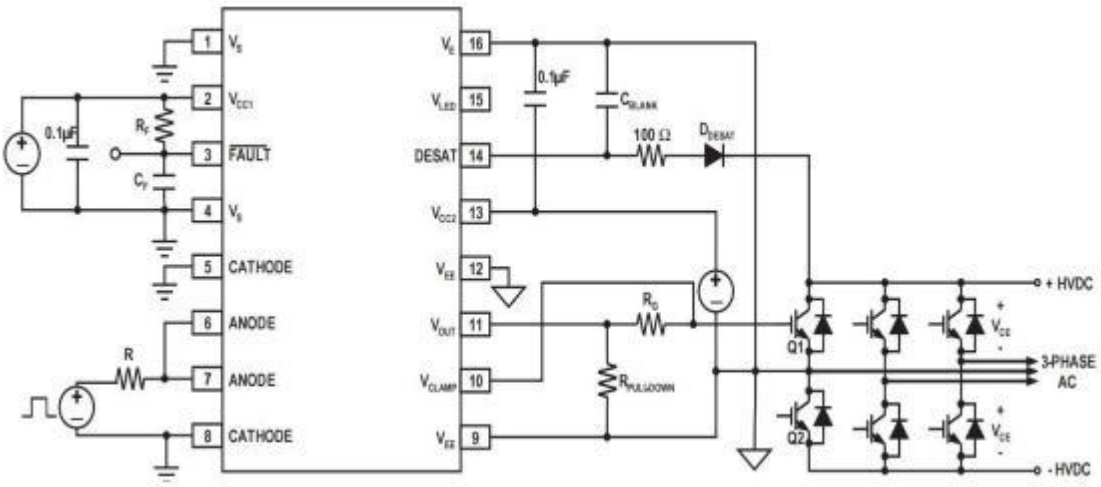
AT332J 具有一个 LED 输入栅极控制和一个开路集电极故障输出， 适用于“或”逻辑电路应用。 图 35 所示的推荐应用电路显示了使用 AT332J 的典型栅极驱动电路。下面介绍有关 IGBT 的驱动。 同样， 它也适用于 MOSFET。根据 MOSFET 或 IGBT 栅极阈值要求， 设计人员可能需要调整 V_{CC} 电源电压(对于 IGBT， 建议 V_{CC} = 17.5V， 对于 MOSFET， 建议 V_{CC}= 12.5V)。

The AT332J has an LED input gate control, and an open collector fault output suitable for wired ‘OR’ applications. The recommended application circuit shown in Figure 35 illustrates a typical gate drive implementation using the AT332J. The following describes about driving IGBT. However, it is also applicable to MOSFET. Depending upon the MOSFET or IGBT gate threshold requirements, designers may want to adjust the V_{CC} supply voltage (Recommended V_{CC} = 17.5V for IGBT and 12.5V for MOSFET).

两个电源旁路电容(0.1 μ F)在开关瞬态提供瞬态大电流。 由于充电电流的瞬态特性， 一个小功率电流(5mA)电源就足够了。快速恢复型去饱和二极管 D_{DESAT} （ 600V/ 1200V） 、t_{rr}低于 75ns(如 ERA34-10)和电容 C_{BLANK} 是故障检测电路的必要外部部件。栅极电阻 R_G 用于限制栅极充电电流， 并控制 IGBT 集电极电压的上升和下降时间。开路集电极故障输出端有一个无源上拉电阻 R_F (2.1kΩ)和一个 1000pF 的滤波电容 C_F， V_{OUT} 输出端的 47kΩ下拉电阻 $R_{PULL-DOWN}$， 可提供一个可预测的高电平输出电压(V_{OH})。在这种应用中， 当检测到故障并在 IGBT 的下一个开通信号将故障复位时， IGBT 门驱动器将关断。

The two supply bypass capacitors (0.1 μ F) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (5mA) power supply suffices. The desaturation diode D_{DESAT} 600V/1200V fast recovery type, t_{rr} below 75ns (e.g. ERA34-10) and capacitor C_{BLANK} are necessary external components for the fault detection circuitry. The gate resistor R_G serves to limit gate charge current and controls the IGBT collector voltage rise and fall times. The open collector fault output has a passive pull-up resistor R_F (2.1k Ω) and a 1000pF filtering capacitor, C_F. A 47k Ω pull down resistor $R_{PULL-DOWN}$ on V_{OUT} provides a predictable high level output voltage (V_{OH}). In this application, the IGBT gate driver will shut down when a fault is detected and fault reset by next cycle of IGBT turn on.

Figure 35. Recommended application circuit (Single Supply) with desaturation detection and active Miller Clamp



操作描述 Description of Operation

1. 正常操作 Normal Operation

正常工作期间， AT332J 的 V_{OUT} 由输入 LED 电流 I_F (引脚 5、6、7 和 8)控制， IGBT 集电极-发射极电压通过 DESAT 监控。FAULT 端输出高电平。参见图 36。

During normal operation, V_{OUT} of the AT332J is controlled by input LED current I_F (pins 5, 6, 7 and 8), with the IGBT collector-to-emitter voltage being monitored through DESAT. The FAULT output is high. See Figure 36.

2. 故障条件 Fault Condition

DESAT 引脚监控 IGBT 的 V_{ce}压降。 当 IGBT 开启时， DESAT 引脚上的电压超过 6.5 V， V_{OUT} 将逐渐降低电平， 以实现“软”关断， 防止出现过高的 di/dt 和感应电压。 同时激活的还有一个内部反馈通道， 当满足报警条件时 FAULT 端输出低电平， 向微控制器报警。

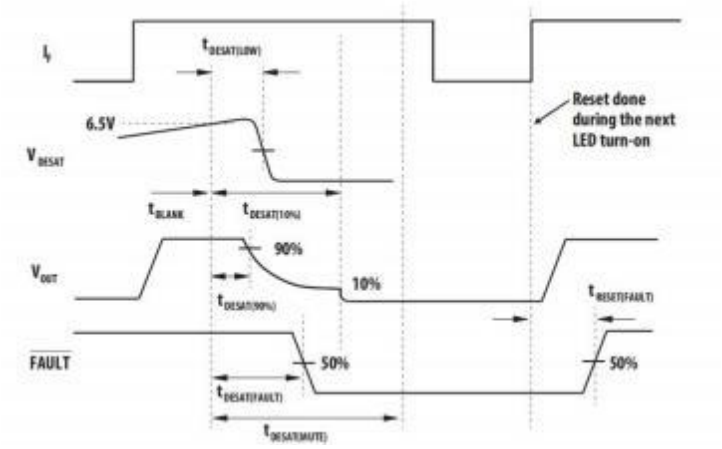
The DESAT pin monitors the IGBT V_{ce}voltage. When the voltage on the DESAT pin exceeds 6.5 V while the IGBT is on, V_{OUT} is slowly brought low in order to “softly” turn-off the IGBT and prevent large di/dt induced voltages. Also activated is an internal feedback channel which brings the FAULT output low for the purpose of notifying the micro-controller of the fault condition.

3. 故障复位 Fault Reset

一旦检测到故障， 输出将在 5μs（最小值）内衰减。在衰减期间， LED 所有输入信号都将被忽略， 让驱动电路完全软关断 IGBT。故障状态将在 5us（最小）衰减时间后的下一次 LED 开启时复位。见图 36。

Once fault is detected, the output will be muted for 5 μs (minimum). All input LED signals will be ignored during the mute period to allow the driver to completely soft shut-down the IGBT. The fault mechanism can be reset by the next LED turn-on after the 5us (minimum) mute time. See Figure 36.

Figure 36. Fault Timing diagram



4. 输出控制 Output Control

AT332J 的输出部分(V_{OUT} 和 FAULT)由 I_F、UVLO 和一个检测到的 IGBT Desat 的组合共同控制。一旦 UVLO 保护没有激活(V_{CC2} - V_E > V_{UVLO})， V_{OUT} 就会被允许输出高电平，AT332J 的 DESAT 检测功能将成为 IGBT 保护的主要手段。一旦 V_{CC2} 从 0V 增加到 V_{UVLO+} 以上， DESAT 将继续发挥作用， 直到 V_{CC2} < V_{UVLO-}。 因此， AT332J 的 DESAT (Pin 14)检测和 UVLO 功能同时工作以确保恒定的 IGBT 保护。

The outputs (V_{OUT} and FAULT) of the AT332J are controlled by the combination of I_F, UVLO and a detected IGBT Desat condition. Once UVLO is not active (V_{CC2} - V_E > V_{UVLO}), V_{OUT} is allowed to go high, and the DESAT (Pin14) detection feature of the AT332J will be the primary source of IGBT protection. Once V_{CC2} is increased from 0V to above V_{UVLO+}, DESAT will remain functional until V_{CC2} is decreased below V_{UVLO-}. Thus, the DESAT detection and UVLO features of the AT332J work in conjunction to ensure constant IGBT protection.

I_F	UVLO (V_{CC2}-V_E)	DESAT 检测状态 DESAT Function	故障输出 FAULT Output	V_{OUT}
导通 ON	有效 Active	无效 Not Active	高 High	低 Low
导通 ON	无效 Not Active	有效(DESAT 故障) Active (with DESAT fault)	低(故障) Low (FAULT)	低 Low
导通 ON	无效 Not Active	有效(无 DESAT 故障) Active (no DESAT fault)	高(或无故障) High (or no fault)	高 High
关断 OFF	有效 Active	无效 Not Active	高 High	低 Low
关断 OFF	无效 Not Active	无效 Not Active	高 High	低 Low

5. 抗饱和检测和大电流保护 Desaturation Detection and High Current Protection

AT332J 满足了将高速、大电流输出驱动器、输入和输出之间的高压光隔离、 IGBT 饱和检测、关断以及一个光隔离的故障状态信号反馈集成到一个 16 引脚封装中的标准。

The AT332J satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shut down, and an optically isolated fault status feedback signal into a single 16-pin surface mount package.

AT332J 中的故障检测方法是通过监测 IGBT 的饱和（集电极）电压实现的， 并在集电极电压超过预定阈值时触发局部故障停机。小栅极放电装置缓慢降低由 IGBT 短路引起的大电流， 防止产生破坏性尖峰电压。在能耗达到破坏性水平之前，将 IGBT 关断。在 IGBT 关断状态期间， 故障检测电路失效， 以防止产生虚假的“故障”信号。

The fault detection method, which is adopted in the AT332J, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off state of the IGBT, the fault detect circuitry is simply disabled to prevent false ‘fault’ signals.

如果功率器件的短路能力已知， 采用测量 IGBT 电流以防止去饱和的替代保护方案是有效的， 但是如果栅极驱动电压降低到仅能将 IGBT 部分接通， 则该方法将失败。通过直接测量集电极电压， AT332J 即使在栅极驱动电压不足的情况下也能限制 IGBT 的功耗。去饱和检测方法另一个更巧妙的优势是监控 IGBT 中的功耗的同时， 先预设一个的电流阈值来预测安全工作的范围再采用电流感测方法。 因此， 不需要过于保守的过电流阈值来保护 IGBT。

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the AT332J limits the power dissipation in the IGBT even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method

is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly conservative over current threshold is not needed to protect the IGBT.

6. 故障状态下 IGBT 门极“软”关断 Slow IGBT Gate Discharge during Fault Condition

当检测到去饱和故障时， AT332J 输出驱动阶段中弱下拉器件将开通， 以促使 IGBT“软”关断。该器件使 IGBT 栅极缓慢放电， 以防止漏电流的快速变化， 这种变化会因引线电感而产生破坏性的尖峰电压。在缓慢关断期间， 大输出下拉器件保持关断， 直到输出电压降至 V_{EE}+2V 以下， 此时大的下拉器件将 IGBT 栅极钳位至 V_{EE}。

When a desaturation fault is detected, a weak pull-down device in the AT332J output drive stage will turn on to ‘softly’ turn off the IGBT. This device slowly discharges the IGBT gate to prevent fast changes in drain current that could cause damaging voltage spikes due to lead and wire inductance. During the slow turn off, the large output pull-down device remains off until the output voltage falls below V_{EE} + 2 Volts, at which time the large pull down device clamps the IGBT gate to V_{EE}.

7. DESAT 故障检测消隐时间 DESAT Fault Detection Blanking Time

IGBT 开启后， DESAT 故障检测电路必须保持失效一段时间， 以使集电极电压降至 DESAT 阈值以下。这段时间称为 DESAT 消隐时间， 由内部 DESAT 充电电流、 DESAT 电压阈值和外部 DESAT 电容控制。

The DESAT fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT threshold. This time period, called the DESAT blanking time is controlled by the internal DESAT charge current, the DESAT voltage threshold, and the external DESAT capacitor.

理论上消隐时间根据外部电容(C_{BLANK})、故障阈值电压(V_{DESAT})和 DESAT 充电电流(I_{CHG})计算得出， 即 $t_{BLANK} = C_{BLANK} \times V_{DESAT} / I_{CHG}$。推荐的 100pF 电容的理论消隐时间为 100pF * 6.5V/240μA =2.7 μsec。

The nominal blanking time is calculated in terms of external capacitance (C_{BLANK}), FAULT threshold voltage (V_{DESAT}), and DESAT charge current (I_{CHG}) as $t_{BLANK} = C_{BLANK} \times V_{DESAT} / I_{CHG}$. The nominal blanking time with the recommended 100pF capacitor is 100pF * 6.5 V / 240μA = 2.7 μsec.

可以稍微调整电容值来调整消隐时间， 但不建议使用小于 100pF 的电容。理论消隐时间代表 AT332J 响应 DESAT 故障状态所需的最长时间。如果 IGBT 开启的同时， 集电极和发射极之间与供电电源短路(切换为短路)， 则软关断措施将在大约 3 μs 后启动。如果 IGBT 开启之后， 集电极和发射极之间与供电电源短路(切换为短路)， 由于 DESAT 二极管的寄生并联电容， 响应时间会大大加快。推荐的 100pF 电容会提供足够的消隐以适应大多数应用的故障响应时间。

The capacitance value can be scaled slightly to adjust the blanking time, though a value smaller than 100pF is not recommended. This nominal blanking time represents the longest time it will take for the AT332J to respond to a DESAT fault condition. If the IGBT is turned on while the collector and emitter are shorted to the supply rails (switching into a short), the soft shut-down sequence will begin after approximately 3 μsec. If the IGBT collector and emitter are shorted to the supply rails after the IGBT is already on, the response time will be much quicker due to the parasitic parallel capacitance of the DESAT diode. The recommended 100pF capacitor should provide adequate blanking as well as fault response times for most applications.

8. 欠压闭锁 Under Voltage Lockout

AT332J 欠压闭锁(UVLO)功能旨在防止上电期间因 IGBT 栅极电压不足而强制 AT332J 输出低电平。 IGBTs 通常需要 15V 的栅极电压来获得其额定的 V_{CE}(导通)电压。通常在栅极电压低于 13V 时， V_{CE}(导通)电压急剧增加， 尤其是在流经较高的电流下。在栅极电压非常低(低于 10V)时， IGBT 可能会工作在线性区域， 并迅速过热。 只要施加的工作电源(V_{CC2})不足， UVLO 功能就会导致输出端被钳位。一旦 V_{CC2} 超过 V_{UVLO+} (正向 UVLO 阈值)， UVLO 钳位就会被释放， 允许器件响应输入信号而输出。 当 V_{CC2} 从 0V(低于 V_{UVLO+})开始升高， DESAT 保护电路首先激活。 随着 V_{CC2} 进一步增加(高于 V_{UVLO+})， UVLO 钳位

被释放。在 UVLO 钳位被释放之前， DESAT 保护已经激活。 因此， 无论电源电压(V_{CC2})如何， UVLO 和 DESAT 故障检测特性都可以同时工作， 提供全面保护。

The AT332J Under Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to the IGBT by forcing the AT332J output low during power-up. IGBTs typically require gate voltages of 15V to achieve their rated V_{CE}(ON) voltage. At gate voltages below 13V typically, the V_{CE}(ON) voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10V), the IGBT may operate in the linear region and quickly overheat. The UVLO function causes the output to be clamped whenever insufficient operating supply (V_{CC2}) is applied. Once V_{CC2} exceeds V_{UVLO+} (the positive-going UVLO threshold), the UVLO clamp is released to allow the device output to turn on in response to input signals. As V_{CC2} is increased from 0V (at some level below V_{UVLO+}), first the DESAT protection circuitry becomes active. As V_{CC2} is further increased (above V_{UVLO+}), the UVLO clamp is released. Before the time the UVLO clamp is released, the DESAT protection is already active. Therefore, the UVLO and DESAT Fault detection feature work together to provide seamless protection regardless of supply voltage (V_{CC2}).

9. 有源米勒钳位 Active Miller Clamp

米勒钳位允许在高 dV/dt 情况下控制米勒电流， 并且在大多数应用中可以取消负电源电压。关断期间， 当栅极电压低于 2V(相对于 V_{EE})时， 监控栅极电压， 同时钳位输出被激活。对于高达 1100mA 的米勒电流， 钳位电压典型值为 V_{OL}+2.5V。当再次触发 LED 输入时， 钳位失效。

A Miller clamp allows the control of the Miller current during a high dV/dt situation and can eliminate the use of a negative supply voltage in most of the applications. During turn-off, the gate voltage is monitored and the clamp output is activated when gate voltage goes below 2V (relative to V_{EE}). The clamp voltage is V_{OL}+2.5V typ for a Miller current up to 1100mA. The clamp is disabled when the LED input is triggered again

其他推荐组件 Other Recommended Components

图 35 中的应用电路中一个输出下拉电阻、一个 DESAT 端保护电阻、一个 FAULT 端电容、一个 FAULT 端上拉电阻和有源米勒钳位相连接。

The application circuit in Figure 35 includes an output pull-down resistor, a DESAT pin protection resistor, a FAULT pin capacitor, and a FAULT pin pullup resistor and Active Miller Clamp connection.

Figure 37. Output pull-down resistor

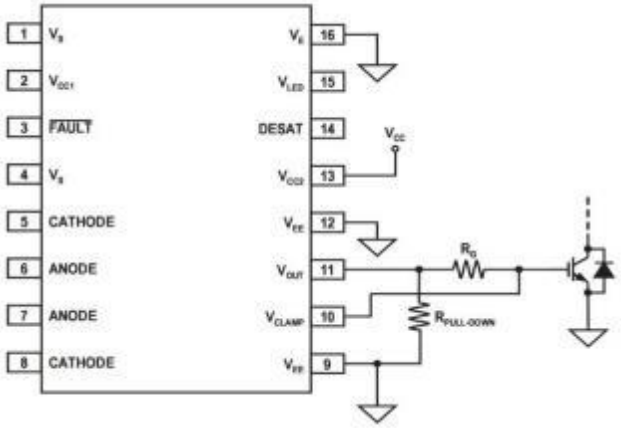
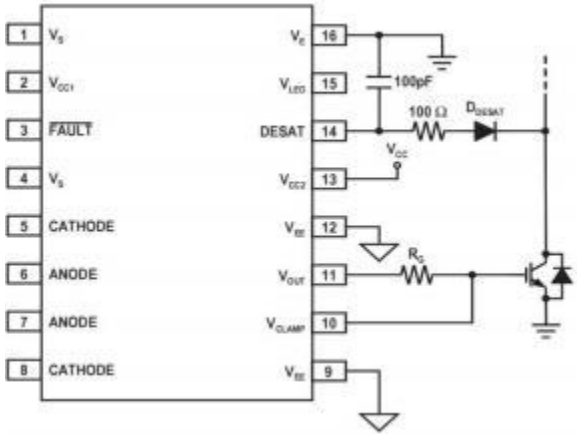


Figure 38. DESAT pin protection



1. 输出下拉电阻 Output Pull-Down Resistor

在输出为高电平的转换期间， 输出电压迅速上升至 V_{CC2}，在 3 个二极管压降以内。如果输出电流因容性负载而降至零， 输出电压将在几微秒内大约缓慢上升至 V_{CC2}-3(V_{BE})与 V_{CC2} 之间。为了将输出电压限制在 V_{CC2}-3(V_{BE})， 建议在输出与 V_{EE} 之间接一个下拉电阻 $R_{PULL-DOWN}$， 以便在输出为高电平时产生几个 650μA 的灌电流。下拉电阻值取决于正向电源的值， 可以根据公式 $R_{pull-down}$ = [V_{CC2}-3 *(V_{BE})]/650μA 进行调整。

During the output high transition, the output voltage rapidly rises to within 3 diode drops of V_{CC2}. If the output current then drops to zero due to a capacitive load, the output voltage will slowly rise from roughly V_{CC2}-3(V_{BE}) to V_{CC2} within a period of several microseconds. To limit the output voltage to V_{CC2}-3(V_{BE}), a pull-down resistor, $R_{PULL-DOWN}$ between the output and V_{EE} is recommended to sink a static current of several 650μA while the output is high. Pull-down resistor values are dependent on the amount of positive supply and can be adjusted according to the formula, $R_{pull-down}$ = [V_{CC2}-3 * (V_{BE})] / 650μA.

2. DESAT 引脚保护电阻 DESAT Pin Protection Resistor

与 IGBTs 连接的续流二极管会产生大大超过二极管理论正向电压的瞬态正向电压值。这可能会导致 DESAT 引脚上产生较大的反向尖峰电压， 如果不采取保护措施的话， 将会从驱动器中转移大量电流。为了将此电流限制在不会损坏驱动器 IC 的水平， 需要插入一个 100 欧姆的电阻与 DESAT 二极管串联。这个新增的电阻不会改变 DESAT 阈值或 DESAT 消隐时间。

The freewheeling of flyback diodes connected across the IGBTs can have large instantaneous forward voltage transients which greatly exceed the nominal forward voltage of the diode. This may result in a large negative voltage spike on the DESAT pin which will draw substantial current out of the driver if protection is not used. To limit this current to levels that will not damage the driver IC, a 100 ohm resistor should be inserted in series with the DESAT diode. The added resistance will not alter the DESAT threshold or the DESAT blanking time.

3. 高 CMR 故障端的电容 Capacitor on FAULT Pin for High CMR

当故障输出处于高电平状态时， 快速共模瞬变会影响故障端电压。 FAULT 和地之间应连接一个 1000pF 电容， 当额定 CMR 为 50kV/μs 时， 可获得足够的 CMOS 噪声容限。

Rapid common mode transients can affect the fault pin voltage while the fault output is in the high state. A 1000 pF capacitor should be connected between the fault pin and ground to achieve adequate CMOS noise margins at the specified CMR value of 50kV/μs.

4. FAULT 端的上拉电阻 Pull-up Resistor on FAULT Pin

FAULT 引脚是集电极开路输出， 因此需要一个上拉电阻来提供一个高电平信号。此外， 故障输出可以通过“或”运算与其他类型的保护(例如过热、过压、过流)连接在一起， 向微控制器报警。

The FAULT pin is an open collector output and therefore requires a pull-up resistor to provide a high-level signal. Also the FAULT output can be wire ‘OR’ ed together with other types of protection (e.g. over-temperature, over-voltage, over-current) to alert the microcontroller.

5. 其他可能的应用电路(输出端) Other Possible Application Circuit (Output Stage)

图.39 具有负栅极驱动、外部升压器和去饱和检测的 IGBT 驱动 （V_{Clamp}端不使用时， 需要与 V_{EE} 连接) V_{Clamp}作为栅极的二级放电路径。*表示负栅极驱动拓扑结构所必须的组成部分。

Figure 39. IGBT drive with negative gate drive, external booster and desaturation detection (V_{Clamp} should be connected to V_{EE} when it is not used) V_{Clamp} is used as secondary gate discharge path. * indicates component required for negative gate drive topology.

Fig.39

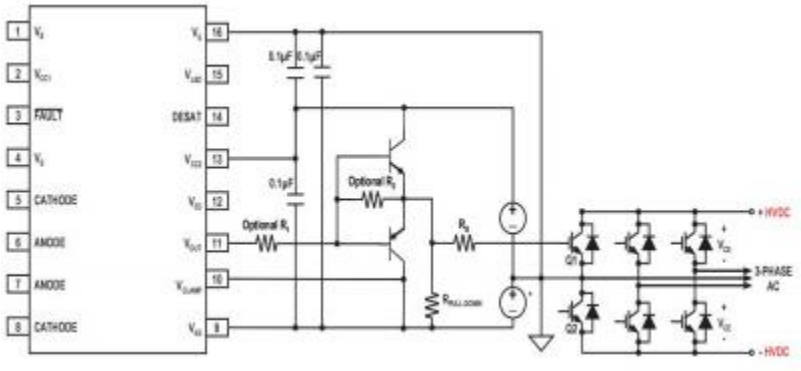
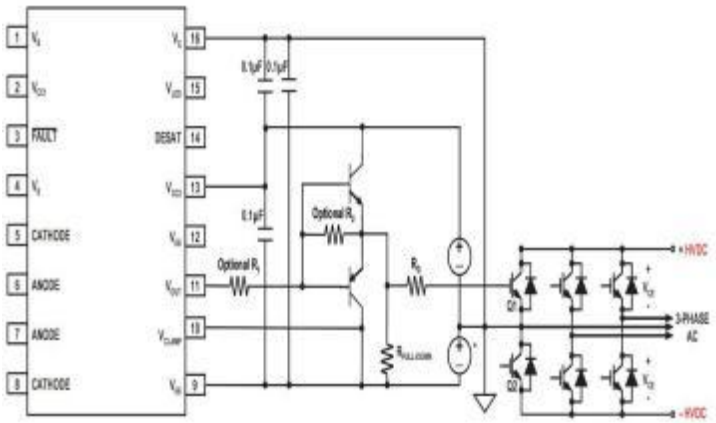


Fig.40 Large IGBT drive with negative gate drive, external booster. VCLAMP control secondary discharge path for higher power application



热模型 Thermal Model

AT332J 设计旨在通过输入 IC 的引脚 1、4、 5 和 8 以及输出 IC 的引脚 9 和 12 进行散热。 (因此， 输出端有两个 V_{EE} 引脚， 即引脚 9 和 12) 通过其他引脚或封装直接进入环境的热流被认为是可以忽略的， 此处不予建模。

The AT332J is designed to dissipate the majority of the heat through pins 1, 4, 5 & 8 for the input IC and pins 9 &12 for the output IC. (There are two V_{EE} pins on the output side, pins 9 and 12, for this purpose.) Heat flow through other pins or through the package directly into ambient are considered negligible and not modeled here.

为了达到绝对最大规格中规定的功耗， 引脚 5、9 和 12 必须与接地层连接。只要不超过最大功率规格， 125℃的绝对最大结温规格是对功耗的唯一其他限制， 结温可通过以下公式计算:

In order to achieve the power dissipation specified in the absolute maximum specification, it is imperative that pins 5, 9, and 12 have ground planes connected to them. As long as the maximum power specification is not exceeded, the only other limitation to the amount of power one can dissipate is the absolute maximum junction temperature specification of 125°C. The junction temperatures can be calculated with the following equations:

$T_{ji} = P_i (\theta_{i5} + \theta_{5A}) + T_A$

$T_{jo} = P_o (\theta_{o9,12} + \theta_{9,12A}) + T_A$

其中 P_i =输入 IC 的功率， P_o =输出 IC 的功率。 由于θ_{5A}和$\theta_{9，12A}$取决于 PCB 布局和气流， 可能无法获得它们的准确数值。 因此，更精确地计算结温的方法如以下公式:

Where Pi = power into input IC and Po = power into output IC. Since θ_{5A} and $\theta_{9,12A}$ are dependent on PCB layout and airflow, their exact number may not be available. Therefore, a more accurate method of calculating the junction temperature is with the following equations:

$T_{ji} = P_i\theta_{i5} + T_{P5}$

$T_{jo} = P_o\theta_{o9,12} + T_{P9,12}$

然而， 这些公式需要利用 AT332J 封装边缘引脚上的热电偶来测量引脚 5 和引脚 9、12 的温度。

These equations, however, require that the pin 5 and pins 9, 12 temperatures be measured with a thermal couple on the pin at the AT332J package edge.

如果图 41 中热模型的计算结温高于 125℃， 则应在最差工作环境下测量引脚 9 和 12 的引脚温度(在封装边缘),以便更精确地估计结温。

If the calculated junction temperatures for the thermal model in Figure 41 is higher than 125°C, the pin temperature for pins 9 and 12 should be measured (at the package edge) under worst case operating environment for a more accurate estimate of the junction temperatures.

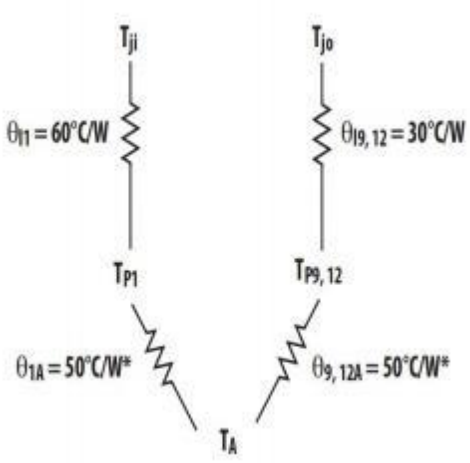


Figure. 41 AT332J thermal model

T_{ji} =输入端 IC 的结温

T_{ji} = junction temperature of input side IC

T_{jo} =输出端 IC 的结温

T_{jo} = junction temperature of output side IC

T_{P5} =封装边缘引脚 5 的温度

T_{P5} = pin 5 temperature at package edge

$T_{P9,2}$ =封装边缘引脚 9 和 12 的温度

$T_{P9,2}$ = pin 9 and 12 temperature at package edge

θ_{I5} =输入端 IC 引脚 5 的热阻

θ_{I5} = input side IC to pin 5 thermal resistance

$\theta_{o9,12}$ =输出端 IC 引脚 9 和 12 的热阻

$\theta_{o9,12}$ = output side IC to pin 9 and 12 thermal resistance

θ_{5A} =引脚 5 环境热阻

θ_{5A} = pin 5 to ambient thermal resistance

$\theta_{9,12A}$ =引脚 9 和 12 环境热阻

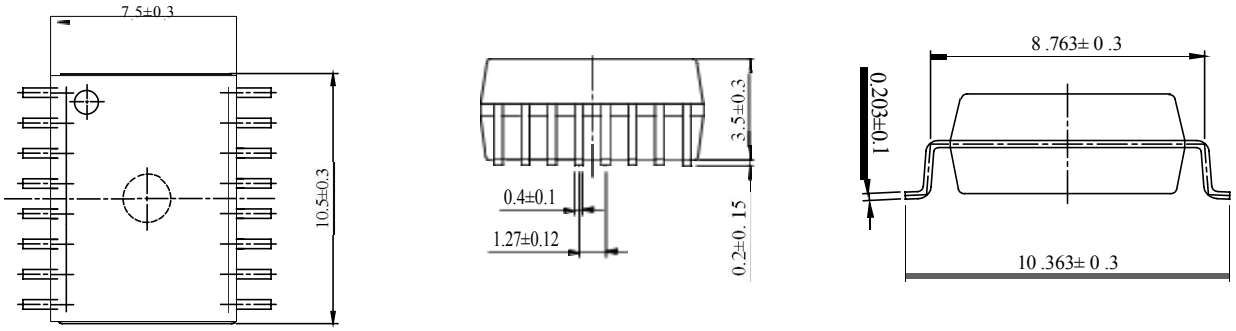
$\theta_{9,12A}$ = pin 9 and 12 to ambient thermal resistance

*此处显示的θ_{5A}和$\theta_{9,12A}$值适用于气流合理的 PCB 布局。根据 PCB 布局/气流情况， 该值可能增加或减少 2 倍。

*The θ_{5A} and $\theta_{9,12A}$ values shown here are for PCB layouts with reasonable air flow. This value may increase or decrease by a factor of 2 depending on PCB layout or airflow.

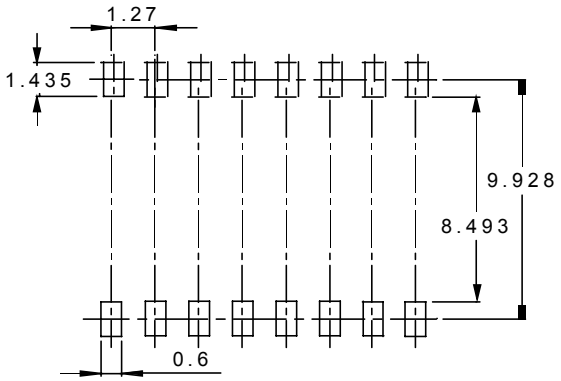
外形尺寸 Package Dimensions

SOP16



单位 Unit: mm

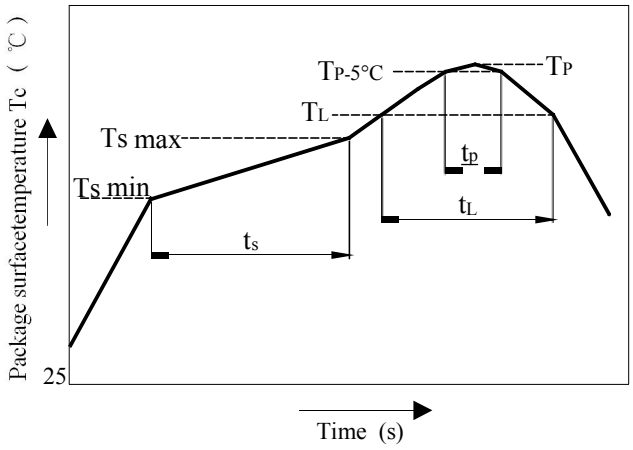
建议焊盘布局 Land Pattern Dimensions



单位 Unit: mm

注： 上图为产品正视图。
Note： The picture above is the front view of the product.

回流焊温度曲线图 Solder Reflow Profile

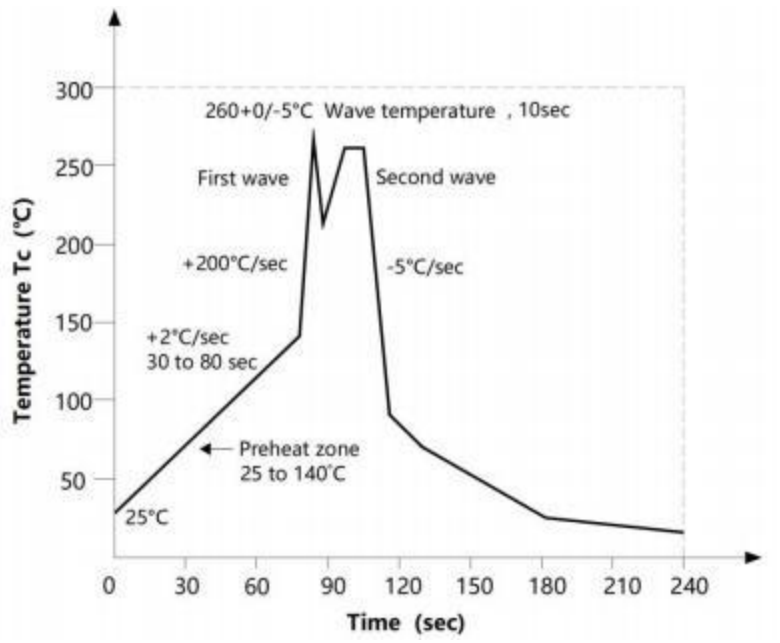


项目 Item	符号 Symbol	最小值 Min.	最大值 Max.	单位 Unit
预热温度 Preheat Temperature	T_S	150	200	℃
预热时间 Preheat Time	t_S	60	120	s
升温速率 Ramp-Up Rate (T_L to T_P)	-	-	3	℃/s
液相线温度 Liquidus Temperature	T_L	217		℃
时间高于 T_L Time Above T_L	t_L	60	150	s
峰值温度 Peak Temperature	T_P	-	260	℃
T_C在(T_P-5)和 T_P之间的时间 Time During Which T_C Is Between (T_P-5) and T_P	t_p	-	30	s
降温速率 Ramp-down Rate(T_P to T_L)	-	-	6	℃/s

注： 建议在所示的温度和时间条件下进行回流焊， 最多不能超过三次。

Note： Reflow soldering is recommended at the temperatures and times shown, no more than three times.

波峰焊温度曲线图 Wave Soldering Profile



手工烙铁焊接 Soldering with hand soldering iron

A. 手工烙铁焊仅用于产品返修或样品测试；
Hand soldering iron is only used for product rework or sample testing;

B. 手工烙铁焊要求： 温度 360℃ ± 5℃， 时间≤3s。
Manual soldering method Temperature: 360℃ ± 5℃, within 3s.

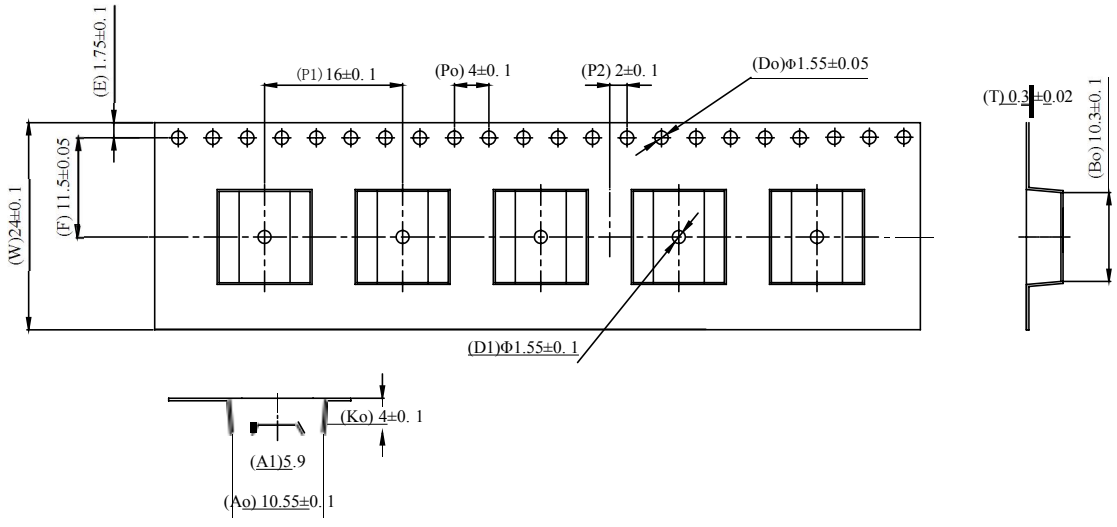
包装 Packing

■ 汇总表 Summary table

封装形式	包装形式	每卷数量	每盒数量	每箱数量	防静电包规格	注意
SOP16	Reel(ϕ330mm 蓝盘)	850 个/卷	2 条/箱	10 盒/箱	450*390*0.1mm	防护带最小 200mm
Package Type	**Packing Form**	**Quantity per Reel**	**Quantity per Box**	**Quantity per Carton**	**Antistatic Bag Specification**	**Note**
SOP16	Reel(ϕ330mm Blue)	850pcs/reel	2Reel/box	10box/ctn	450*390*0.1mm	Guard band 200mm min.

■ 编带包装 Tape & Reel

1) 每卷数量： 850 只。
   Qty/reel： 850pcs.
2) 每箱数量： 17000 只。
   Qty/ctn： 17000pcs.
3) 内包装： 每盒 2 盘。
   Inner packing： 2 reels/box.
4) 示意图 Schematic：



单位 Unit： mm

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