

Description

The TLC2272 and TLC2274 are dual and quadruple operational amplifiers. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC2272 and TLC2274 family offers 2 MHz of bandwidth and 3 V/ μ s of slew rate for higher-speed applications. These devices offer comparable AC performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC2272 and TLC2274 has a noise voltage of 9 nV/ $\sqrt{\text{Hz}}$, two times lower than competitive solutions.

The TLC2272 and TLC2274 family of devices, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA family is available with a maximum input offset voltage of 950 μ V. This family is fully characterized at 5 V and ± 5 V.

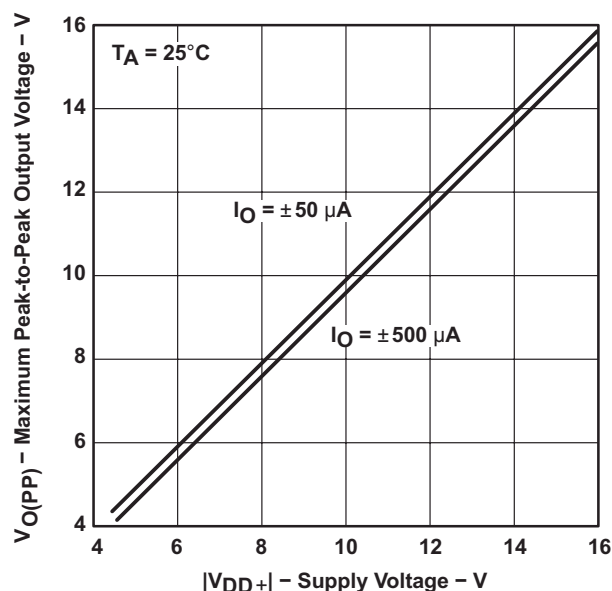
Applications

- White Goods (Refrigerators, Washing Machines)
- Hand-held Monitoring Systems
- Configuration Control and Print Support
- Transducer Interfaces
- Battery-Powered Applications

Features

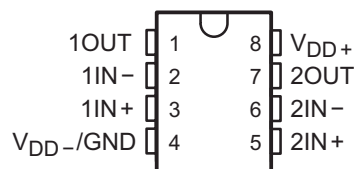
- Output Swing Includes Both Supply Rails
- Low Noise: 9 nV/ $\sqrt{\text{Hz}}$ Typical at $f = 1$ kHz
- Low-Input Bias Current: 1-pA Typical
- Fully-Specified for Both Single-Supply and Split-Supply Operation
- Common-Mode Input Voltage Range Includes Negative Rail
- High-Gain Bandwidth: 2.2-MHz Typical
- High Slew Rate: 3.6-V/ μ s Typical
- Low Input Offset Voltage: 950 μ V Maximum at $T_A = 25^\circ\text{C}$

Maximum Peak-to-Peak Output Voltage vs Supply Voltage

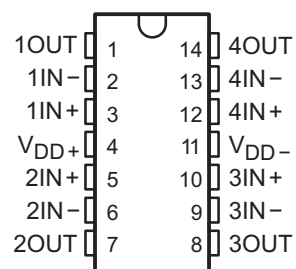


Pin Configuration and Functions

TLC2272
SOP-8 Top View



TLC2274
SOP-14 Top View



Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	TLC2272	TLC2274		
	SOP8	SOP14		
1IN+	3	3	I	Non-inverting input, Channel 1
1IN-	2	2	I	Inverting input, Channel 1
1OUT	1	1	O	Output, Channel 1
2IN+	5	5	I	Non-inverting input, Channel 2
2IN-	6	6	I	Inverting input, Channel 2
2OUT	7	7	O	Output, Channel 2
3IN+	—	10	I	Non-inverting input, Channel 3
3IN-	—	9	I	Inverting input, Channel 3
3OUT	—	8	O	Output, Channel 3
4IN+	—	12	I	Non-inverting input, Channel 4
4IN-	—	13	I	Inverting input, Channel 4
4OUT	—	14	O	Output, Channel 4
V _{DD+}	8	4	—	Positive (highest) supply
V _{DD-}	—	11	—	Negative (lowest) supply
V _{DD-/GND}	4	—	—	Negative (lowest) supply
NC	—	—	—	No Connection

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, V_{DD+} ⁽²⁾			8	V
V_{DD-} ⁽²⁾		-8		V
Differential input voltage, V_{ID} ⁽³⁾			±16	V
Input voltage, V_I (any input) ⁽²⁾		$V_{DD-} - 0.3$	V_{DD+}	V
Input current, I_I (any input)			±5	mA
Output current, I_O			±50	mA
Total current into V_{DD+}			±50	mA
Total current out of V_{DD-}			±50	mA
Duration of short-circuit current at (or below) 25°C ⁽⁴⁾		Unlimited		
Operating free-air temperature range, T_A	C level parts	0	70	°C
	I, Q level parts	-40	125	
	M level parts	-55	125	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D package		260	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
- (3) Differential voltages are at $IN+$ with respect to $IN-$. Excessive current will flow if input is brought below $V_{DD-} - 0.3$ V.
- (4) The output may be shorted to either supply. Temperature or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	Q-grade and M-grade devices in D and PW packages	±2000	V
		Charged-device model (CDM), per AEC Q100-011	Q-grade and M-grade devices in D and PW packages	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{DD±}$	Supply voltage	C LEVEL PARTS	±2.2	±8	V
		I LEVEL PARTS	±2.2	±8	
		Q LEVEL PARTS	±2.2	±8	
		M LEVEL PARTS	±2.2	±8	
V_I	Input voltage	C LEVEL PARTS	V_{DD-}	$V_{DD+} - 1.5$	V
		I LEVEL PARTS	V_{DD-}	$V_{DD+} - 1.5$	
		Q LEVEL PARTS	V_{DD-}	$V_{DD+} - 1.5$	
		M LEVEL PARTS	V_{DD-}	$V_{DD+} - 1.5$	
V_{IC}	Common-mode input voltage	C LEVEL PARTS	V_{DD-}	$V_{DD+} - 1.5$	V
		I LEVEL PARTS	V_{DD-}	$V_{DD+} - 1.5$	
		Q LEVEL PARTS	V_{DD-}	$V_{DD+} - 1.5$	
		M LEVEL PARTS	V_{DD-}	$V_{DD+} - 1.5$	

Recommended Operating Conditions (continued)

		MIN	MAX	UNIT
T _A	C LEVEL PARTS	0	70	°C
	I LEVEL PARTS	-40	125	
	Q LEVEL PARTS	-40	125	
	M LEVEL PARTS	-55	125	

Thermal Information

THERMAL METRIC ⁽¹⁾		TLC2272	TLC2274	UNIT
		D (SOP)	D (SOP)	
		8-PIN	14-PIN	
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾⁽³⁾	115.6	83.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance ⁽²⁾⁽³⁾	61.8	43.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	55.9	38.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	14.3	9.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	55.4	38.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A) / θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.

TLC2272 and TLC2272A Electrical Characteristics V_{DD} = 5 V

at specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	V _{IC} = 0 V, V _{DD±} = ±2.5 V, V _O = 0 V, R _S = 50 Ω	TLC2272		300	2500	μV
			TLC2272A		300	950	
			TLC2272	Full Range ⁽¹⁾		3000	
			TLC2272A			1500	
α _{VIO}	Temperature coefficient of input offset voltage	V _{IC} = 0 V, V _{DD±} = ±2.5 V, V _O = 0 V, R _S = 50 Ω			2		μV/°C
	Input offset voltage long-term drift ⁽²⁾	V _{IC} = 0 V, V _{DD±} = ±2.5 V, V _O = 0 V, R _S = 50 Ω			0.002		μV/mo
I _{IO}	Input offset current	V _{IC} = 0 V, V _{DD±} = ±2.5 V, V _O = 0 V, R _S = 50 Ω	All level parts	T _A = 25°C	0.5	60	pA
			C level part	T _A = 0°C to 80°C		100	
			I level part	T _A = -40°C to 85°C		150	
			Q level part	T _A = -40°C to 125°C		800	
			M level part	T _A = -55°C to 125°C		800	
I _{IB}	Input bias current	V _{IC} = 0 V, V _{DD±} = ±2.5 V, V _O = 0 V, R _S = 50 Ω	All level parts	T _A = 25°C	1	60	pA
			C level part	T _A = 0°C to 80°C		100	
			I level part	T _A = -40°C to 85°C		150	
			Q level part	T _A = -40°C to 125°C		800	
			M level part	T _A = -55°C to 125°C		800	
V _{ICR}	Common-mode input voltage	R _S = 50 Ω; V _{IO} ≤ 5 mV		T _A = 25°C	-0.3	2.5	V
				Full Range ⁽¹⁾	0	2.5	

(1) T_A = -55°C to 125°C.

(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272 and TLC2272A Electrical Characteristics $V_{DD} = 5\text{ V}$ (continued)

at specified free-air temperature, $V_{DD} = 5\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V _{OH}	High-level output voltage	I _{OH} = −20 μA			4.99		V	
		I _{OH} = −200 μA	T _A = 25°C	4.85	4.93			
			Full Range ⁽¹⁾	4.85				
		I _{OH} = −1 mA	T _A = 25°C	4.25	4.65			
			Full Range ⁽¹⁾	4.25				
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V	I _{OL} = 50 μA		0.01		V	
			I _{OL} = 500 μA	T _A = 25°C		0.09		0.15
				Full Range ⁽¹⁾				0.15
			I _{OL} = 5 mA	T _A = 25°C		0.9		1.5
				Full Range ⁽¹⁾				1.5
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V; R _L = 10 kΩ ⁽³⁾	C level part	T _A = 25°C	15	35	V/mV	
				T _A = 0°C to 80°C	15			
			I level part	T _A = 25°C	15	35		
				T _A = −40°C to 85°C	15			
			Q level part	T _A = 25°C	10	35		
				T _A = −40°C to 125°C	10			
			M level part	T _A = 25°C	10	35		
				T _A = −55°C to 125°C	10			
			V _{IC} = 2.5 V, V _O = 1 V to 4 V; R _L = 1 MΩ ⁽³⁾			175		
r _{id}	Differential input resistance			10 ¹²		Ω		
r _i	Common-mode input resistance			10 ¹²		Ω		
C _i	Common-mode input capacitance	f = 10 kHz, P package			8		pF	
Z _o	Closed-loop output impedance	f = 1 MHz, A _v = 10			140		Ω	
CMRR	Common-mode rejection ratio	V _{IC} = 0 V to 2.7 V, V _O = 2.5 V, R _S = 50 Ω	T _A = 25°C	70	75	dB		
			Full Range ⁽¹⁾	70				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} / ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} / 2, no load	T _A = 25°C	80	95	dB		
			Full Range ⁽¹⁾	80				
I _{DD}	Supply current	V _O = 2.5 V, no load	T _A = 25°C		2.2	3	mA	
			Full Range ⁽¹⁾			3		
SR	Slew rate at unity gain	V _O = 0.5 V to 2.5 V, R _L = 10 kΩ ⁽³⁾ , C _L = 100 pF ⁽³⁾	T _A = 25°C	2.3	3.6	V/μs		
			Full Range ⁽¹⁾	1.7				
V _n	Equivalent input noise voltage	f = 10 Hz			50	nV/√Hz		
		f = 1 kHz			9			
V _{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			1	μV		
		f = 0.1 Hz to 10 Hz			1.4			
I _n	Equivalent input noise current				0.6	fA/√Hz		
THD+N	Total harmonic distortion + noise	V _O = 0.5 V to 2.5 V, f = 20 kHz, R _L = 10 kΩ ⁽³⁾	A _v = 1		0.0013%			
			A _v = 10		0.004%			
			A _v = 100		0.03%			
	Gain-bandwidth product	f = 10 kHz, R _L = 10 kΩ ⁽³⁾ , C _L = 100 pF ⁽³⁾			2.18	MHz		
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, A _v = 1, R _L = 10 kΩ ⁽³⁾ , C _L = 100 pF ⁽³⁾			1	MHz		
t _s	Settling time	A _v = −1, R _L = 10 kΩ ⁽³⁾ , Step = 0.5 V to 2.5 V, C _L = 100 pF ⁽³⁾	To 0.1%		1.5	μs		
			To 0.01%		2.6			
Φ _m	Phase margin at unity gain	R _L = 10 kΩ ⁽³⁾ , C _L = 100 pF ⁽³⁾			50°			
	Gain margin	R _L = 10 kΩ ⁽³⁾ , C _L = 100 pF ⁽³⁾			10	dB		

TLC2272 and TLC2272A Electrical Characteristics $V_{DD\pm} = \pm 5\text{ V}$

at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω	TLC2272	T _A = 25°C		300	2500	μV
			TLC2272A			300	950	
			TLC2272	Full Range ⁽¹⁾			3000	
			TLC2272A				1500	
α _{VIO}	Temperature coefficient of input offset voltage	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω				2		μV/°C
	Input offset voltage long-term drift ⁽²⁾	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω				0.002		μV/mo
I _{IO}	Input offset current	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω	All level parts	T _A = 25°C		0.5	60	pA
			C level part	T _A = 0°C to 80°C			100	
			I level part	T _A = −40°C to 85°C			150	
			Q level part	T _A = −40°C to 125°C			800	
			M level part	T _A = −55°C to 125°C			800	
I _{IB}	Input bias current	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω	All level parts	T _A = 25°C		1	60	pA
			C level part	T _A = 0°C to 80°C			100	
			I level part	T _A = −40°C to 85°C			150	
			Q level part	T _A = −40°C to 125°C			800	
			M level part	T _A = −55°C to 125°C			800	
V _{ICR}	Common-mode input voltage	R _S = 50 Ω; V _{IO} ≤ 5 mV		T _A = 25°C	−5.3	0	4	V
				Full Range ⁽¹⁾	−5	0	3.5	
V _{OM+}	Maximum positive peak output voltage	I _O = −20 μA				4.99		V
		I _O = −200 μA		T _A = 25°C	4.85	4.93		
				Full Range ⁽¹⁾	4.85			
		I _O = −1 mA		T _A = 25°C	4.25	4.65		
Full Range ⁽¹⁾	4.25							
V _{OM-}	Maximum negative peak output voltage	V _{IC} = 0 V,	I _O = 50 μA			−4.99		V
			I _O = 500 μA	T _A = 25°C	−4.85	−4.91		
				Full Range ⁽¹⁾	−4.85			
			I _O = 5 mA	T _A = 25°C	−3.5	−4.1		
A _{VD}		V _O = ±4 V; R _L = 10 kΩ	C level part	T _A = 25°C	25	50		V/mV
				T _A = 0°C to 80°C	25			
			I level part	T _A = 25°C	25	50		
				T _A = −40°C to 85°C	25			
			Q level part	T _A = 25°C	20	50		
				T _A = −40°C to 125°C	20			
			M level part	T _A = 25°C	20	50		
				T _A = −55°C to 125°C	20			
V _O = ±4 V; R _L = 1 MΩ					300			
r _{id}	Differential input resistance					10 ¹²		Ω
r _i	Common-mode input resistance					10 ¹²		Ω
C _i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z _o	Closed-loop output impedance	f = 1 MHz, A _v = 10				130		Ω
CMRR	Common-mode rejection ratio	V _{IC} = −5 V to 2.7 V, V _O = 0 V, R _S = 50 Ω		T _A = 25°C	75	80		dB
				Full Range ⁽¹⁾	75			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} / ΔV _{IO})	V _{DD+} = 2.2 V to ±8 V, V _{IC} = 0 V, no load		T _A = 25°C	80	95		dB
				Full Range ⁽¹⁾	80			
I _{DD}	Supply current	V _O = 0 V, no load		T _A = 25°C		2.4	3	mA
				Full Range ⁽¹⁾			3	

(1) $T_A = -55^\circ\text{C}$ to 125°C .

(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272 and TLC2272A Electrical Characteristics $V_{DD\pm} = \pm 5\text{ V}$

at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	$T_A = 25^\circ\text{C}$	2.3	3.6		V/ μs
			Full Range ⁽¹⁾	1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$			50		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$			1		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$			1.4		
I_n	Equivalent input noise current				0.6		fA/ $\sqrt{\text{Hz}}$
THD+N	Total harmonic distortion + noise	$V_O = \pm 2.3$, $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega$	$A_V = 1$		0.0011%		
			$A_V = 10$		0.004%		
			$A_V = 100$		0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $A_V = 1$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$			0.54		MHz
t_s	Settling time	$A_V = -1$, $R_L = 10\text{ k}\Omega$, Step = $-2.3\text{ V to }2.3\text{ V}$, $C_L = 100\text{ pF}$	To 0.1%		1.5		μs
			To 0.01%		3.2		
Φ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$			52°		
	Gain margin	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$			10		dB

TLC2274 and TLC2274A Electrical Characteristics $V_{DD} = 5\text{ V}$

at specified free-air temperature, $V_{DD} = 5\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	V _{IC} = 0 V, V _{DD±} = ±2.5 V, V _O = 0 V, R _S = 50 Ω	TLC2274	T _A = 25°C		300	2500	μV
			TLC2274A			300	950	
			TLC2274	Full Range ⁽¹⁾			3000	
			TLC2274A				1500	
α _{VIO}	Temperature coefficient of input offset voltage	V _{IC} = 0 V, V _{DD±} = ±2.5 V, V _O = 0 V, R _S = 50 Ω				2		μV/°C
	Input offset voltage long-term drift ⁽²⁾	V _{IC} = 0 V, V _{DD±} = ±2.5 V, V _O = 0 V, R _S = 50 Ω				0.002		μV/mo
I _{IO}	Input offset current	V _{IC} = 0 V, V _{DD±} = ±2.5 V, V _O = 0 V, R _S = 50 Ω	All level parts	T _A = 25°C		0.5	60	pA
			C level part	T _A = 0°C to 80°C			100	
			I level part	T _A = −40°C to 85°C			150	
			Q level part	T _A = −40°C to 125°C			800	
			M level part	T _A = −55°C to 125°C			800	
I _{IB}	Input bias current	V _{IC} = 0 V, V _{DD±} = ±2.5 V, V _O = 0 V, R _S = 50 Ω	All level parts	T _A = 25°C		1	60	pA
			C level part	T _A = 0°C to 80°C			100	
			I level part	T _A = −40°C to 85°C			150	
			Q level part	T _A = −40°C to 125°C			800	
			M level part	T _A = −55°C to 125°C			800	
V _{ICR}	Common-mode input voltage	R _S = 50 Ω; V _{IO} ≤ 5 mV	T _A = 25°C	−0.3	2.5	4	V	
			Full Range ⁽¹⁾	0	2.5	3.5		
V _{OH}	High-level output voltage	I _{OH} = −20 μA				4.99		V
		I _{OH} = −200 μA		T _A = 25°C	4.85	4.93		
				Full Range ⁽¹⁾	4.85			
		I _{OH} = −1 mA		T _A = 25°C	4.25	4.65		
				Full Range ⁽¹⁾	4.25			

(1) $T_A = -55^\circ\text{C to }125^\circ\text{C}$.

(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274 and TLC2274A Electrical Characteristics $V_{DD} = 5\text{ V}$

at specified free-air temperature, $V_{DD} = 5\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	$V_{IC} = 2.5\text{ V}$	$I_{OL} = 50\text{ }\mu\text{A}$		0.01		V
			$I_{OL} = 500\text{ }\mu\text{A}$	$T_A = 25^\circ\text{C}$	0.09	0.15	
				Full Range ⁽¹⁾		0.15	
			$I_{OL} = 5\text{ mA}$	$T_A = 25^\circ\text{C}$	0.9	1.5	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V}$ to 4 V ; $R_L = 10\text{ k}\Omega$ ⁽³⁾	C level part	$T_A = 25^\circ\text{C}$	15	35	V/mV
				$T_A = 0^\circ\text{C}$ to 80°C	15		
			I level part	$T_A = 25^\circ\text{C}$	15	35	
				$T_A = -40^\circ\text{C}$ to 85°C	15		
			Q level part	$T_A = 25^\circ\text{C}$	10	35	
				$T_A = -40^\circ\text{C}$ to 125°C	10		
			M level part	$T_A = 25^\circ\text{C}$	10	35	
				$T_A = -55^\circ\text{C}$ to 125°C	10		
		$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V}$ to 4 V ; $R_L = 1\text{ M}\Omega$ ⁽³⁾			175		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
C_i	Common-mode input capacitance	$f = 10\text{ kHz}$, P package			8		pF
Z_o	Closed-loop output impedance	$f = 1\text{ MHz}$, $A_V = 10$			140		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ V}$ to 2.7 V , $V_O = 2.5\text{ V}$, $R_S = 50\text{ }\Omega$	$T_A = 25^\circ\text{C}$	70	75		dB
			Full Range ⁽¹⁾	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 4.4\text{ V}$ to 16 V , $V_{IC} = V_{DD} / 2$, no load	$T_A = 25^\circ\text{C}$	80	95		dB
			Full Range ⁽¹⁾	80			
I_{DD}	Supply current	$V_O = 2.5\text{ V}$, no load	$T_A = 25^\circ\text{C}$		4.4	6	mA
			Full Range ⁽¹⁾			6	
SR	Slew rate at unity gain	$V_O = 0.5\text{ V}$ to 2.5 V , $R_L = 10\text{ k}\Omega$ ⁽³⁾ , $C_L = 100\text{ pF}$ ⁽³⁾	$T_A = 25^\circ\text{C}$	2.3	3.6		V/ μs
			Full Range ⁽¹⁾	1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$			50		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz}$ to 1 Hz			1		μV
		$f = 0.1\text{ Hz}$ to 10 Hz			1.4		
I_n	Equivalent input noise current				0.6		fA/ $\sqrt{\text{Hz}}$
THD+N	Total harmonic distortion + noise	$V_O = 0.5\text{ V}$ to 2.5 V , $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega$ ⁽³⁾	$A_V = 1$		0.0013%		
			$A_V = 10$		0.004%		
			$A_V = 100$		0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$ ⁽³⁾ , $C_L = 100\text{ pF}$ ⁽³⁾			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $A_V = 1$, $R_L = 10\text{ k}\Omega$ ⁽³⁾ , $C_L = 100\text{ pF}$ ⁽³⁾			1		MHz
t_s	Settling time	$A_V = -1$, $R_L = 10\text{ k}\Omega$ ⁽³⁾ , Step = 0.5 V to 2.5 V , $C_L = 100\text{ pF}$ ⁽³⁾	To 0.1%		1.5		μs
			To 0.01%		2.6		
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ ⁽³⁾ , $C_L = 100\text{ pF}$ ⁽³⁾			50°		
	Gain margin	$R_L = 10\text{ k}\Omega$ ⁽³⁾ , $C_L = 100\text{ pF}$ ⁽³⁾			10		dB

TLC2274 and TLC2274A Electrical Characteristics $V_{DD\pm} = \pm 5\text{ V}$

at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω	TLC2274	T _A = 25°C			300	2500	μV
			TLC2274A			300	950		
			TLC2274	Full Range ⁽¹⁾			3000		
			TLC2274A			1500			
α _{VIO}	Temperature coefficient of input offset voltage	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω				2		μV/°C	
	Input offset voltage long-term drift ⁽²⁾	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω				0.002		μV/mo	
I _{IO}	Input offset current	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω	All level parts	T _A = 25°C		0.5	60	pA	
			C level part	T _A = 0°C to 80°C			100		
			I level part	T _A = –40°C to 85°C			150		
			Q level part	T _A = –40°C to 125°C			800		
			M level part	T _A = –55°C to 125°C			800		
I _{IB}	Input bias current	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω	All level parts	T _A = 25°C		1	60	pA	
			C level part	T _A = 0°C to 80°C			100		
			I level part	T _A = –40°C to 85°C			150		
			Q level part	T _A = –40°C to 125°C			800		
			M level part	T _A = –55°C to 125°C			800		
V _{ICR}	Common-mode input voltage	R _S = 50 Ω; V _{IO} ≤ 5 mV		T _A = 25°C	–5.3	0	4	V	
				Full Range ⁽¹⁾	–5	0	3.5		
V _{OM+}	Maximum positive peak output voltage	I _O = –20 μA				4.99		V	
		I _O = –200 μA		T _A = 25°C	4.85	4.93			
				Full Range ⁽¹⁾	4.85				
		I _O = –1 mA		T _A = 25°C	4.25	4.65			
Full Range ⁽¹⁾	4.25								
V _{OM-}	Maximum negative peak output voltage	V _{IC} = 0 V	I _O = 50 μA			–4.99		V	
			I _O = 500 μA	T _A = 25°C	–4.85	–4.91			
				Full Range ⁽¹⁾	–4.85				
			I _O = 5 mA	T _A = 25°C	–3.5	–4.1			
A _{VD}		V _O = ±4 V; R _L = 10 kΩ	C level part	T _A = 25°C	25	50		V/mV	
				T _A = 0°C to 80°C	25				
			I level part	T _A = 25°C	25	50			
				T _A = –40°C to 85°C	25				
			Q level part	T _A = 25°C	20	50			
				T _A = –40°C to 125°C	20				
			M level part	T _A = 25°C	20	50			
				T _A = –55°C to 125°C	20				
		V _O = ±4 V; R _L = 1 MΩ			300				
r _{id}	Differential input resistance					10 ¹²		Ω	
r _i	Common-mode input resistance					10 ¹²		Ω	
c _i	Common-mode input capacitance	f = 10 kHz, P package				8		pF	
z _o	Closed-loop output impedance	f = 1 MHz, A _V = 10				130		Ω	
CMRR	Common-mode rejection ratio	V _{IC} = –5 V to 2.7 V, V _O = 0 V, R _S = 50 Ω		T _A = 25°C	75	80		dB	
				Full Range ⁽¹⁾	75				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} / ΔV _{IO})	V _{DD+} = 2.2 V to ±8 V, V _{IC} = 0 V, no load		T _A = 25°C	80	95		dB	
				Full Range ⁽¹⁾	80				
I _{DD}	Supply current	V _O = 0 V, no load		T _A = 25°C		4.8	6	mA	
				Full Range ⁽¹⁾			6		

(1) $T_A = -55^\circ\text{C}$ to 125°C .

(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274 and TLC2274A Electrical Characteristics $V_{DD\pm} = \pm 5\text{ V}$

at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	$T_A = 25^\circ\text{C}$	2.3	3.6		V/ μs
			Full Range ⁽¹⁾	1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$			50		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$			1		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$			1.4		
I_n	Equivalent input noise current				0.6		fA/ $\sqrt{\text{Hz}}$
THD+N	Total harmonic distortion + noise	$V_O = \pm 2.3$, $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega$	$A_V = 1$		0.0011%		
			$A_V = 10$		0.004%		
			$A_V = 100$		0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $A_V = 1$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$			0.54		MHz
t_s	Settling time	$A_V = -1$, $R_L = 10\text{ k}\Omega$, Step = $-2.3\text{ V to }2.3\text{ V}$, $C_L = 100\text{ pF}$	To 0.1%		1.5		μs
			To 0.01%		3.2		
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$			52°		
	Gain margin	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$			10		dB

Typical Characteristics

Table 1. Table of Graphs

			FIGURE ⁽¹⁾
V_{IO}	Input offset voltage	Distribution	1, 2, 3, 4
		vs Common-mode voltage	5, 6
α_{VIO}	Input offset voltage temperature coefficient	Distribution	7, 8, 9, 10 ⁽²⁾
I_{IB}/I_{IO}	Input bias and input offset current	vs Free-air temperature	11 ⁽²⁾
V_I	Input voltage	vs Supply voltage	12
		vs Free-air temperature	13 ⁽²⁾
V_{OH}	High-level output voltage	vs High-level output current	14 ⁽²⁾
V_{OL}	Low-level output voltage	vs Low-level output current	15, 16 ⁽²⁾
V_{OM+}	Maximum positive peak output voltage	vs Output current	17 ⁽²⁾
V_{OM-}	Maximum negative peak output voltage	vs Output current	18 ⁽²⁾
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	19
I_{OS}	Short-circuit output current	vs Supply voltage	20
		vs Free-air temperature	21 ⁽²⁾
V_O	Output voltage	vs Differential input voltage	22, 23
A_{VD}	Large-signal differential voltage amplification	vs Load resistance	24
	Large-signal differential voltage amplification and phase margin	vs Frequency	25, 26
	Large-signal differential voltage amplification	vs Free-air temperature	27 ⁽²⁾ , 28 ⁽²⁾
Z_O	Output impedance	vs Frequency	29, 30
CMRR	Common-mode rejection ratio	vs Frequency	31
		vs Free-air temperature	32
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	33, 34
		vs Free-air temperature	35 ⁽²⁾
I_{DD}	Supply current	vs Supply voltage	36 ⁽²⁾ , 37 ⁽²⁾
		vs Free-air temperature	38 ⁽²⁾ , 39 ⁽²⁾
SR	Slew rate	vs Load Capacitance	40
		vs Free-air temperature	41 ⁽²⁾
V_O	Inverting large-signal pulse response		42, 43
	Voltage-follower large-signal pulse response		44, 45
	Inverting small-signal pulse response		46, 47
	Voltage-follower small-signal pulse response		48, 49
V_n	Equivalent input noise voltage	vs Frequency	50, 51
	Noise voltage over a 10-second period		52
	Integrated noise voltage	vs Frequency	53
THD+N	Total harmonic distortion + noise	vs Frequency	54
	Gain-bandwidth product	vs Supply voltage	55
		vs Free-air temperature	56 ⁽²⁾
Φ_m	Phase margin	vs Load capacitance	57
	Gain margin	vs Load capacitance	58

(1) For all graphs where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

(2) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

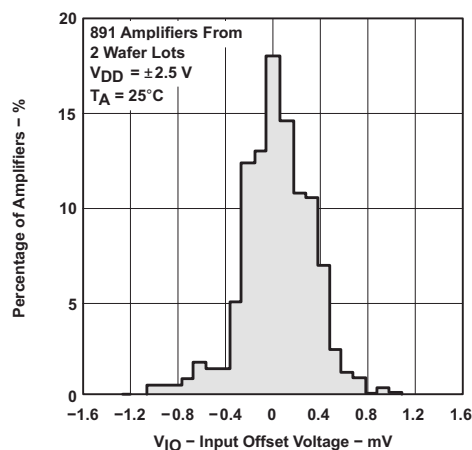


Figure 1. Distribution of TLC2272 Input Offset Voltage

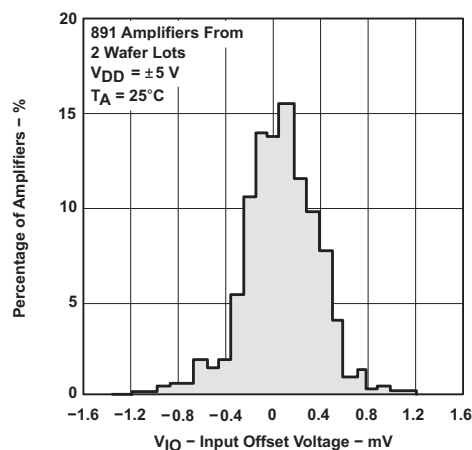


Figure 2. Distribution of TLC2272 Input Offset Voltage

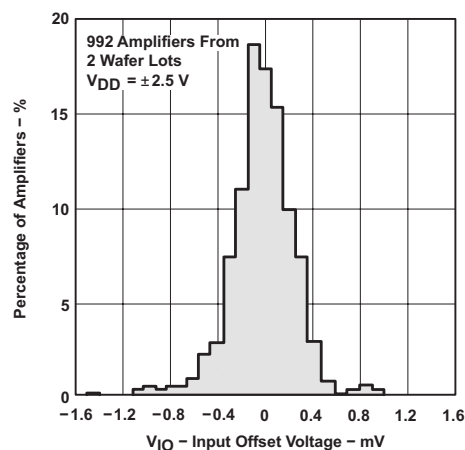


Figure 3. Distribution of TLC2274 Input Offset Voltage

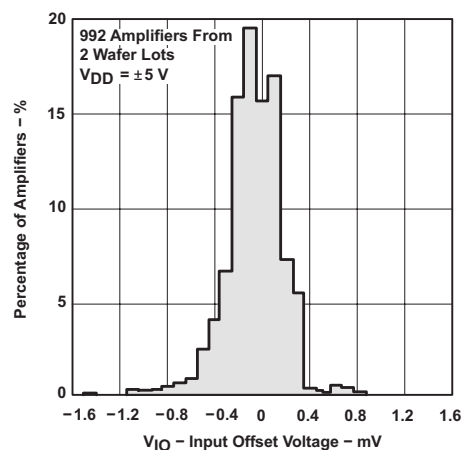


Figure 4. Distribution of TLC2274 Input Offset Voltage

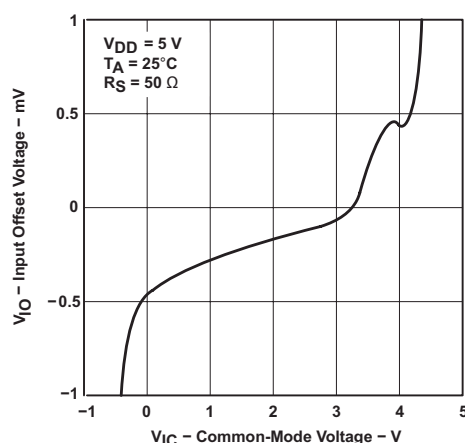


Figure 5. Input Offset Voltage vs Common-Mode Voltage

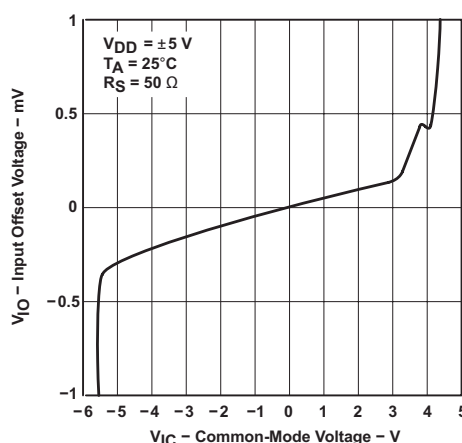


Figure 6. Input Offset Voltage vs Common-Mode Voltage

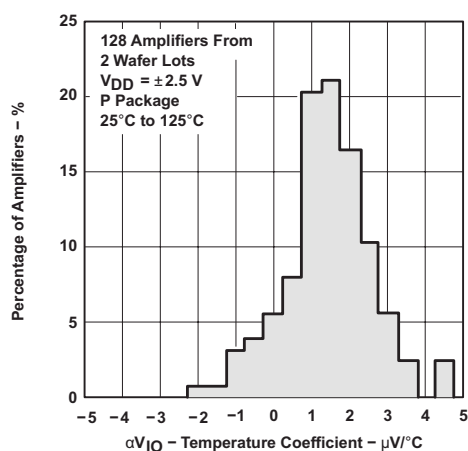


Figure 7. Distribution of TLC2272 vs Input Offset Voltage Temperature Coefficient

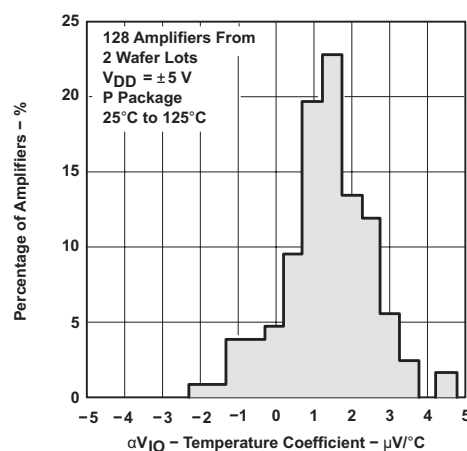


Figure 8. Distribution of TLC2272 vs Input Offset Voltage Temperature Coefficient

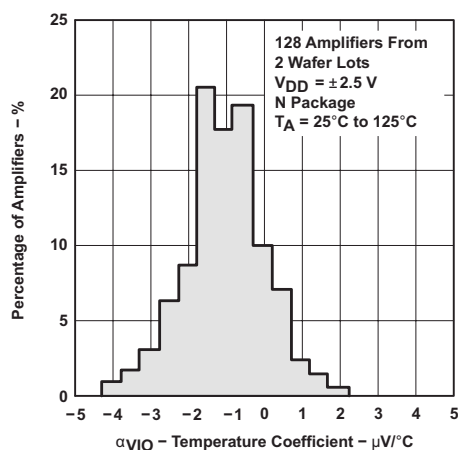


Figure 9. Distribution of TLC2274 vs Input Offset Voltage Temperature Coefficient

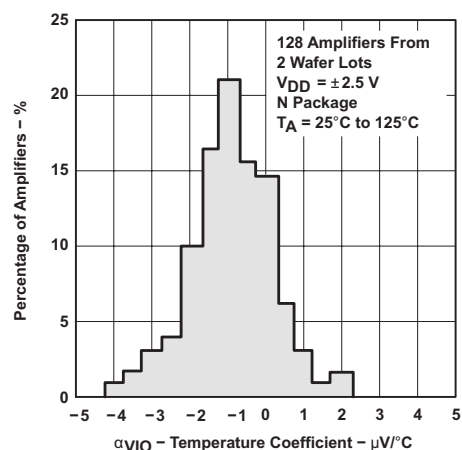


Figure 10. Distribution of TLC2274 vs Input Offset Voltage Temperature Coefficient

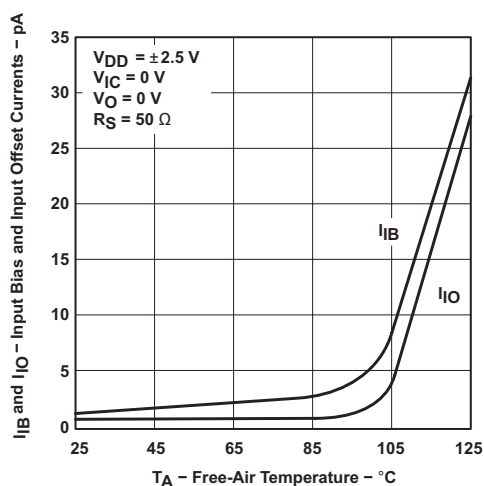


Figure 11. Input Bias and Input Offset Current vs Free-Air Temperature

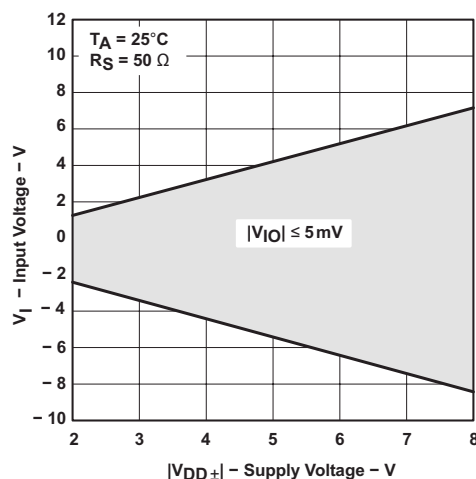


Figure 12. Input Voltage vs Supply Voltage

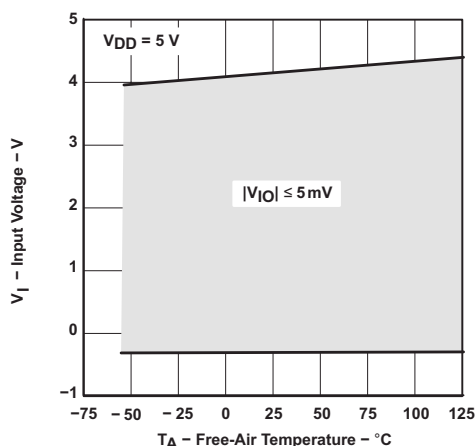


Figure 13. Input Voltage vs Free-Air Temperature

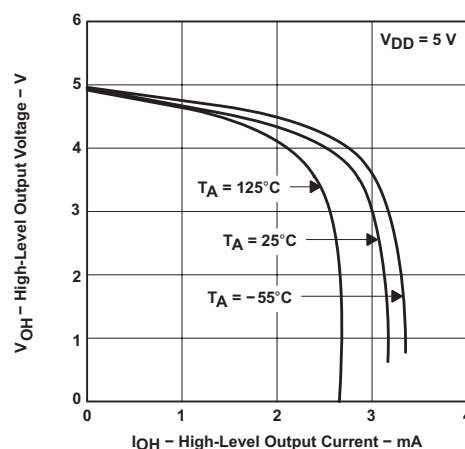


Figure 14. High-Level Output Voltage vs High-Level Output Current

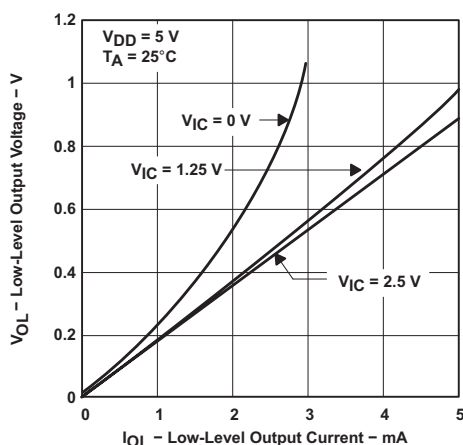


Figure 15. Low-Level Output Voltage vs Low-Level Output Current

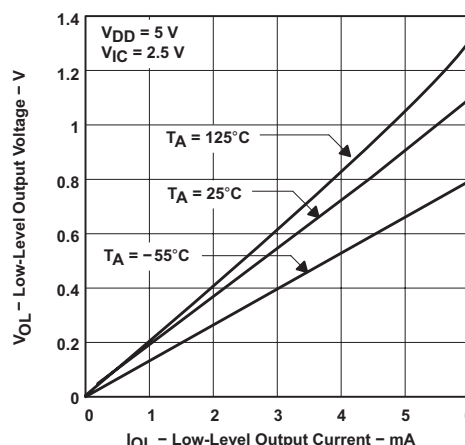


Figure 16. Low-Level Output Voltage vs Low-Level Output Current

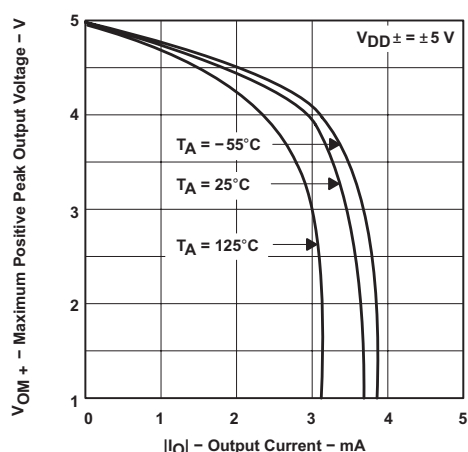


Figure 17. Maximum Positive Peak Output Voltage vs Output Current

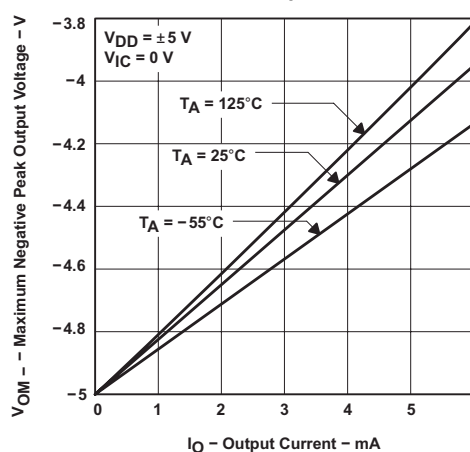


Figure 18. Maximum Positive Peak Output Voltage vs Output Current

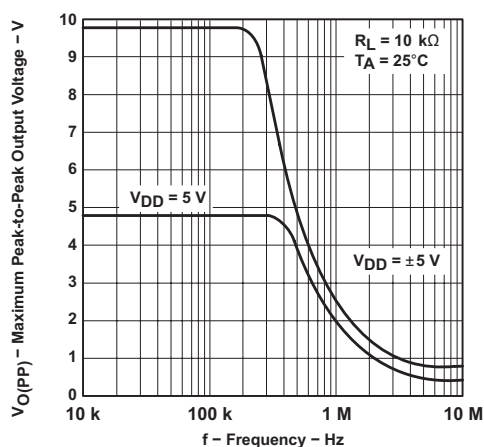


Figure 19. Maximum Peak-to-Peak Output Voltage vs Frequency

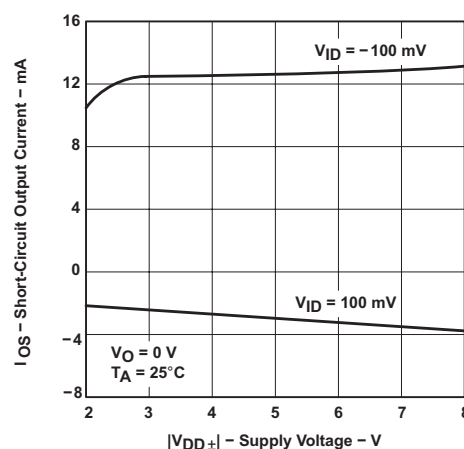


Figure 20. Short-Circuit Output Current vs Supply Voltage

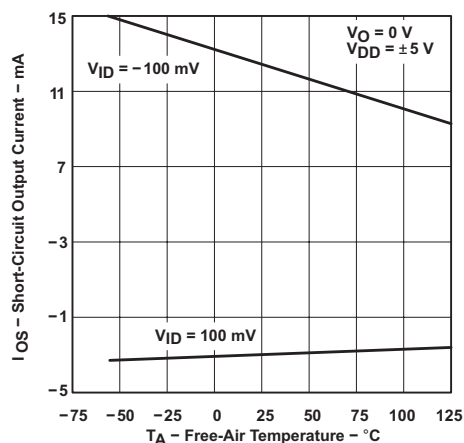


Figure 21. Short-Circuit Output Current vs Free-Air Temperature

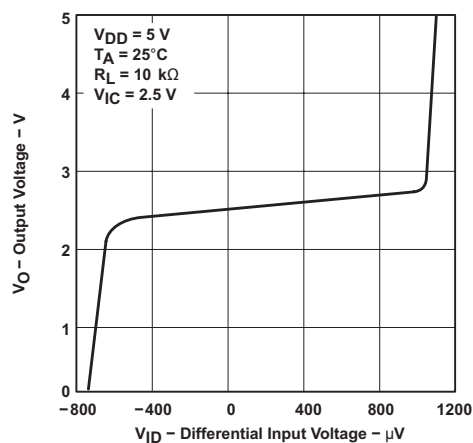


Figure 22. Output Voltage vs Differential Input Voltage

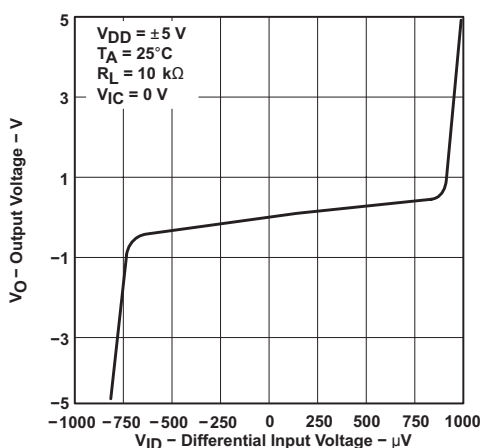


Figure 23. Output Voltage vs Differential Input Voltage

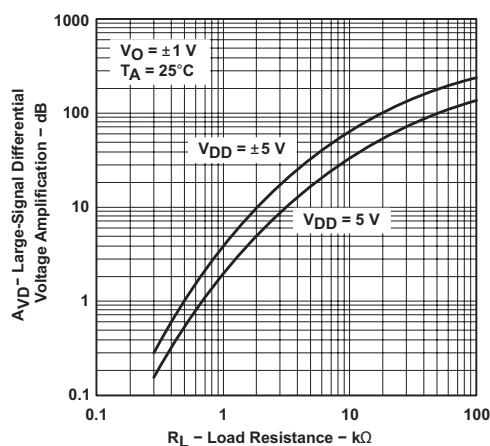


Figure 24. Large-Signal Differential Voltage Amplification vs Load Resistance

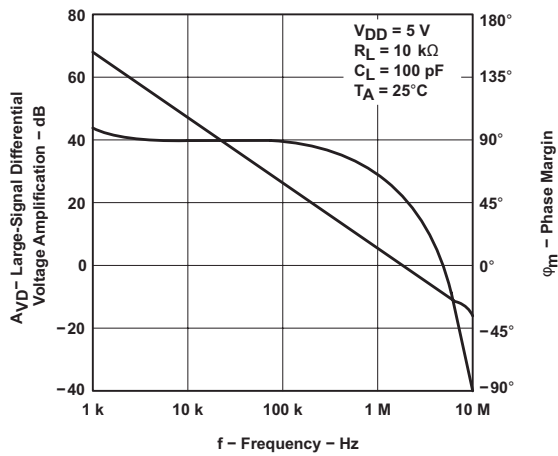


Figure 25. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

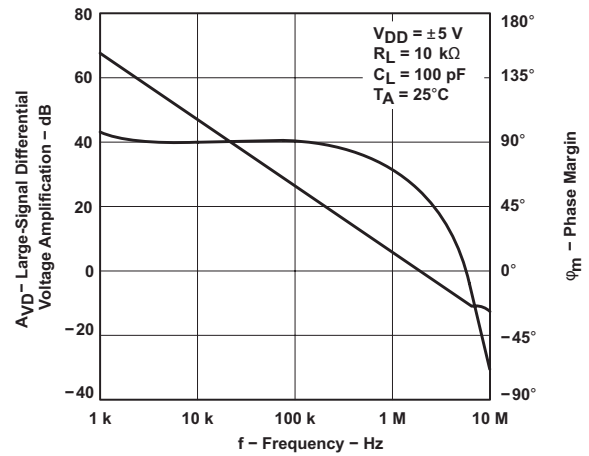


Figure 26. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

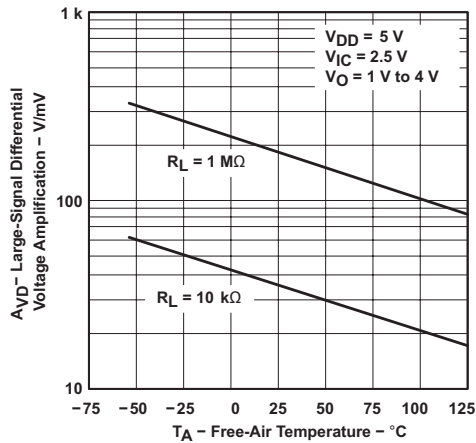


Figure 27. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

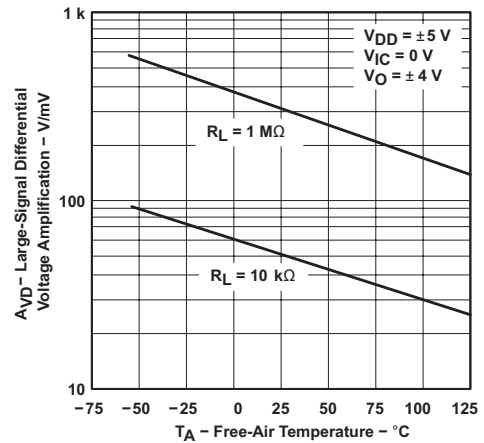


Figure 28. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

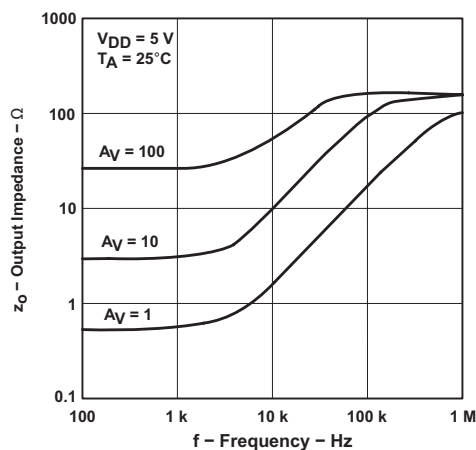


Figure 29. Output Impedance vs Frequency

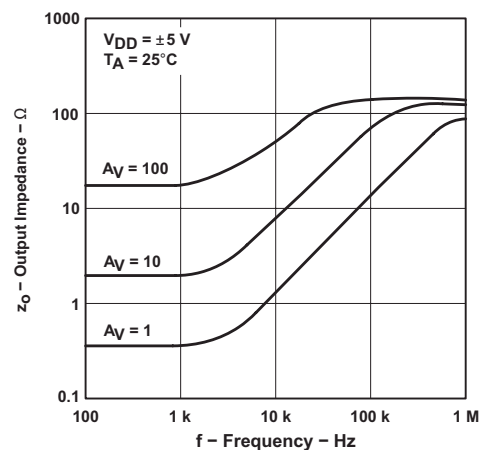


Figure 30. Output Impedance vs Frequency

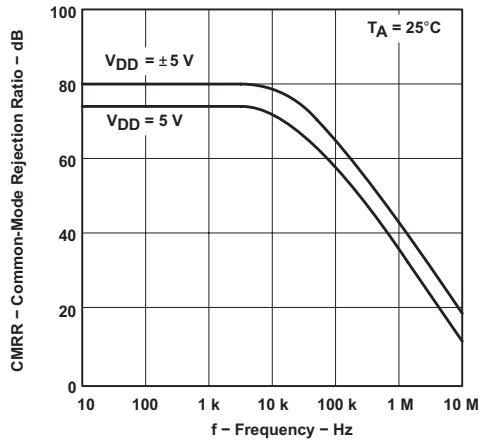


Figure 31. Common-Mode Rejection Ratio vs Frequency

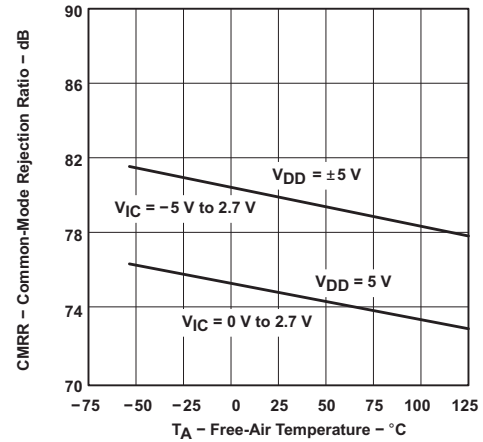


Figure 32. Common-Mode Rejection Ratio vs Free-Air Temperature

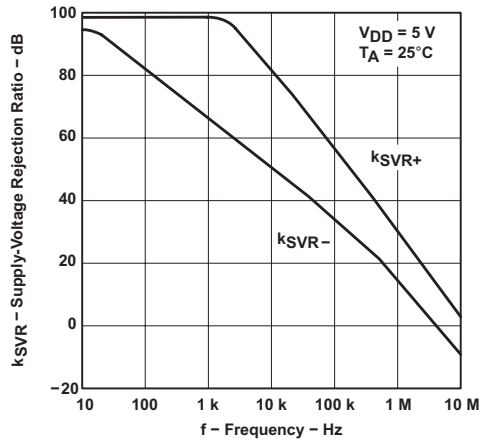


Figure 33. Supply-Voltage Rejection Ratio vs Frequency

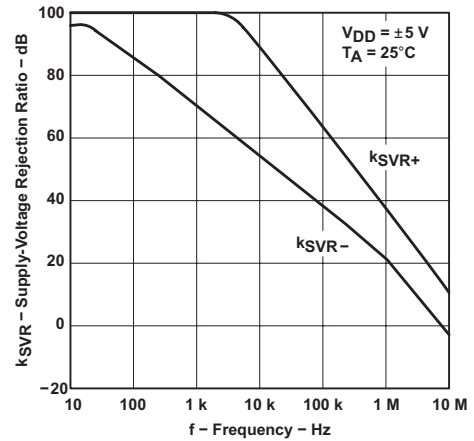


Figure 34. Supply-Voltage Rejection Ratio vs Frequency

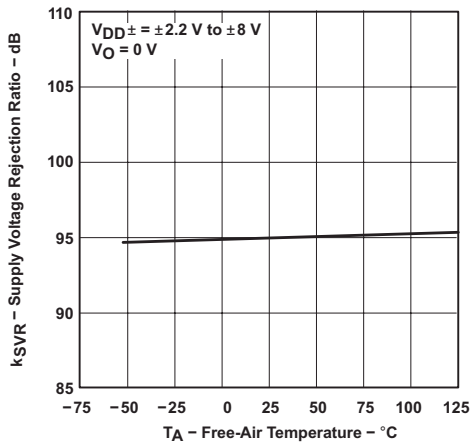


Figure 35. Supply-Voltage Rejection Ratio vs Free-Air Temperature

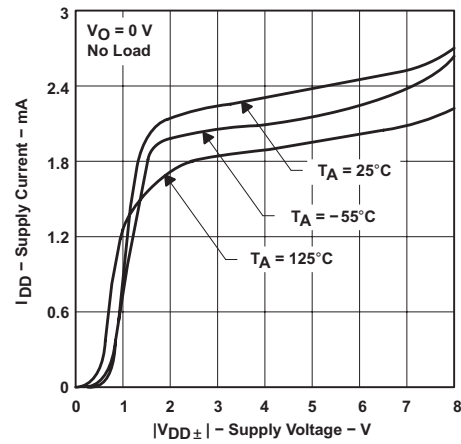


Figure 36. TLC2272 Supply Current vs Supply Voltage

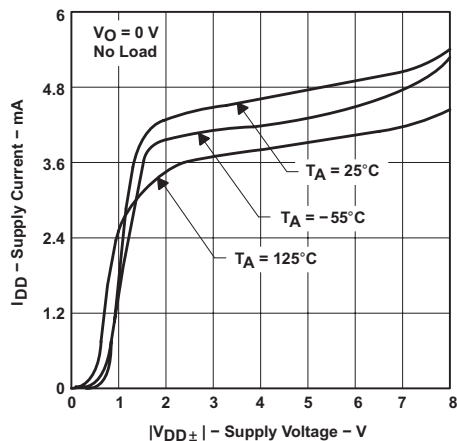


Figure 37. TLC2274 Supply Current vs Supply Voltage

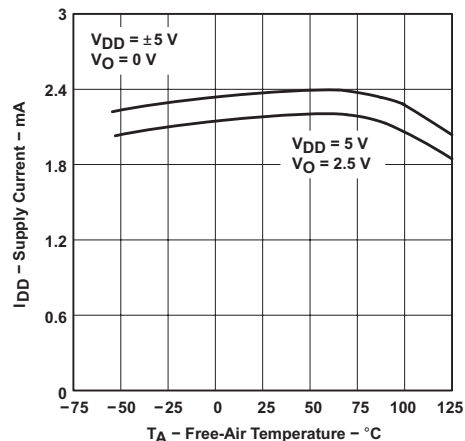


Figure 38. TLC2272 Supply Current vs Free-Air Temperature

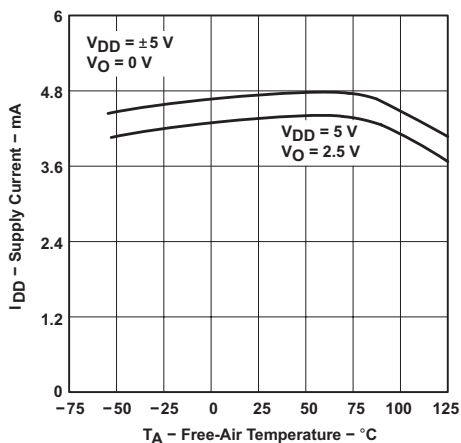


Figure 39. TLC2274 Supply Current vs Free-Air Temperature

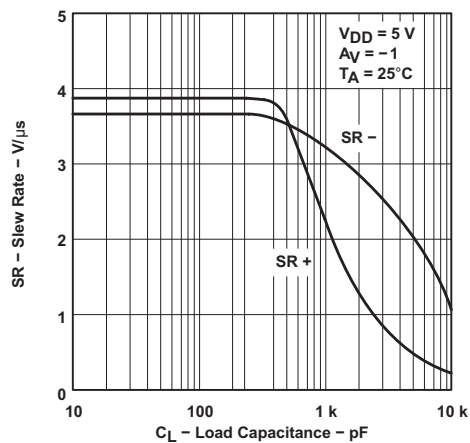


Figure 40. Slew Rate vs Load Capacitance

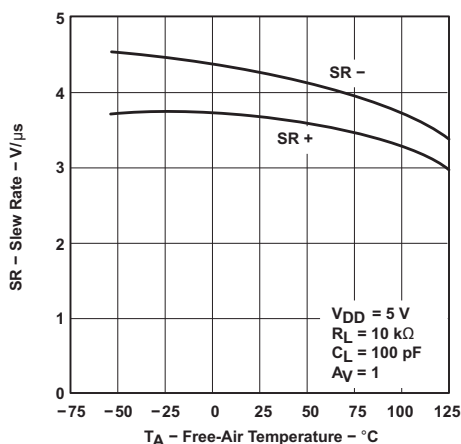


Figure 41. Slew Rate vs Free-Air Temperature

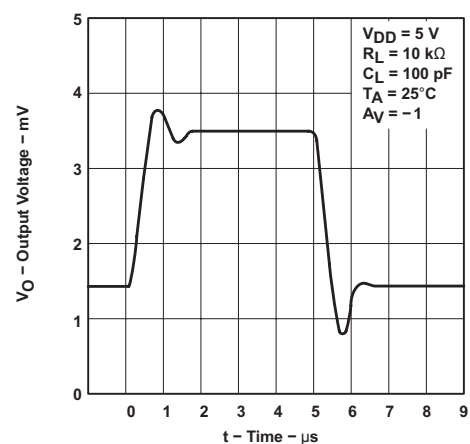


Figure 42. Inverting Large-Signal Pulse Response

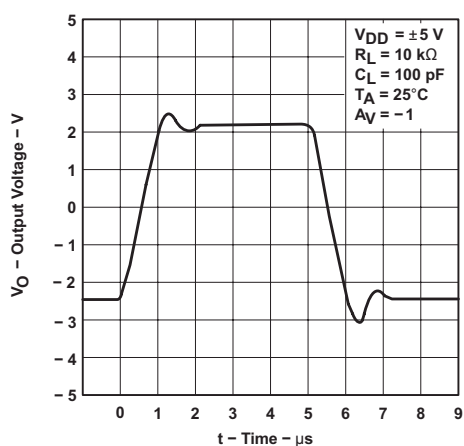


Figure 43. Inverting Large-Signal Pulse Response

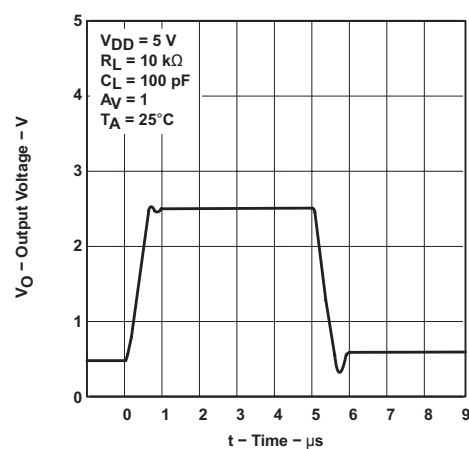


Figure 44. Voltage-Follower Large-Signal Pulse Response

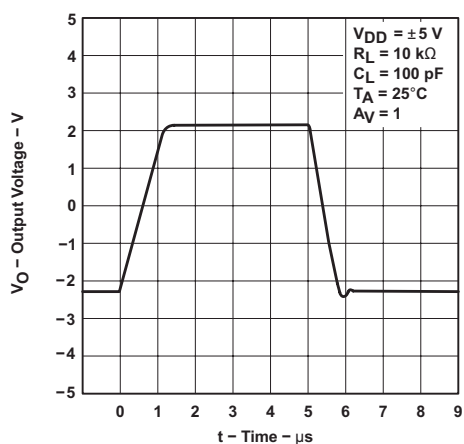


Figure 45. Voltage-Follower Large-Signal Pulse Response

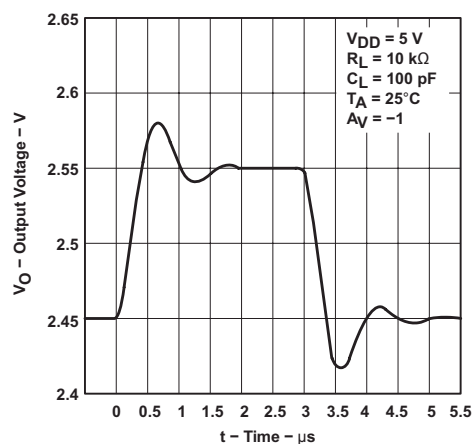


Figure 46. Inverting Small-Signal Pulse Response

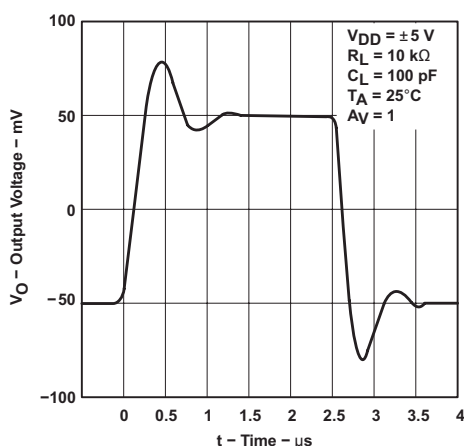


Figure 47. Inverting Small-Signal Pulse Response

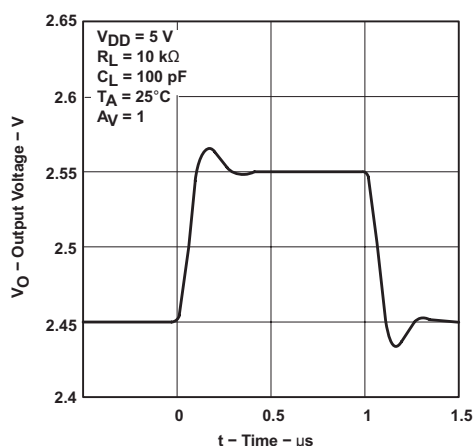


Figure 48. Voltage-Follower Small-Signal Pulse Response

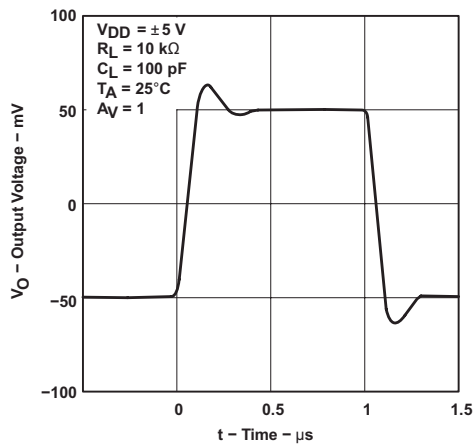


Figure 49. Voltage-Follower Small-Signal Pulse Response

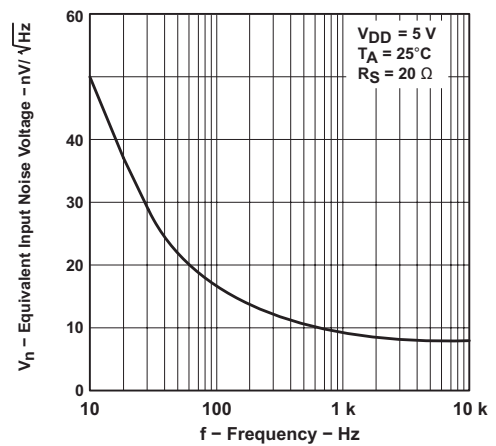


Figure 50. Equivalent Input Noise Voltage vs Frequency

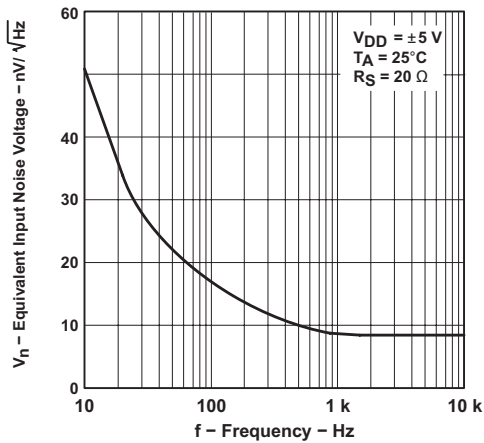


Figure 51. Equivalent Input Noise Voltage vs Frequency

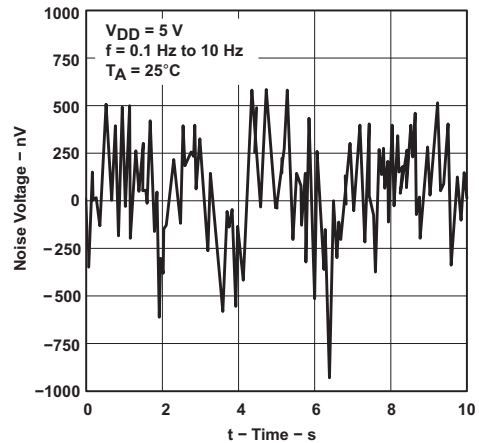


Figure 52. Noise Voltage Over a 10 Second Period

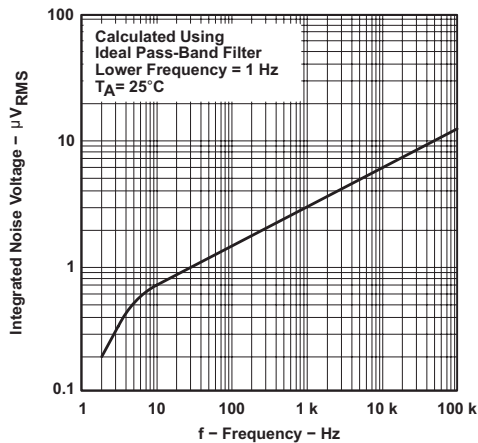


Figure 53. Integrated Noise Voltage vs Frequency

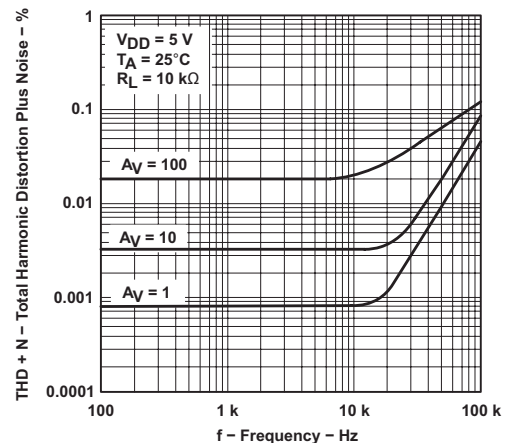


Figure 54. Total Harmonic Distortion + Noise vs Frequency

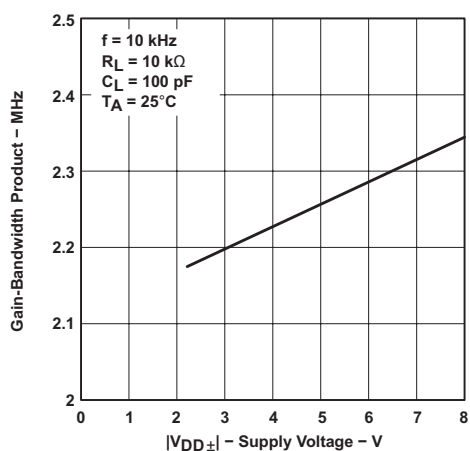


Figure 55. Gain-Bandwidth Product vs Supply Voltage

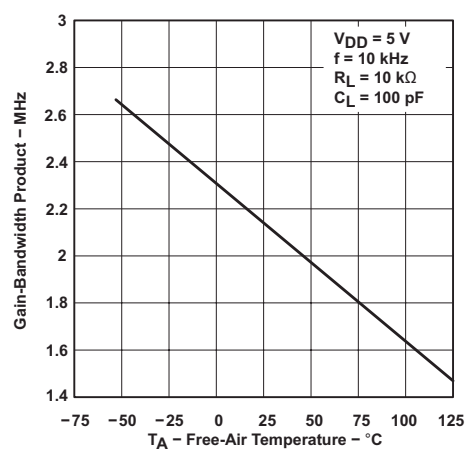


Figure 56. Gain-Bandwidth Product vs Free-Air Temperature

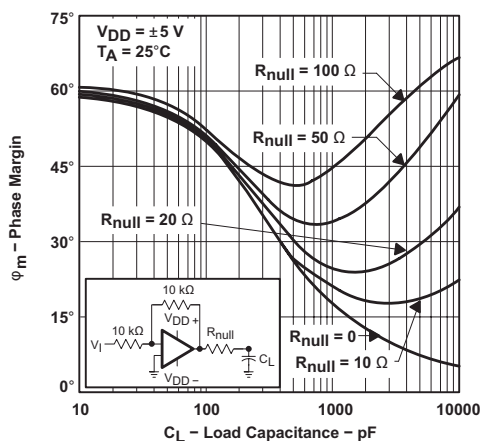


Figure 57. Phase Margin vs Load Capacitance

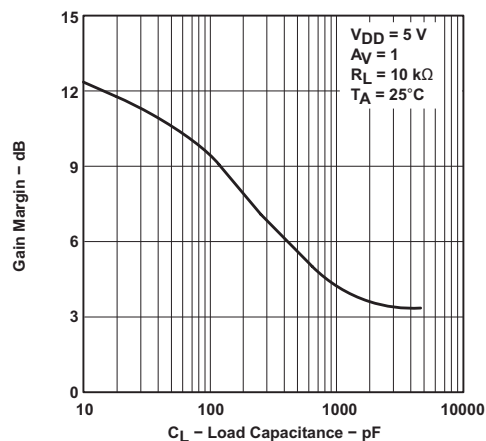
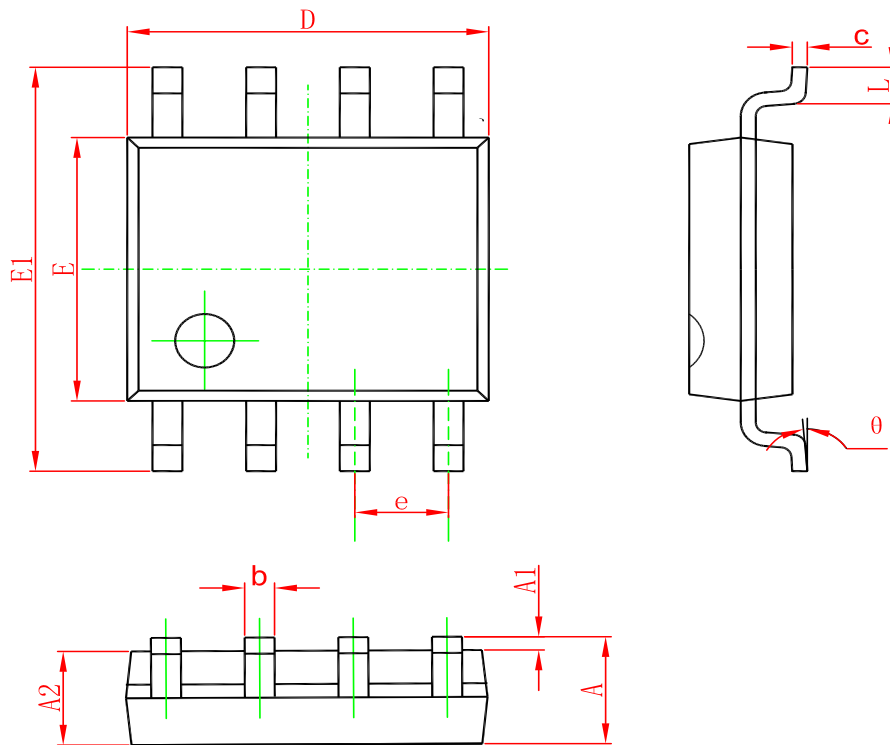


Figure 58. Gain Margin vs Load Capacitance

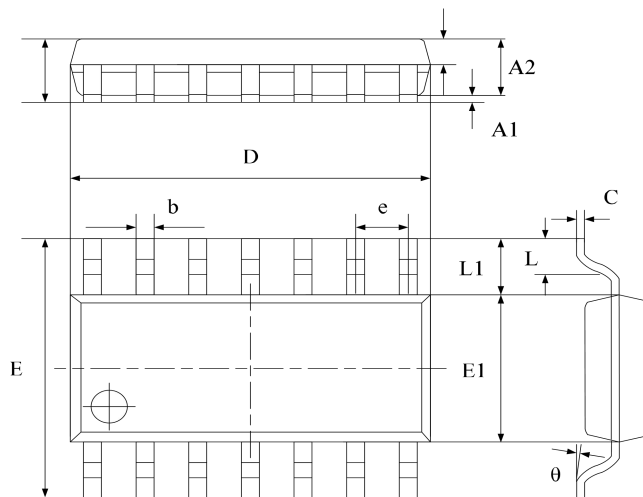
Package Dimension

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.059	0.076
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.055	0.063
A3	0.550	0.750	0.022	0.031
b	0.406typ.		0.017typ.	
C	0.203typ.		0.008typ.	
D	8.630	8.830	0.352	0.360
E	5.840	6.240	0.238	0.255
E1	3.850	4.050	0.157	0.165
e	1.270 typ.		0.050 typ.	
L1	1.040 ref.		0.041 ref.	
L	0.350	0.750	0.014	0.031
θ	2°	8°	2°	8°

Ordering information

Order code	Package	Baseqty	Deliverymode	Marking
UMW TLC2272ACDR	SOP-8	2500	Tape and reel	TLC2272
UMW TLC2272CDR	SOP-8	2500	Tape and reel	TLC2272
UMW TLC2272AIDR	SOP-8	2500	Tape and reel	TLC2272
UMW TLC2272IDR	SOP-8	2500	Tape and reel	TLC2272
UMW TLC2274ACDR	SOP-14	2500	Tape and reel	TLC2274
UMW TLC2274CDR	SOP-14	2500	Tape and reel	TLC2274
UMW TLC2274AIDR	SOP-14	2500	Tape and reel	TLC2274
UMW TLC2274IDR	SOP-14	2500	Tape and reel	TLC2274