

## System PMIC for Mobile and Automotive Applications

### General Description

DA9063 is a high current system PMIC suitable for dual- and quad-core processors used in smartphones, tablets, ultra-books, and other handheld and automotive applications that require up to 5 A core processor supply.

DA9063 contains six DC-DC buck converters designed for small external 1  $\mu$ H inductors capable of supplying in total up to 12 A continuous output (0.3 V to 3.3 V). The buck converters do not require external Schottky diodes. They dynamically optimize their efficiency depending on the load current using an Automatic Sleep mode. The bucks incorporate pin and s/w controlled Dynamic Voltage Control (DVC) to support processor load adaptive adjustment of the supply voltage. One buck can also be used in a DDR memory termination mode.

Eleven SmartMirror™ programmable LDO regulators are incorporated, rated up to 300 mA. All support remote capacitor placement and can support operation from a low 1.5 V/1.8 V input voltage: this allows the linear regulators to be cascaded with a suitable buck supply to improve overall system efficiency.

Processor core leakage can be minimized by using the integrated rail switch controller for ultra-fast power domain isolation/reconnection while current limited switches provide support for external peripherals such as external accessory or memory cards.

There are five distinct operating modes consuming < 20  $\mu$ A including a 1.5  $\mu$ A RTC mode with alarm and wake-up. A system monitor watchdog can be enabled in ACTIVE mode.

The DA9063 provides an OTP start-up sequencing engine that offers autonomous hardware system start-up or software controlled start-up and configurable power modes. The on key detects the button press time and offers configurable key lock and application shutdown functions. Up to 16 freely configurable GPIO pins can perform system functions, including: keypad supervision, application wake-up, and timing controlled external regulator, power switch, or other IC enable.

An integrated 10-channel ADC includes advanced voltage monitoring, internal temperature supervision, three general-purpose channels with programmable high/low thresholds, an integrated current source for resistive measurements, and system voltage monitoring with a programmable low-voltage warning. The ADC has 8-bit resolution in AUTO mode and 10-bit resolution in manual conversion mode.

Three RGB-LED driver pins are provided with PWM control.

LDO8 can be configured as a 6-bit, PWM-controlled, vibration motor driver with automatic battery voltage correction.

## System PMIC for Mobile and Automotive Applications

### Key Features

- 6 DC-DC buck converters with DVC
  - 2.5 A BuckCore1
  - 2.5 A BuckCore2
  - 2.5 A BuckPro
  - 1.5 A BuckPeri
  - 1.5 A BuckMem
  - 1.5 A BuckIO

} 5 A in dual phase mode

} 3 A in merged mode
- 3 MHz switching frequency ( $\pm 10\%$ ) (allows use of low profile [1 mm] 1  $\mu$ H inductors)
- 11 programmable LDO regulators:
  - 3 low noise, 4 with DVC, 5 with current limited switch mode
- Two rail switches
- Power Manager with programmable regulators, rail switch start-up, and configurable low power modes
- Multiple master application support via two independent control interfaces
- System monitor with watchdog timer
- Up to 16 flexible GPIO pins for enhanced wake-up and peripheral control
- RGB-LED driver with autonomous flashing
- PWM vibration motor driver
- 10-bit ADC with nine channels and configurable alarm thresholds
- Regulator supervision with automatic under-/over-voltage protection
- Coin cell/super-capacitor backup charger
- Ultra-low power, 1.5  $\mu$ A RTC with alarm and oscillator circuitry with crystal frequency adjustment
- $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$  junction temperature operation
- Two package variants:
  - 100 VFBGA 8.0 mm x 8.0 mm x 1.0 mm, 0.8 mm pitch, 0.30 mm balls
  - 100 TFBGA 8.0 mm x 8.0 mm x 1.2 mm, 0.8 mm pitch, 0.45 mm balls
- Automotive AEC-Q100 Grade 2 available (DA9063-A)

### Applications

- Smartphones
- Ultrabooks
- Tablets, e-books
- Car infotainment and ADAS
- Navigation devices
- Set-top boxes, TV, and media players
- Portable industrial and medical devices
- IoT devices

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### 1 References

Dialog Semiconductor technical documentation is available on the web site:

[Power Management ICs \(PMICs\)](#).

- [1] AN-PM-068, Application Note, VBAT Current in RTC or DELIVERY Modes, Dialog Semiconductor.
- [2] AN-PM-024, Application Note, DA9063 Voltage Monitoring, Dialog Semiconductor.
- [3] AN-PM-010, Application Note, PCB Layout Guidelines, Dialog Semiconductor.

### 2 Block Diagram

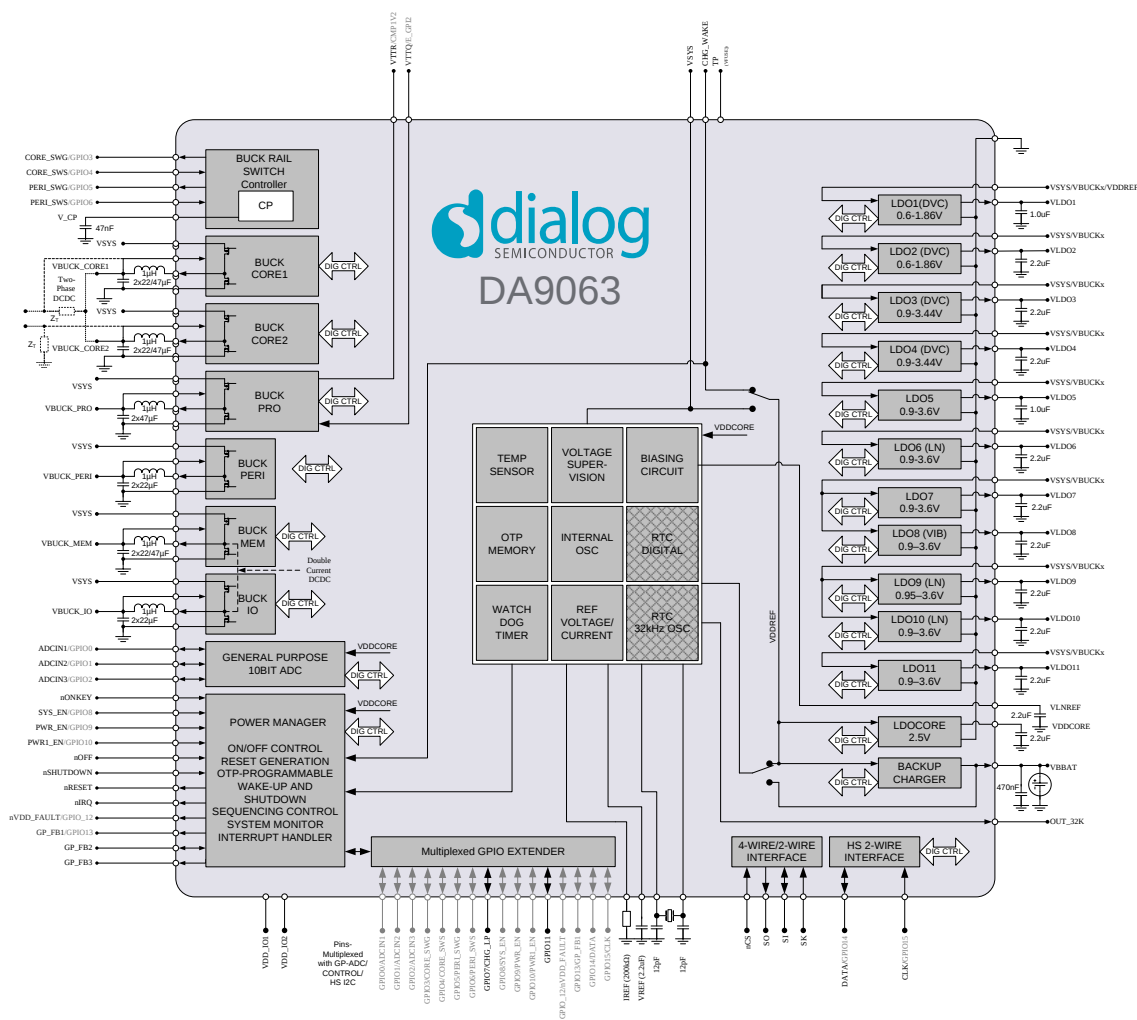


Figure 1: Block Diagram

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### 3 Pinout



Figure 2: Connection Diagram

Table 1: Pin Type Definition

| Pin Type | Description          | Pin Type | Description         |
|----------|----------------------|----------|---------------------|
| DI       | Digital input        | AI       | Analog input        |
| DO       | Digital output       | AO       | Analog output       |
| DIO      | Digital input/output | AIO      | Analog input/output |
| PWR      | Power supply         | GND      | Ground connection   |

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Table 2: Pin Description

| Pin                  | Pin Name   | Alternate Function | Type (Table 1) | Description                                                                                                                                                                                                                        |
|----------------------|------------|--------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Power Manager</b> |            |                    |                |                                                                                                                                                                                                                                    |
| A9                   | nVDD_FAULT | GPIO12             | DO/DIO         | Indication for low supply voltage / GPIO12 / VDD_MON controlled GPO                                                                                                                                                                |
| B6                   | CHG_WAKE   |                    | DI/PWR         | Wake-up signal from companion charger to trigger a start-up and temporary supply voltage for PMIC (VBUS_PROT in case of an inserted supply until charger Buck provides power to V <sub>sys</sub> ).<br>Connect to GND if not used. |
| B7                   | nIRQ       |                    | DO             | IRQ line for host                                                                                                                                                                                                                  |
| B8                   | nSHUTDOWN  |                    | DI             | Active-low input from switch or host to initiate shutdown                                                                                                                                                                          |
| B9                   | SYS_EN     | GPIO8              | DI/DIO         | Hardware enable of power domain SYSTEM/GPIO8                                                                                                                                                                                       |
| B10                  | PWR1_EN    | GPIO10             | DI/DIO         | Hardware enable of power domain POWER1/GPIO10 with high power output / input for power sequencer WAIT ID                                                                                                                           |
| C3                   | VDD_IO2    |                    | PWR            | Alternate supply I/O voltage                                                                                                                                                                                                       |
| C4                   | VDD_IO1    |                    | PWR            | First supply I/O voltage rail                                                                                                                                                                                                      |
| C8                   | GP_FB2     |                    | DO/DI          | PWR_OK status indicator: all supervised regulators are in-range / HW input for watchdog supervision / dual-phase BUCKCORE voltage sense at output capacitor                                                                        |
| C9                   | PWR_EN     | GPIO9              | DI/DIO         | Hardware enable of power domain power / sequencer controlled GPO                                                                                                                                                                   |
| D3                   | GPIO7      |                    | DIO            | Sequencer controlled GPO                                                                                                                                                                                                           |
| D5                   | TP         |                    | DIO            | Test pin: enables power commander boot mode and supply pin for OTP fusing voltage                                                                                                                                                  |
| D9                   | nRESET     |                    | DO             | Active low reset for host                                                                                                                                                                                                          |
| E8                   | GP_FB1     | GPIO13             | DO/DIO         | Status indication for host of a valid wake-up event (EXT_WAKEUP) / indicator for on-going power mode transition (READY) / GPIO13, regulator HW control                                                                             |
| E9                   | GPIO11     |                    | DIO            | GPIO11 with high power output and blinking feature                                                                                                                                                                                 |
| H9                   | GP_FB3     |                    | DO/DO          | Second 32 kHz oscillator output: OUT32_2 / VIB_BREAK control signal for vibration motor driver (LDO8)                                                                                                                              |
| J4                   | nOFF       |                    | DI             | Active-low input from error indication line to initiate fast emergency shutdown                                                                                                                                                    |
| J7                   | nONKEY     |                    | DI             | On/off key with optional long press shutdown                                                                                                                                                                                       |

## System PMIC for Mobile and Automotive Applications

| Pin                             | Pin Name    | Alternate Function | Type (Table 1) | Description                                                                                                                |
|---------------------------------|-------------|--------------------|----------------|----------------------------------------------------------------------------------------------------------------------------|
| <b>4-Wire/2-Wire Interfaces</b> |             |                    |                |                                                                                                                            |
| A4                              | SO          |                    | DO             | 4-wire data output                                                                                                         |
| A5                              | SI          |                    | DIO            | 4-wire data input / 2-wire data                                                                                            |
| A7                              | DATA        | GPIO14             | DIO            | HS-2-WIRE data / GPIO14 (optional reset if long press in parallel with GPI15) with high power output and blinking feature  |
| A8                              | CLK         | GPIO15             | DI             | HS-2-WIRE clock / GPIO15 (optional reset if long press in parallel with GPI14) with high power output and blinking feature |
| B3                              | nCS         |                    | DI             | 4-wire (active low) chip select                                                                                            |
| B4                              | SK          |                    | DI             | 4-wire/2-wire clock                                                                                                        |
| <b>Voltage Regulators</b>       |             |                    |                |                                                                                                                            |
| A3                              | VSYS        |                    | PWR            | Supply voltage for PMIC and input for voltage supervision (decouple with 1.0 $\mu$ F)                                      |
| A6                              | VDDCORE     |                    | AO             | Regulated supply for internal circuitry (2.2 V/2.5 V) (decouple with 2.2 $\mu$ F)                                          |
| C1                              | VLDO11      |                    | AO             | Output voltage from LDO11                                                                                                  |
| D1                              | VLDO10      |                    | AO             | Output voltage from LDO10                                                                                                  |
| D2                              | VDD_LDO11   |                    | PWR            | Supply voltage for LDO11                                                                                                   |
| E1                              | VLDO9       |                    | AO             | Output voltage from LDO9                                                                                                   |
| E2                              | VDD_LDO7_8  |                    | PWR            | Supply voltage for LDO7 and LDO8                                                                                           |
| E3                              | VDD_LDO9_10 |                    | PWR            | Supply voltage for LDO9 and LDO10                                                                                          |
| F1                              | VLDO8       |                    | AO             | Output voltage from LDO8                                                                                                   |
| F2                              | VLDO7       |                    | AO             | Output voltage from LDO7                                                                                                   |
| F3                              | VDD_LDO6    |                    | PWR            | Supply voltage for LDO6                                                                                                    |
| G1                              | VLDO6       |                    | AO             | Output voltage from LDO6                                                                                                   |
| G2                              | VDD_LDO5    |                    | PWR            | Supply voltage for LDO5                                                                                                    |
| G3                              | VDD_LDO3    |                    | PWR            | Supply voltage for LDO3                                                                                                    |
| G4                              | VDD_LDO4    |                    | PWR            | Supply voltage for LDO4                                                                                                    |
| H1                              | VLDO5       |                    | AO             | Output voltage from LDO5                                                                                                   |
| H2                              | VDD_LDO2    |                    | PWR            | Supply voltage for LDO2                                                                                                    |
| H3                              | VDD_LDO1    |                    | PWR            | Supply voltage for LDO1                                                                                                    |
| J1                              | VLDO4       |                    | AO             | Output voltage from LDO4                                                                                                   |
| K1                              | VLDO3       |                    | AO             | Output voltage from LDO3                                                                                                   |
| K2                              | VLDO2       |                    | AO             | Output voltage from LDO2                                                                                                   |
| K3                              | VLDO1       |                    | AO             | Output voltage from LDO1                                                                                                   |

## System PMIC for Mobile and Automotive Applications

| Pin                          | Pin Name      | Alternate Function | Type (Table 1) | Description                                                                                 |
|------------------------------|---------------|--------------------|----------------|---------------------------------------------------------------------------------------------|
| <b>DC/DC Buck Converters</b> |               |                    |                |                                                                                             |
| A1                           | XTAL_OUT      |                    | AIO            | 32 kHz crystal connection (adjust with 10 pF)                                               |
| A2                           | VREF          |                    | AIO            | Filter node for internal reference voltage (decouple with 0.22 $\mu$ F)                     |
| A10                          | OUT_32K       |                    | DO             | 32 kHz oscillator buffer                                                                    |
| B1                           | XTAL_IN       |                    | AIO            | 32 kHz crystal connection (adjust with 10 pF)                                               |
| B2                           | VLNREF        |                    |                | Filter node for LN (low noise) (decouple with 0.22 $\mu$ F)                                 |
| B5                           | VTTR          | CMP1V2             | AO/DO          | Memory bus termination reference voltage (50 % of VDDQ), COMP1V2 controlled GPO             |
| C2                           | IREF          |                    | AO             | Connection for bias setting (configure with high precision 200 k $\Omega$ resistor)         |
| C5                           | ADCIN2        | GPIO1              | AI/DIO         | Connection to GPADC channel 2 with 1.2 V HW comparator IRQ/GPIO1, regulator HW control      |
| C6                           | ADCIN3        | GPIO2              | AI/DIO         | Connection to GPADC channel 3/GPIO2, regulator HW control                                   |
| C7                           | ADCIN1        | GPIO0              | AI/DIO         | Connection to GPADC auto channel 1 with threshold IRQ and resistor measurement option/GPIO0 |
| C10                          | V_CP          |                    | AIO            | Charge pump output bypass (decouple with 10 nF)                                             |
| D4                           | VDDQ          | E_GPI2             | AI/DO          | BUCKPRO target voltage sense port / state of E_GPI2 controlled GPO                          |
| D8                           | PERI_SWS      | GPIO6              | AI/DO          | BUCKPERI sense node from rail switch output/ GPIO6<br>Pulled down when switch is open       |
| D10                          | SWBUCKPRO_B   |                    | AO             | Switching node for BUCKPRO (full-current)                                                   |
| E10                          | SWBUCKPRO_A   |                    | AO             | Switching node for BUCKPRO (half-current)                                                   |
| F8, F9                       | VDD_BUCKPRO   |                    | PWR            | Supply voltage for buck<br>To be connected to VSYS                                          |
| F10                          | SWBUCKCORE2_A |                    | AO             | Switching node for BUCKCORE2 (half-current)                                                 |
| G8, G9                       | VDD_BUCKCORE2 |                    | PWR            | Supply voltage for buck<br>To be connected to VSYS                                          |
| G10                          | SWBUCKCORE2_B |                    | AO             | Switching node for BUCKCORE2 (full-current)                                                 |
| H4                           | VDD_BUCKPERI  |                    | PWR            | Supply voltage for buck<br>To be connected to VSYS                                          |
| H5                           | VDD_BUCKMEM   |                    | PWR            | Supply voltage for buck<br>To be connected to VSYS                                          |

## System PMIC for Mobile and Automotive Applications

| Pin                           | Pin Name      | Alternate Function | Type (Table 1) | Description                                                                                                                                                                             |
|-------------------------------|---------------|--------------------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H6                            | VDD_BUCKIO    |                    | PWR            | Supply voltage for buck<br>To be connected to VSYS                                                                                                                                      |
| H7, H8                        | VDD_BUCKCORE1 |                    | PWR            | Supply voltage for buck<br>To be connected to VSYS                                                                                                                                      |
| H10                           | SWBUCKCORE1_A |                    | AO             | Switching node for BUCKCORE1 (half-current)                                                                                                                                             |
| J2                            | VBUCKPERI     |                    | AI             | Sense node for BUCKPERI                                                                                                                                                                 |
| J3                            | VBUCKMEM      |                    | AI             | Sense node for DC/DC BUCKMEM                                                                                                                                                            |
| J5                            | PERI_SWG      | GPIO5              | AIO/DIO        | NMOS gate driver for buck rail switch/GPIO5                                                                                                                                             |
| J6                            | CORE_SWG      | GPIO3              | AIO/DIO        | NMOS gate driver for buck rail switch/GPIO3                                                                                                                                             |
| J8                            | CORE_SWS      | GPIO4              | AI/DO          | BUCKCORE sense node from rail switch output or output capacitor of dual-phase BUCKCORE/<br>connection of internal switch to the output of LDO1/GPIO4<br>Pulled down when switch is open |
| J10                           | SWBUCKCORE1_B |                    | AO             | Switching node for BUCKCORE1 (full-current)                                                                                                                                             |
| K4                            | VBUCKIO       |                    | AI             | Sense node for BUCKIO                                                                                                                                                                   |
| K5                            | SWBUCKPERI    |                    | AO             | Switching node for BUCKPERI                                                                                                                                                             |
| K6                            | SWBUCKMEM     |                    | AO             | Switching node for BUCKMEM                                                                                                                                                              |
| K7                            | SWBUCKIO      |                    | AO             | Switching node for BUCKIO<br>To be connected to SWBUCKMEM for buck merge                                                                                                                |
| K8                            | VBUCKCORE1    |                    | AI             | Sense node for BUCKCORE1                                                                                                                                                                |
| K9                            | VBUCKCORE2    |                    | AI             | Sense node for BUCKCORE2                                                                                                                                                                |
| K10                           | VBUCKPRO      |                    | AI             | Sense node for BUCKPRO                                                                                                                                                                  |
| <b>Backup Battery Charger</b> |               |                    |                |                                                                                                                                                                                         |
| J9                            | VBBAT         |                    | AIO            | Backup battery connection<br>Coin-cell or super-cap (decouple with 470 nF)                                                                                                              |
| <b>Vss</b>                    |               |                    |                |                                                                                                                                                                                         |
| D6-7, E4, F4                  | GND           |                    | GND            | VSS_LDO, VSS_ADC, VSS_CORE, VSUB                                                                                                                                                        |
| E5-7, F5-7, G5-7              | GND           |                    | GND            | VSS_BUCKCORE1_A, VSS_BUCKCORE1_B, VSS_BUCKCORE2_A, VSS_BUCKCORE2_B, VSS_BUCK_PRO_A, VSS_BUCK_PRO_B, VSS_BUCK_IO, VSS_BUCK_MEM, VSS_BUCK_PERI                                            |

## System PMIC for Mobile and Automotive Applications

### 4 Regulator Overview

Table 3: Regulators

| Regulator | Supplied Pins | Supplied Voltage (V) | Supplied Max. Current (mA)                                     | External Component                         | Notes                                                                                                                                                                                                                                                                                                                                                                              |
|-----------|---------------|----------------------|----------------------------------------------------------------|--------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BUCKCORE1 | VBUCKCORE1    | 0.3 to 1.57          | 1250/<br>2500<br>(full-current mode)<br><a href="#">Note 1</a> | 1.0 $\mu$ H/<br>44 $\mu$ F /<br>88 $\mu$ F | <ul style="list-style-type: none"> <li>GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5, 1.0, 2.0, 4.0] <math>\mu</math>s)</li> <li>10 mV steps</li> <li>&lt; 0.7 V PFM mode only</li> <li>2500 mA in full-current mode (double pass device and current limit)</li> <li>Provides dual-phase buck with up to 5 A if combined with BUCKCORE2</li> </ul> |
| BUCKCORE2 | VBUCKCORE2    | 0.3 to 1.57          | 1250/<br>2500<br>(full-current mode)<br><a href="#">Note 1</a> | 1.0 $\mu$ H/<br>44/88 $\mu$ F              | <ul style="list-style-type: none"> <li>GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] <math>\mu</math>s)</li> <li>10 mV steps</li> <li>&lt; 0.7 V PFM mode only</li> <li>2500 mA in full-current mode (double pass device and current limit)</li> <li>Provides dual-phase Buck if combined with BUCKCORE1</li> </ul>                   |
| BUCKPRO   | VBUCKPRO      | 0.53 to 1.80         | 1250/<br>2500<br>(full-current mode)<br><a href="#">Note 1</a> | 1.0 $\mu$ H/<br>44/88 $\mu$ F              | <ul style="list-style-type: none"> <li>GPIO and host interface-controlled DVC with variable slew rate, (10 mV in [0.5/1.0/2.0/4.0] <math>\mu</math>s)</li> <li>10 mV steps and VTT regulator mode</li> <li>&lt; 0.7 V PFM mode only</li> <li>2500 mA in full-current mode (double pass device and current limit)</li> </ul>                                                        |
| BUCKMEM   | VBUCKMEM      | 0.8 to 3.34          | 1500<br><a href="#">Note 1</a>                                 | 1.0 $\mu$ H/<br>44 $\mu$ F                 | <ul style="list-style-type: none"> <li>GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] <math>\mu</math>s)</li> <li>20 mV steps</li> <li>Can be merged with BUCK_IO towards single buck with up to 3 A output current</li> </ul>                                                                                                         |

## System PMIC for Mobile and Automotive Applications

| Regulator | Supplied Pins | Supplied Voltage (V) | Supplied Max. Current (mA)     | External Component         | Notes                                                                                                                                                                                                                                          |
|-----------|---------------|----------------------|--------------------------------|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BUCKIO    | VBUCKIO       | 0.8 to 3.34          | 1500<br><a href="#">Note 1</a> | 1.0 $\mu$ H/<br>44 $\mu$ F | <ul style="list-style-type: none"> <li>GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] <math>\mu</math>s)</li> <li>20 mV steps, can be merged with BUCK_MEM</li> </ul>                              |
| BUCKPERI  | VBUCKPERI     | 0.8 to 3.34          | 1500<br><a href="#">Note 1</a> | 1.0 $\mu$ H/<br>44 $\mu$ F | <ul style="list-style-type: none"> <li>GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] <math>\mu</math>s)</li> <li>20 mV steps</li> </ul>                                                           |
| LDO1      | VLDO1         | 0.6 to 1.86          | 100                            | 1.0 $\mu$ F                | <ul style="list-style-type: none"> <li>GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] <math>\mu</math>s)</li> <li>20 mV steps</li> <li>Optional voltage tracking of BUCKCORE or BUCKPRO</li> </ul> |
| LDO2      | VLDO2         | 0.6 to 1.86          | 200                            | 2.2 $\mu$ F                | <ul style="list-style-type: none"> <li>GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] <math>\mu</math>s)</li> <li>20 mV steps</li> </ul>                                                           |
| LDO3      | VLDO3         | 0.9 to 3.44          | 200                            | 2.2 $\mu$ F                | <ul style="list-style-type: none"> <li>Bypass mode</li> <li>GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] <math>\mu</math>s)</li> <li>20 mV steps</li> </ul>                                      |
| LDO4      | VLDO4         | 0.9 to 3.44          | 200                            | 2.2 $\mu$ F                | <ul style="list-style-type: none"> <li>Bypass mode</li> <li>GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] <math>\mu</math>s)</li> <li>20 mV steps</li> </ul>                                      |
| LDO5      | VLDO5         | 0.9 to 3.6           | 100                            | 1.0 $\mu$ F                | 50 mV steps                                                                                                                                                                                                                                    |
| LDO6      | VLDO6         | 0.9 to 3.6           | 200                            | 2.2 $\mu$ F                | <ul style="list-style-type: none"> <li>Low noise</li> <li>50 mV steps</li> </ul>                                                                                                                                                               |
| LDO7      | VLDO7         | 0.9 to 3.6           | 200                            | 2.2 $\mu$ F                | <ul style="list-style-type: none"> <li>Bypass mode</li> <li>50 mV steps</li> <li>Common supply with LDO8</li> </ul>                                                                                                                            |

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| Regulator | Supplied Pins        | Supplied Voltage (V)   | Supplied Max. Current (mA) | External Component | Notes                                                                                                                                                                                                      |
|-----------|----------------------|------------------------|----------------------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO8      | VLDO8                | 0.9 to 3.6             | 200                        | 2.2 $\mu$ F        | <ul style="list-style-type: none"> <li>Bypass and switching vibration motor driver mode</li> <li>50 mV steps</li> <li>Common supply with LDO7</li> </ul>                                                   |
| LDO9      | VLDO9                | 0.95 to 3.6            | 200                        | 2.2 $\mu$ F        | <ul style="list-style-type: none"> <li>Low noise</li> <li>50 mV steps</li> <li>OTP trimmed</li> <li>Common supply with LDO10</li> </ul>                                                                    |
| LDO10     | VLDO10               | 0.9 to 3.6             | 300                        | 2.2 $\mu$ F        | <ul style="list-style-type: none"> <li>Low noise LDO</li> <li>50 mV steps</li> <li>Common supply with LDO9</li> </ul>                                                                                      |
| LDO11     | VLDO11               | 0.9 to 3.6             | 300                        | 2.2 $\mu$ F        | <ul style="list-style-type: none"> <li>Bypass mode</li> <li>50 mV steps</li> </ul>                                                                                                                         |
| BACKUP    | VBBAT                | 1.1 to 3.1             | 6                          | 470 nF             | <ul style="list-style-type: none"> <li>100/200 mV steps</li> <li>Configurable charge current between 100 <math>\mu</math>A and 6000 <math>\mu</math>A</li> <li>Reverse current protection (RCP)</li> </ul> |
| LDOCORE   | Internal PMIC supply | 2.5 $\pm$ 2 % accuracy | 4                          | 2.2 $\mu$ F        | <ul style="list-style-type: none"> <li>Internal LDO</li> <li>OTP trimmed</li> </ul>                                                                                                                        |

**Note 1** For short durations to meet peak current requirements  $I_{OUT}$  can be operated at up to 20 % higher than the specified maximum operating condition. The part should not be operated in this mode for extended periods and is not guaranteed for continuous operation.

## System PMIC for Mobile and Automotive Applications

### 5 Electrical Characteristics

#### 5.1 Absolute Maximum Ratings

Table 4 lists the absolute maximum ratings of the device. Exceeding these ratings may cause permanent damage to the device. Device functionality is only guaranteed under the conditions listed in Sections 5.1 and 5.2. Operating the device in conditions exceeding those listed in Table 5 but compliant with the absolute maximum ratings listed in Table 4, for extended periods of time may affect device reliability.

**Table 4: Absolute Maximum Ratings**

| Parameter                                   | Description                                 | Conditions     | Min  | Typ | Max                      | Unit |
|---------------------------------------------|---------------------------------------------|----------------|------|-----|--------------------------|------|
| T <sub>STG</sub>                            | Storage temperature                         |                | -65  |     | +150                     | °C   |
| T <sub>J</sub>                              | Junction temperature                        | Note 2         | -40  |     | +150                     | °C   |
| V <sub>SYS</sub> ,<br>V <sub>CHG_WAKE</sub> | Supply voltage                              |                | -0.3 |     | 6.0                      | V    |
| V <sub>BBAT</sub>                           |                                             |                | -0.3 |     | 3.25                     | V    |
| V <sub>TP</sub>                             |                                             | Note 4         | -0.3 |     | 8.0                      | V    |
| All other pins                              |                                             | Note 3         | -0.3 |     | V <sub>DDREF</sub> + 0.3 | V    |
| V <sub>ESD_HBM</sub>                        | ESD protection - Human Body Model (HBM)     |                | 2000 |     |                          | V    |
| V <sub>ESD_CDM</sub>                        | ESD protection - Charged Device Model (CDM) | Corner pins    | 750  |     |                          | V    |
|                                             |                                             | All other pins | 500  |     |                          |      |

**Note 2** See Section 5.16 and Section 6.17.

**Note 3** Maximum 6.0 V. An internal node V<sub>DDREF</sub> is defined as the higher rail of CHG\_WAKE and V<sub>SYS</sub>.

**Note 4** Voltage on TP pin should be 0 V except during in-circuit programming.

## System PMIC for Mobile and Automotive Applications

### 5.2 Recommended Operating Conditions

All voltages are referenced to VSS unless otherwise stated. Currents flowing into DA9063 are deemed positive; currents flowing out are deemed negative. All parameters are valid over the recommended temperature range and power supply range unless otherwise stated. Please note that the power dissipation must be limited to avoid overheating of DA9063.

**Table 5: Recommended Operating Conditions**

| Parameter                      | Description                                  | Conditions                                                                                     | Min  | Typ   | Max  | Unit |
|--------------------------------|----------------------------------------------|------------------------------------------------------------------------------------------------|------|-------|------|------|
| $T_J$                          | Junction temperature                         |                                                                                                | -40  |       | +125 | °C   |
| $V_{SYS}$ ,<br>$V_{CHG\_WAKE}$ | Supply voltage                               |                                                                                                | 0    |       | 5.5  | V    |
| $V_{BBAT}$                     | Backup supply voltage                        |                                                                                                | 0    |       | 3.15 | V    |
| $V_{DD\_IO1/2}$                | Supply voltage IO                            | Note 1                                                                                         | 1.2  |       | 3.6  | V    |
| $V_{TP}$                       | TP programming supply                        | Note 5                                                                                         | 7.25 | 7.5   | 7.75 | V    |
| $I_{OUT}$                      | BUCKCORE1,<br>BUCKCORE2,<br>BUCKPRO          | Note 2                                                                                         |      |       | 2500 | mA   |
| $I_{OUT}$                      | BUCKMEM,<br>BUCKIO,<br>BUCKPERI              | Note 2                                                                                         |      |       | 1500 | mA   |
| $R_{\theta\_JA}$               | Thermal resistance junction to ambient       | 100 VFBGA package<br>Note 3                                                                    |      | 27.7  |      | °C/W |
|                                |                                              | 100 TFBGA package<br>Note 4                                                                    |      | 17.2  |      | °C/W |
| $R_{\theta\_JB}$               | Thermal resistance junction to Board         | 100 TFBGA package<br>Note 4                                                                    |      | 11.1  |      | °C/W |
| $R_{\theta\_JC}$               | Thermal resistance junction to case          | 100 TFBGA package<br>Note 4                                                                    |      | 13.29 |      | °C/W |
| $P_D$                          | Maximum power dissipation, see Section 5.2.1 | 100 VFBGA<br>Derating factor above<br>$T_A = 70\text{ °C}$ :<br>36.1 mW/°C ( $1/\theta_{JA}$ ) | 2000 |       |      | mW   |
|                                |                                              | 100 TFBGA<br>Derating factor above<br>$T_A = 70\text{ °C}$ :<br>58.1 mW/°C ( $1/\theta_{JA}$ ) | 3770 |       |      | mW   |

**Note 1**  $V_{DDIO1/2}$  must not exceed  $V_{DDREF}$ .

**Note 2** For short durations to meet peak current requirements  $I_{OUT}$  can be operated at up to 20 % higher than the specified maximum operating condition. The part should not be operated in this mode for extended periods and is not guaranteed for continuous operation.

**Note 3** Obtained from package thermal simulations, JEDEC 2S2P four layer board (76.2 mm x 114 mm x 1.6 mm), 70  $\mu$ m (2 oz) copper thickness power planes, 35  $\mu$ m (1 oz) copper thickness signal layer traces, natural convection (still air), see Section 9.1.

## System PMIC for Mobile and Automotive Applications

**Note 4** Obtained from package thermal simulations, JEDEC 2S2P four layer board (101.6 mm x 114.3 mm x 1.6 mm), 70  $\mu\text{m}$  (2 oz) copper thickness power planes, 35  $\mu\text{m}$  (1 oz) copper thickness signal layer traces, natural convection (still air), see Section 9.1.

**Note 5** Voltage on TP pin should be 0 V except during in-circuit programming.

### 5.2.1 Power Derating Curves

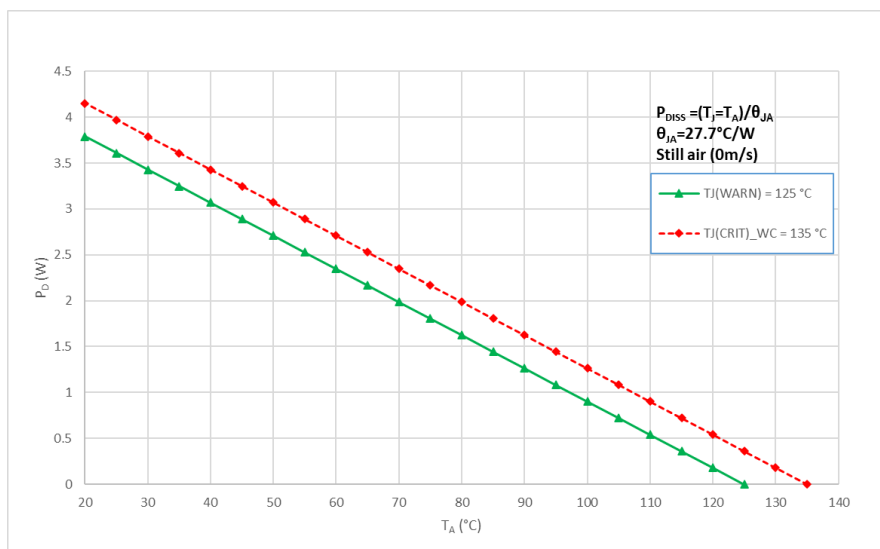


Figure 3: 100 VFBGA Power Derating Curve

Table 6: Typical Temperatures

|                   | $T_A = 70^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ | $T_A = 105^\circ\text{C}$ |
|-------------------|--------------------------|--------------------------|---------------------------|
| $T_{J\_WARN}$     | $P_D = 1.99\text{ W}$    | $P_D = 1.44\text{ W}$    | $P_D = 0.72\text{ W}$     |
| $T_{J\_CRIT\_WC}$ | $P_D = 2.35\text{ W}$    | $P_D = 1.81\text{ W}$    | $P_D = 1.083\text{ W}$    |

## System PMIC for Mobile and Automotive Applications

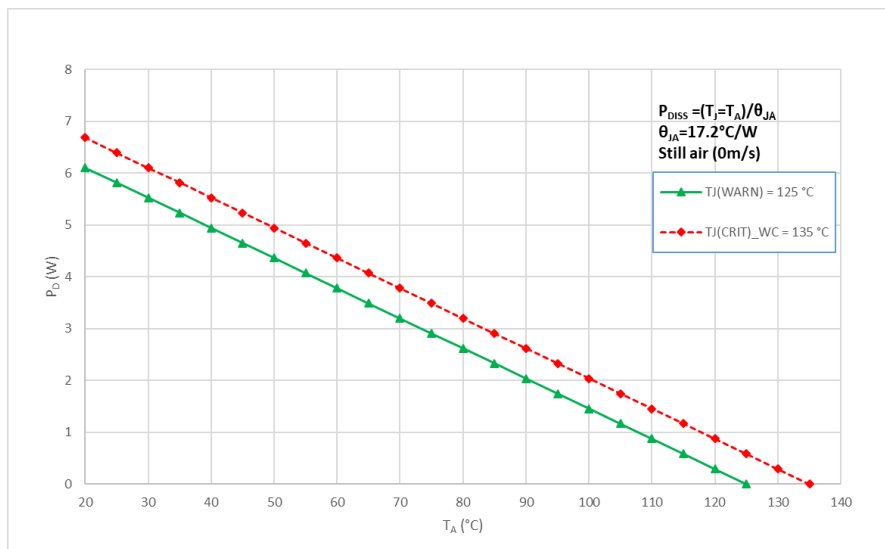


Figure 4:100 TFBGA Power Derating Curve

Table 7: Typical Temperatures

|                   | $T_A = 70^{\circ}\text{C}$ | $T_A = 85^{\circ}\text{C}$ | $T_A = 105^{\circ}\text{C}$ |
|-------------------|----------------------------|----------------------------|-----------------------------|
| $T_{J\_WARN}$     | $P_D = 3.19\text{ W}$      | $P_D = 2.32\text{ W}$      | $P_D = 1.16\text{ W}$       |
| $T_{J\_CRIT\_WC}$ | $P_D = 3.77\text{ W}$      | $P_D = 2.9\text{ W}$       | $P_D = 1.74\text{ W}$       |

## System PMIC for Mobile and Automotive Applications

### 5.3 Typical Current Consumption

Table 8: Typical Current Consumption

| Operating Mode             | Conditions (Note 1)                                                                                                                                    | Backup Device | Battery        | Unit          |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|----------------|---------------|
| NO-POWER mode (POR)        | $2.4\text{ V} > V_{DDREF} > V_{BBAT} > 1.5\text{ V}$                                                                                                   | 0             | 16             | $\mu\text{A}$ |
| DELIVERY mode Note 2       | $V_{BBAT} > V_{DDREF} > 1.5\text{ V}$                                                                                                                  | 0.5           | 0.4<br>Note 3  | $\mu\text{A}$ |
|                            | $V_{DDREF} > V_{BBAT} > 1.5\text{ V}$                                                                                                                  | 0             | 1.5            |               |
| RTC mode Note 2            | $V_{BBAT} > V_{DDREF} > 2.0\text{ V}$                                                                                                                  | 1.4           | 1.06<br>Note 3 | $\mu\text{A}$ |
|                            | $V_{DDREF} > V_{BBAT} > 2.0\text{ V}$                                                                                                                  | 0.05          | 7              |               |
| RESET mode                 | $V_{DDREF} > 2.2\text{ V}$ , supplies off (except LDOCORE), RTC on, pulsed mode:                                                                       |               |                | $\mu\text{A}$ |
|                            | $V_{BBAT} > V_{DDREF}$                                                                                                                                 | 1.6           | 11             |               |
|                            | $V_{BBAT} < V_{DDREF}$                                                                                                                                 | 0.05          | 18             |               |
| LOW-POWER mode             | $V_{SYS} > V_{DD\_FAULT\_LOWER}$ , supplies off (except LDOCORE), all blocks in POWERDOWN mode, RTC on, pulsed mode with limited parametric compliance |               | 18             | $\mu\text{A}$ |
| POWERDOWN mode (Hibernate) | $V_{SYS} > V_{DD\_FAULT\_LOWER}$ , supplies off (except LDOCORE), all blocks in POWERDOWN mode, RTC on                                                 |               | 40             | $\mu\text{A}$ |
| POWERDOWN mode (Standby)   | BUCKCORE, LDOCORE, LDO2, 4, 5 enabled, RTC and GPIO unit on                                                                                            |               | 65<br>Note 4   | $\mu\text{A}$ |
| ACTIVE mode                | All supplies, GPIO, RTC and GPADC on                                                                                                                   |               | 320            | $\mu\text{A}$ |

**Note 1** nONKEY/CHG\_WAKE/ $V_{DDREF}$  detection circuit is enabled in all modes.

**Note 2** See  $V_{BBAT}$  current in RTC or DELIVERY modes [1]

**Note 3** 0  $\mu\text{A}$  if no main battery available.

**Note 4** Regulators are running in SLEEP mode.

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### 5.4 Digital I/O Characteristics

Table 9: Digital I/O Electrical Characteristics,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

| Parameter | Description                                                                                                             | Conditions                                                               | Min                   | Typ | Max                   | Unit |
|-----------|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-----------------------|-----|-----------------------|------|
| $V_{IH}$  | GPIO to GPI15, nOFF, nSHUTDOWN<br>SYS_EN, PWR_EN, PWR1_EN<br>Input High Voltage                                         | VDDCORE mode                                                             | 1.0                   |     | $V_{SYS}$             | V    |
|           |                                                                                                                         | VDD_IO2 mode                                                             | $0.7 \times VDD\_IO2$ |     | $V_{SYS}$             |      |
| $V_{IL}$  | GPIO to GPI15, nOFF, nSHUTDOWN<br>SYS_EN, PWR_EN, PWR1_EN<br>Input Low Voltage                                          | VDDCORE mode                                                             | -0.3                  |     | 0.4                   | V    |
|           |                                                                                                                         | VDD_IO2 mode<br>$VDD\_IO2 \geq 1.5\text{V}$                              | -0.3                  |     | $0.3 \times VDD\_IO2$ |      |
| $V_{IH}$  | nONKEY, CHG_WAKE<br>Input High Voltage                                                                                  |                                                                          | 1.0                   |     | $V_{SYS}$             | V    |
| $V_{IL}$  | nONKEY, CHG_WAKE<br>Input Low Voltage                                                                                   |                                                                          | -0.3                  |     | 0.4                   | V    |
| $V_{IH}$  | CLK, DATA, SK, SI<br>(2-WIRE mode)<br>Input High Voltage                                                                | VDDCORE mode                                                             | 1.0                   |     |                       | V    |
|           |                                                                                                                         | VDD_IO2 mode                                                             | $0.7 \times VDD\_IO2$ |     |                       |      |
| $V_{IL}$  | CLK, DATA, SK, SI<br>(2-WIRE mode)<br>Input Low Voltage                                                                 | VDDCORE mode                                                             |                       |     | 0.4                   | V    |
|           |                                                                                                                         | VDD_IO2 mode<br>$VDD\_IO2 \geq 1.5\text{V}$                              |                       |     | $0.3 \times VDD\_IO2$ |      |
| $V_{IH}$  | SK, nCS, SI<br>(4-WIRE mode)<br>Input High Voltage                                                                      |                                                                          | $0.7 \times VDD\_IOx$ |     |                       | V    |
| $V_{IL}$  | SK, nCS, SI<br>(4-WIRE mode)<br>Input Low Voltage                                                                       |                                                                          |                       |     | $0.3 \times VDD\_IOx$ | V    |
| $V_{OH}$  | GPO0 to GPO15,<br>nVDD_FAULT, SO,<br>nRESET, nIRQ,<br>E_GPI_2, COMP1V2,<br>OUT_32K,<br>OUT_32K_2<br>Output High Voltage | $I_{OUT} = -1\text{ mA}$<br>$VDD\_IO1 \geq 1.5\text{ V}$<br>VDD_IO1 mode | $0.8 \times VDD\_IO1$ |     |                       | V    |
|           |                                                                                                                         | $I_{OUT} = -1\text{ mA}$<br>$VDD\_IO2 \geq 1.5\text{ V}$<br>VDD_IO2 mode | $0.8 \times VDD\_IO2$ |     |                       |      |
| $V_{OH}$  | GPO1, 3 to 6, 10, and<br>12 to 15, DATA, SI (2-<br>WIRE mode) SO,<br>nRESET, nIRQ,<br>GP_FB2<br>Output High Voltage     | Open drain                                                               |                       |     | $V_{DDREF}$           | V    |

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| Parameter | Description                                                                                                                     | Conditions                                     | Min            | Typ | Max  | Unit       |
|-----------|---------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|----------------|-----|------|------------|
| $V_{OL}$  | GPO0 to GPO15, SO, nVDD_FAULT, nRESET (Note 1), nIRQ (Note 1), GP_FB2, E_GPI_2, COMP1V2, OUT_32K, OUT_32K_2, Output Low Voltage | $I_{OUT} = 1 \text{ mA}$                       |                |     | 0.3  | V          |
| $V_{OL}$  | DATA, SI (2-WIRE mode) Output Low Voltage                                                                                       | $I_{OUT} = 3 \text{ mA}$                       |                |     | 0.24 | V          |
| $V_{OL}$  | SI (2-WIRE mode) Output Low Voltage                                                                                             | $I_{OUT} = 8 \text{ mA}$                       |                |     | 0.4  | V          |
| $C_{IN}$  | CLK, DATA, SK, SI Input Capacitance                                                                                             |                                                |                |     | 10   | pF         |
| $t_{rDA}$ | SI (2-WIRE MODE) Data Fall Time                                                                                                 | Fast<br>$C_B < 550 \text{ pF}$                 | $20 + 0.1 C_b$ |     | 120  | ns         |
|           |                                                                                                                                 | HS<br>$10 < C_B < 100 \text{ pF}$              | 10             |     | 40   |            |
|           |                                                                                                                                 | HS<br>$C_B < 400 \text{ pF}$                   | 20             |     | 80   |            |
|           | Sink current capability<br>GPO 10, 11, 14, 15                                                                                   | $V_{GPIO} = 0.4 \text{ V}$<br>Note 2           |                | 11  |      | mA         |
|           | Source current capability<br>GPO 10, 11, 14, 15                                                                                 | $V_{GPIO} = 0.8 \cdot V_{DD\_IO1/2}$<br>Note 2 |                | -4  |      | mA         |
|           | Sink current capability<br>GPO 0 to 9, 12, 13                                                                                   | $V_{GPIO} = 0.3 \text{ V}$                     |                | 1   |      | mA         |
|           | Source current capability<br>GPO 0 to 9, 12, 13                                                                                 | $V_{GPIO} = 0.8 \cdot V_{DD\_IO1/2}$<br>Note 3 |                | -1  |      | mA         |
|           | GPI pull-down resistor                                                                                                          |                                                | 50             | 100 | 250  | k $\Omega$ |
|           | GPO pull-up resistor<br>Note 4                                                                                                  | $V_{DD\_IO1/2} = 1.5 \text{ V}$                | 60             | 180 | 310  | k $\Omega$ |
|           |                                                                                                                                 | $V_{DD\_IO1/2} = 1.8 \text{ V}$                | 45             | 120 | 190  |            |
|           |                                                                                                                                 | $V_{DD\_IO1/2} = 3.3 \text{ V}$                | 20             | 40  | 60   |            |

**Note 1** Electrical characteristics are guaranteed down to  $V_{DDREF} = 2.0 \text{ V}$  ( $V_{POR\_LOWER}$ ). For lower voltages the port continues operating with reduced performance.

**Note 2** At low  $V_{DDREF}$  values and high temperatures, the sink current capability is reduced.

**Note 3** For  $V_{DD\_IO1/2} < 1.5 \text{ V}$  the source current capability is reduced.

**Note 4**  $V(PAD) = 0 \text{ V}$ .

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### 5.5 Watchdog

Table 10: Watchdog,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

| Parameter     | Description           | Conditions                 | Min | Typ | Max  | Unit |
|---------------|-----------------------|----------------------------|-----|-----|------|------|
| $T_{WD\_MIN}$ | Minimum Watchdog time | External 32 kHz oscillator |     |     | 0.11 | s    |
|               |                       | Internal 25 kHz oscillator |     |     | 0.2  | s    |
| $T_{WD\_MAX}$ | Maximum Watchdog time | External 32 kHz oscillator | 2   |     |      | s    |
|               |                       | Internal 25 kHz oscillator | 2.5 |     |      |      |

### 5.6 Power Manager and HS-2-Wire Control Bus

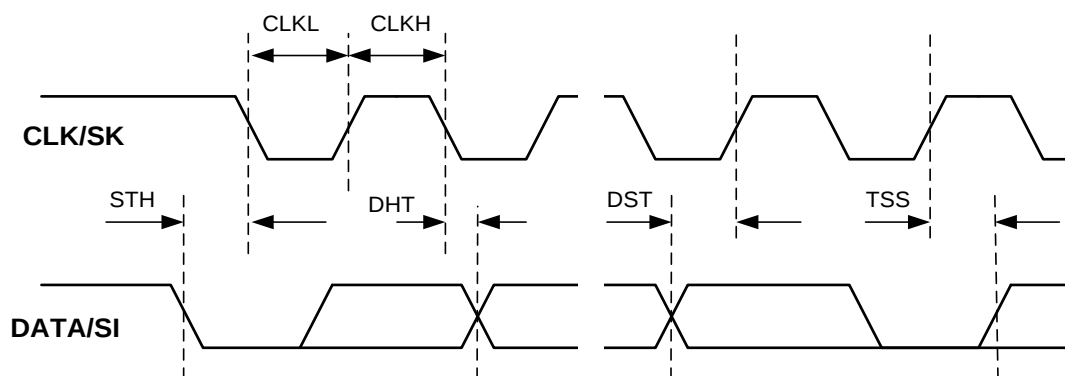


Figure 5: 2-Wire Bus Timing

Table 11: Power Manager and HS-2-Wire Control Bus Electrical Characteristics,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

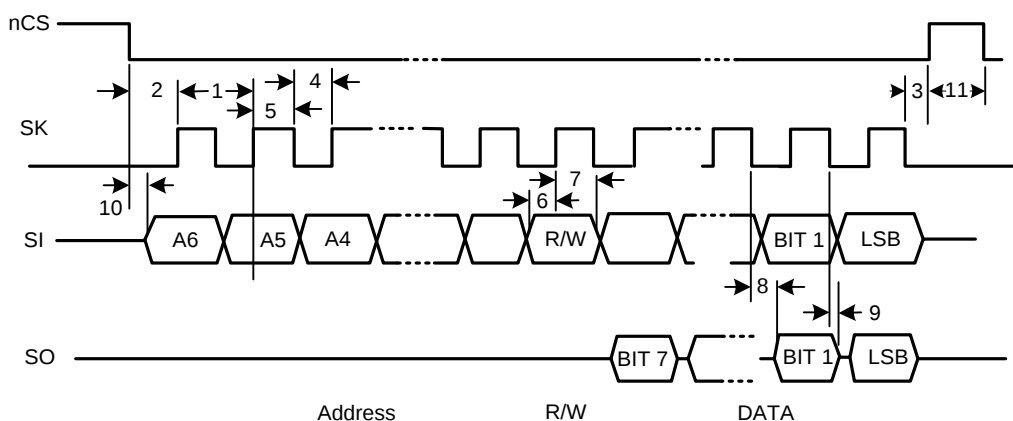
| Parameter                       | Description                   | Conditions                                | Min  | Typ | Max  | Unit          |
|---------------------------------|-------------------------------|-------------------------------------------|------|-----|------|---------------|
|                                 | Bus free time STOP to START   |                                           | 0.5  |     |      | $\mu\text{s}$ |
| $C_B$                           | Bus line capacitive load      |                                           |      |     | 150  | pF            |
| <b>Standard/Fast/Fast+ Mode</b> |                               |                                           |      |     |      |               |
|                                 | CLK clock frequency           | $V_{DD\_IO2} \geq 1.5\text{ V}$<br>Note 1 | 0    |     | 1000 | kHz           |
|                                 | Bus free time STOP to START   |                                           | 0.5  |     |      | $\mu\text{s}$ |
|                                 | Start condition set-up time   |                                           | 0.26 |     |      | $\mu\text{s}$ |
| STH                             | Start condition hold time     |                                           | 0.26 |     |      | $\mu\text{s}$ |
| CLKL                            | CLK low time                  |                                           | 0.5  |     |      | $\mu\text{s}$ |
| CLKH                            | CLK high time                 |                                           | 0.26 |     |      | $\mu\text{s}$ |
|                                 | 2-WIRE CLK and DATA rise time | (input requirement)                       |      |     | 1000 | ns            |

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| Parameter              | Description                         | Conditions                | Min  | Typ | Max  | Unit |
|------------------------|-------------------------------------|---------------------------|------|-----|------|------|
|                        | 2-WIRE CLK and DATA fall time       | (input requirement)       |      |     | 300  | ns   |
| DST                    | Data set-up time                    |                           | 50   |     |      | ns   |
| DHT                    | Data hold-time                      |                           | 0    |     |      | ns   |
|                        | Data valid time                     |                           |      |     | 0.45 | μs   |
|                        | Data valid time acknowledge         |                           |      |     | 0.45 | μs   |
| TSS                    | Stop condition set-up time          |                           | 0.26 |     |      | μs   |
| <b>High Speed Mode</b> |                                     |                           |      |     |      |      |
|                        | CLK clock frequency                 | VDD_IO2 ≥ 1.8 V<br>Note 1 | 0    |     | 3400 | kHz  |
|                        | Start condition set-up time         |                           | 160  |     |      | ns   |
| STH                    | Start condition hold time           |                           | 160  |     |      | ns   |
| CLKL                   | CLK low time                        |                           | 160  |     |      | ns   |
| CLKH                   | CLK high time                       |                           | 60   |     |      | ns   |
|                        | 2-WIRE CLKH and SDAH rise/fall time | Input requirement         |      |     | 160  | ns   |
| DST                    | Data set-up time                    |                           | 10   |     |      | ns   |
| DHT                    | Data hold-time                      |                           | 0    |     |      | ns   |
| TSS                    | Stop condition set-up time          |                           | 160  |     |      | ns   |

**Note 1** Minimum clock frequency is 10 kHz if TWOWIRE\_TO is enabled.

### 5.7 4-Wire Control Bus



**Figure 6: 4-Wire Bus Timing**

**Note 1** The above timing is valid for active-low and high CS.

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**Table 12: 4-Wire Control Bus,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter | Description              | Label in Plot                       | Min             | Typ | Max | Unit |
|-----------|--------------------------|-------------------------------------|-----------------|-----|-----|------|
| $C_B$     | Bus line capacitive load |                                     |                 |     | 100 | pF   |
| $t_c$     | Cycle time               | 1                                   | 70              |     |     | ns   |
| $t_{css}$ | Enable lead time         | 2, from nCS active to first SK edge | 20              |     |     | ns   |
| $t_{scs}$ | Enable lag time          | 3, from last SK edge to nCS idle    | 20              |     |     | ns   |
| $t_{CL}$  | Clock low time           | 4                                   | $0.4 \cdot t_c$ |     |     | ns   |
| $t_{CH}$  | Clock high time          | 5                                   | $0.4 \cdot t_c$ |     |     | ns   |
| $t_{SIS}$ | Data-in set-up time      | 6                                   | 5               |     |     | ns   |
| $t_{SIH}$ | Data-in hold time        | 7                                   | 5               |     |     | ns   |
| $t_{SOV}$ | Data-out valid time      | 8                                   |                 |     | 22  | ns   |
| $t_{SOH}$ | Data-out hold time       | 9                                   | 6               |     |     | ns   |
| $t_{wCS}$ | CS inactive time         | 11                                  | 20              |     |     | ns   |

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### 5.8 LDO Voltage Regulators

#### 5.8.1 LDO1

**Table 13: LDO1,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter       | Description                       | Conditions                                                                                                                                                                     | Min           | Typ                           | Max   | Unit                |
|-----------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-------------------------------|-------|---------------------|
| $V_{DD}$        | Input voltage                     | $V_{DD} = V_{SYS}$                                                                                                                                                             | 2.8           |                               | 5.5   | V                   |
|                 |                                   | If supplied from buck                                                                                                                                                          | 1.5<br>Note 1 |                               |       |                     |
| $V_{LDO}$       | Output voltage                    |                                                                                                                                                                                | 0.6           | Note 2                        | 1.86  | V                   |
| $V_{LDO\_ACC}$  | Output accuracy                   | $V_{DD} = V_{SYS} = 2.8\text{ V to } 5.5\text{ V}$<br>$I_{OUT} = 100\text{ mA}$<br>Including static line/load regulation                                                       | -3            |                               | +3    | %                   |
| $C_{OUT}$       | Stabilization capacitor           | Including voltage and temperature coefficient at configured VLDO1                                                                                                              | -55 %         | 1.0                           | +35 % | $\mu\text{F}$       |
| $R_{COUT\_ESR}$ | Output capacitor ESR              | $f > 1\text{ MHz}$<br>Including wiring parasitics                                                                                                                              | 0             |                               | 300   | $\text{m}\Omega$    |
| $I_{OUT\_MAX}$  | Output current                    | $V_{DD} = V_{SYS} = 2.8\text{ V to } 5.5\text{ V}$                                                                                                                             | 100           |                               |       | mA                  |
| $I_{SHORT}$     | Short circuit current             |                                                                                                                                                                                |               | 200                           |       | mA                  |
| $I_{SLEEP}$     | Maximum forced sleep mode current | $V_{DD} \geq 1.8\text{ V}$                                                                                                                                                     | 10            |                               |       | mA                  |
| $V_{DROPOUT}$   | Dropout voltage                   | $V_{DD} = V_{SYS} > 2.8\text{ V}$<br>$I_{OUT} = 100\text{ mA}$<br>( $V_{DD} = 1.5\text{ V}$ , $I_{OUT} = I_{MAX}/3$ )                                                          |               | 100                           | 150   | mV                  |
| $V_{S\_LINE}$   | Static line regulation            | $V_{DD} = V_{SYS} = 3.0\text{ V to } 5.5\text{ V}$<br>$I_{OUT} = 100\text{ mA}$                                                                                                |               | 1                             | 5     | mV                  |
| $V_{S\_LOAD}$   | Static load regulation            | $I_{OUT} = 1\text{ mA to } 100\text{ mA}$                                                                                                                                      |               | 5                             | 10    | mV                  |
| $V_{TR\_LINE}$  | Line transient response           | $V_{DD} = V_{SYS} = 3.0\text{ V to } 3.6\text{ V}$<br>$I_{OUT} = 100\text{ mA}$<br>$t_r = t_f = 10\text{ }\mu\text{s}$                                                         |               | 5                             | 10    | mV                  |
| $V_{TR\_LOAD}$  | Load transient response           | $V_{DD} = 3.6\text{ V}$<br>$I_{OUT} = 1\text{ mA to } 100\text{ mA}$<br>$t_r = t_f = 1\text{ }\mu\text{s}$                                                                     |               | 30                            | 50    | mV                  |
| PSRR<br>Note 3  | PSRR                              | $f = 10\text{ Hz to } 10\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 3.6\text{ V}$ , $I_{OUT} = I_{MAX}/2$<br>$V_{DD} - V_{LDO} \geq 0.6\text{ V}$                 | 50            | 60                            |       | dB                  |
| N               | Output noise                      | $V_{DD} = V_{SYS} = 3.6\text{ V}$ ,<br>$V_{LDO} = 1.8\text{ V}$<br>$I_{OUT} = 5\text{ mA to } I_{MAX}$<br>$f = 10\text{ Hz to } 100\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$ |               | 70                            |       | $\mu\text{V}_{rms}$ |
| $I_{Q\_ON}$     | Quiescent current in ON mode      | Note 4                                                                                                                                                                         |               | $9 + 0.7\%$<br>% of $I_{OUT}$ |       | $\mu\text{A}$       |

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| Parameter            | Description                         | Conditions                                | Min | Typ                            | Max | Unit |
|----------------------|-------------------------------------|-------------------------------------------|-----|--------------------------------|-----|------|
| I <sub>Q_SLEEP</sub> | Quiescent current forced sleep mode |                                           |     | 1.5 + 1.4% of I <sub>OUT</sub> |     | μA   |
| I <sub>Q_OFF</sub>   | Quiescent current OFF mode          |                                           |     | 1                              |     | μA   |
| t <sub>ON</sub>      | Turn-on time                        | 10 % to 90 %                              |     |                                | 300 | μs   |
|                      |                                     | SLEEP mode                                |     |                                | 390 |      |
| t <sub>OFF</sub>     | Turn off time                       | 90 % to 10%<br>Pull-down resistor enabled |     |                                | 1   | ms   |
| R <sub>OFF</sub>     | Pull-down resistance in OFF mode    | Can be disabled via LDO1_PD_DIS           |     | 55                             |     | Ω    |

**Note 1** Max output current is 30 % when the input voltage is 1.5 V.

**Note 2** Programmable in 20 mV voltage steps.

**Note 3** Measured at point of load.

**Note 4** Internal regulator current flowing to ground.

### 5.8.2 LDO2

**Table 14: LDO2, T<sub>J</sub> = -40 °C to +125 °C**

| Parameter                        | Description                       | Conditions                                                                                                                                   | Min           | Typ    | Max   | Unit |
|----------------------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|---------------|--------|-------|------|
| V <sub>DD</sub>                  | Input voltage                     | V <sub>DD</sub> = V <sub>SYS</sub>                                                                                                           | 2.8           |        | 5.5   | V    |
|                                  |                                   | If supplied from buck                                                                                                                        | 1.5<br>Note 1 |        |       |      |
| V <sub>LDO</sub>                 | Output voltage                    |                                                                                                                                              | 0.6           | Note 2 | 1.86  | V    |
| V <sub>LDO_ACC</sub>             | Output accuracy                   | V <sub>DD</sub> = V <sub>SYS</sub> = 2.8 V to 5.5 V<br>I <sub>OUT</sub> = 200 mA<br>Including static line/load regulation                    | -3            |        | +3    | %    |
| C <sub>OUT</sub>                 | Stabilization capacitor           | Including voltage and temperature coefficient at configured VLDO2                                                                            | -55 %         | 2.2    | +35 % | μF   |
| R <sub>COU<sub>T</sub>_ESR</sub> | Output capacitor ESR              | f > 1 MHz<br>including wiring parasitics                                                                                                     | 0             |        | 300   | mΩ   |
| I <sub>OUT_MAX</sub>             | Output current                    | V <sub>DD</sub> = V <sub>SYS</sub> = 2.8 V to 5.5 V                                                                                          | 200           |        |       | mA   |
| I <sub>SHORT</sub>               | Short circuit current             |                                                                                                                                              |               | 400    |       | mA   |
| I <sub>SLEEP</sub>               | Maximum forced sleep mode current | V <sub>DD</sub> ≥ 1.8 V                                                                                                                      | 20            |        |       | mA   |
| V <sub>DROPOUT</sub>             | Dropout voltage                   | V <sub>DD</sub> = V <sub>SYS</sub> > 2.8 V<br>I <sub>OUT</sub> = 200 mA<br>(V <sub>DD</sub> = 1.5 V, I <sub>OUT</sub> = I <sub>MAX</sub> /3) |               | 100    | 150   | mV   |
| V <sub>S_LINE</sub>              | Static line regulation            | V <sub>DD</sub> = V <sub>SYS</sub> = 3.0 V to 5.5 V<br>I <sub>OUT</sub> = 200 mA                                                             |               | 1      | 5     | mV   |
| V <sub>S_LOAD</sub>              | Static load regulation            | I <sub>OUT</sub> = 1 mA to 200 mA                                                                                                            |               | 5      | 10    | mV   |

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| Parameter            | Description                         | Conditions                                                                                                                                           | Min | Typ                                  | Max | Unit      |
|----------------------|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------------------------------|-----|-----------|
| V <sub>TR_LINE</sub> | Line transient response             | V <sub>DD</sub> = V <sub>SYS</sub> = 3.0 V to 3.6 V<br>I <sub>OUT</sub> = 100 mA<br>tr = tf = 10 μs                                                  |     | 5                                    | 10  | mV        |
| V <sub>TR_LOAD</sub> | Load transient response             | V <sub>DD</sub> = 3.6 V<br>I <sub>OUT</sub> = 1 mA to 200 mA<br>tr = tf = 1 μs                                                                       |     | 30                                   | 50  | mV        |
| PSRR<br>Note 3       | PSRR                                | f = 10 Hz to 10 kHz, 25 °C<br>V <sub>DD</sub> = 3.6 V, I <sub>OUT</sub> = I <sub>MAX</sub> /2<br>V <sub>DD</sub> - V <sub>LDO</sub> ≥ 0.6 V          | 50  | 60                                   |     | dB        |
| N                    | Output noise                        | V <sub>DD</sub> = V <sub>SYS</sub> = 3.6 V<br>V <sub>LDO</sub> = 1.8 V<br>I <sub>OUT</sub> = 5 mA to I <sub>MAX</sub><br>f = 10 Hz to 100 kHz, 25 °C |     | 70                                   |     | μV<br>rms |
| I <sub>Q_ON</sub>    | Quiescent current in ON mode        | Note 4                                                                                                                                               |     | 9 +<br>0.4% of<br>I <sub>OUT</sub>   |     | μA        |
| I <sub>Q_SLEEP</sub> | Quiescent current forced sleep mode |                                                                                                                                                      |     | 1.5 +<br>0.9% of<br>I <sub>OUT</sub> |     | μA        |
| I <sub>Q_OFF</sub>   | Quiescent current OFF mode          |                                                                                                                                                      |     | 1                                    |     | μA        |
| t <sub>ON</sub>      | Turn-on time                        | 10 to 90%                                                                                                                                            |     |                                      | 150 | μs        |
|                      |                                     | SLEEP mode                                                                                                                                           |     |                                      | 195 |           |
| t <sub>OFF</sub>     | Turn off time                       | 90 to 10%, pull-down resistor enabled                                                                                                                |     |                                      | 1   | ms        |
| R <sub>OFF</sub>     | Pull-down resistance in OFF mode    | Can be disabled via LDO2_PD_DIS                                                                                                                      |     | 55                                   |     | Ω         |

**Note 1** Max output current is 30% when the input voltage is 1.5 V.

**Note 2** Programmable in 20 mV voltage steps.

**Note 3** Measured at point of load.

**Note 4** Internal regulator current flowing to ground.

### 5.8.3 LDO3

**Table 15: LDO3, T<sub>J</sub> = -40 °C to +125 °C**

| Parameter            | Description               | Conditions                                                                                                               | Min             | Typ    | Max  | Unit |
|----------------------|---------------------------|--------------------------------------------------------------------------------------------------------------------------|-----------------|--------|------|------|
| V <sub>DD</sub>      | Input voltage             | V <sub>DD</sub> = V <sub>SYS</sub>                                                                                       | 2.8             |        | 5.5  | V    |
|                      |                           | If supplied from buck                                                                                                    | (1.5)<br>Note 1 |        |      |      |
| V <sub>LDO</sub>     | Output voltage            |                                                                                                                          | 0.9             | Note 2 | 3.44 | V    |
| V <sub>LDO_ACC</sub> | Output accuracy<br>Note 3 | V <sub>DD</sub> = V <sub>SYS</sub> = 2.8V to 5.5 V<br>I <sub>OUT</sub> = 200 mA<br>Including static line/load regulation | -3              |        | +3   | %    |

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| Parameter                      | Description                         | Conditions                                                                                                                                            | Min  | Typ                                  | Max  | Unit              |
|--------------------------------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|------|--------------------------------------|------|-------------------|
| C <sub>OUT</sub>               | Stabilization capacitor             | Including voltage and temperature coefficient at configured VLDO3                                                                                     | -55% | 2.2                                  | +35% | μF                |
| R <sub>COUT_ESR</sub>          | Output capacitor ESR                | f > 1 MHz including wiring parasitics                                                                                                                 | 0    |                                      | 300  | mΩ                |
| I <sub>OUT_MAX</sub>           | Output current                      | V <sub>DD</sub> = V <sub>SYS</sub> = 2.8 V to 5.5 V                                                                                                   | 200  |                                      |      | mA                |
| I <sub>SHORT</sub>             | Short circuit current               |                                                                                                                                                       |      | 400                                  |      | mA                |
| I <sub>SLEEP</sub>             | Maximum forced sleep mode current   | V <sub>DD</sub> ≥ 1.8 V                                                                                                                               | 20   |                                      |      | mA                |
| V <sub>DROPOUT</sub>           | Dropout voltage                     | V <sub>DD</sub> = V <sub>SYS</sub> > 2.8 V<br>I <sub>OUT</sub> = 100 mA<br>(V <sub>DD</sub> = 1.5 V, I <sub>OUT</sub> = I <sub>MAX</sub> /3)          |      | 100                                  | 150  | mV                |
| V <sub>S_LINE</sub>            | Static line regulation              | V <sub>DD</sub> = V <sub>SYS</sub> = 3.0 V to 5.5 V<br>I <sub>OUT</sub> = 200 mA                                                                      |      | 1                                    | 5    | mV                |
| V <sub>S_LOAD</sub>            | Static load regulation              | I <sub>OUT</sub> = 1 mA to 200 mA                                                                                                                     |      | 5                                    | 10   | mV                |
| V <sub>TR_LINE</sub>           | Line transient response             | V <sub>DD</sub> = V <sub>SYS</sub> = 3.0 V to 3.6 V<br>I <sub>OUT</sub> = 100 mA<br>tr = tf = 10 μs                                                   |      | 5                                    | 10   | mV                |
| V <sub>TR_LOAD</sub>           | Load transient response             | V <sub>DD</sub> = 3.6 V<br>I <sub>OUT</sub> = 1 mA to 200 mA<br>tr = tf = 1 μs                                                                        |      | 30                                   | 50   | mV                |
| PSRR<br><a href="#">Note 4</a> | PSRR                                | f = 10 Hz to 10 kHz, 25 °C<br>V <sub>DD</sub> = 3.6 V, I <sub>OUT</sub> = I <sub>MAX</sub> /2<br>V <sub>DD</sub> - V <sub>LDO</sub> ≥ 0.6 V           | 50   | 60                                   |      | dB                |
| N                              | Output noise                        | V <sub>DD</sub> = V <sub>SYS</sub> = 3.6 V,<br>V <sub>LDO</sub> = 2.8 V<br>I <sub>OUT</sub> = 5 mA to I <sub>MAX</sub><br>f = 10 Hz to 100 kHz, 25 °C |      | 70                                   |      | μV <sub>rms</sub> |
| I <sub>Q_ON</sub>              | Quiescent current in ON mode        | <a href="#">Note 5</a>                                                                                                                                |      | 9 +<br>0.45%<br>of I <sub>OUT</sub>  |      | μA                |
| I <sub>Q_SLEEP</sub>           | Quiescent current forced sleep mode |                                                                                                                                                       |      | 1.5 +<br>1.0% of<br>I <sub>OUT</sub> |      | μA                |
| I <sub>Q_OFF</sub>             | Quiescent current OFF mode          |                                                                                                                                                       |      | 1                                    |      | μA                |
| t <sub>ON</sub>                | Turn-on time                        | 10 to 90%                                                                                                                                             |      |                                      | 300  | μs                |
|                                |                                     | SLEEP mode                                                                                                                                            |      |                                      | 390  |                   |
| t <sub>OFF</sub>               | Turn off time                       | 90 % to 10 %<br>Pull-down resistor enabled                                                                                                            |      |                                      | 1    | ms                |
| R <sub>OFF</sub>               | Pull-down resistance in OFF mode    | Can be disabled via<br>LDO3_PD_DIS                                                                                                                    |      | 55                                   |      | Ω                 |
| <b>Bypass Mode</b>             |                                     |                                                                                                                                                       |      |                                      |      |                   |
| R <sub>ON</sub>                | Bypass on-resistance                | V <sub>DD</sub> > 2.2 V                                                                                                                               |      | 0.5                                  | 0.7  | Ω                 |

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| Parameter       | Description                      | Conditions               | Min | Typ | Max | Unit          |
|-----------------|----------------------------------|--------------------------|-----|-----|-----|---------------|
|                 |                                  | $V_{DD} > 1.8 \text{ V}$ |     |     | 1.0 |               |
| $I_{LIM}$       | Current limit in Bypass mode     |                          |     | 380 |     | mA            |
| $I_{Q\_BYPASS}$ | Quiescent current in Bypass mode |                          |     | 50  | 100 | $\mu\text{A}$ |

**Note 1** Max output current is 30% when the input voltage is 1.5 V.

**Note 2** Programmable in 20 mV voltage steps.

**Note 3** Accuracy values not applicable if bypass mode has been configured.

**Note 4** Measured at point of load.

**Note 5** Internal regulator current flowing to ground.

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### 5.8.4 LDO4

**Table 16: LDO4,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter       | Description                         | Conditions                                                                                                                                                                   | Min           | Typ                           | Max   | Unit                |
|-----------------|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-------------------------------|-------|---------------------|
| $V_{DD}$        | Input voltage                       | $V_{DD} = V_{SYS}$                                                                                                                                                           | 2.8           |                               | 5.5   | V                   |
|                 |                                     | If supplied from buck                                                                                                                                                        | 1.5<br>Note 1 |                               |       |                     |
| $V_{LDO}$       | Output voltage                      |                                                                                                                                                                              | 0.9           | Note 2                        | 3.44  | V                   |
| $V_{LDO\_ACC}$  | Output accuracy<br>Note 3           | $V_{DD} = V_{SYS} = 2.8\text{ V to }5.5\text{ V}$<br>$I_{OUT} = 200\text{ mA}$<br>Including static line/load regulation                                                      | -3            |                               | +3    | %                   |
| $C_{OUT}$       | Stabilization capacitor             | Including voltage and temperature coefficient at configured VLDO4                                                                                                            | -55 %         | 2.2                           | +35 % | $\mu\text{F}$       |
| $R_{COUT\_ESR}$ | Output capacitor ESR                | $f > 1\text{ MHz}$<br>Including wiring parasitics                                                                                                                            | 0             |                               | 300   | m $\Omega$          |
| $I_{OUT\_MAX}$  | Output current                      | $V_{DD} = V_{SYS} = 2.8\text{ V to }5.5\text{ V}$                                                                                                                            | 200           |                               |       | mA                  |
| $I_{SHORT}$     | Short circuit current               |                                                                                                                                                                              |               | 400                           |       | mA                  |
| $I_{SLEEP}$     | Maximum forced sleep mode current   | $V_{DD} \geq 1.8\text{ V}$                                                                                                                                                   | 30            |                               |       | mA                  |
| $V_{DROPOUT}$   | Dropout voltage                     | $V_{DD} = V_{SYS} > 2.8\text{ V}$<br>$I_{OUT} = 200\text{ mA}$<br>( $V_{DD} = 1.5\text{ V}$ , $I_{OUT} = I_{MAX}/3$ )                                                        |               | 100                           | 150   | mV                  |
| $V_{S\_LINE}$   | Static line regulation              | $V_{DD} = V_{SYS} = 3.0\text{ V to }5.5\text{ V}$<br>$I_{OUT} = 200\text{ mA}$                                                                                               |               | 1                             | 5     | mV                  |
| $V_{S\_LOAD}$   | Static load regulation              | $I_{OUT} = 1\text{ mA to }200\text{ mA}$                                                                                                                                     |               | 5                             | 10    | mV                  |
| $V_{TR\_LINE}$  | Line transient response             | $V_{DD} = V_{SYS} = 3.0\text{ V to }3.6\text{ V}$<br>$I_{OUT} = 100\text{ mA}$<br>$t_r = t_f = 10\text{ }\mu\text{s}$                                                        |               | 5                             | 10    | mV                  |
| $V_{TR\_LOAD}$  | Load transient response             | $V_{DD} = 3.6\text{ V}$<br>$I_{OUT} = 1\text{ mA to }200\text{ mA}$<br>$t_r = t_f = 1\text{ }\mu\text{s}$                                                                    |               | 30                            | 50    | mV                  |
| PSRR<br>Note 4  | PSRR                                | $f = 10\text{ Hz to }10\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 3.6\text{ V}$ , $I_{OUT} = I_{MAX}/2$<br>$V_{DD} - V_{LDO} \geq 0.6\text{ V}$                | 50            | 60                            |       | dB                  |
| N               | Output noise                        | $V_{DD} = V_{SYS} = 3.6\text{ V}$ ,<br>$V_{LDO} = 2.8\text{ V}$<br>$I_{OUT} = 5\text{ mA to }I_{MAX}$<br>$f = 10\text{ Hz to }100\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$ |               | 70                            |       | $\mu\text{V}_{rms}$ |
| $I_{Q\_ON}$     | Quiescent current in ON mode        | Note 5                                                                                                                                                                       |               | 9 +<br>0.4%<br>of $I_{OUT}$   |       | $\mu\text{A}$       |
| $I_{Q\_SLEEP}$  | Quiescent current forced sleep mode |                                                                                                                                                                              |               | 1.5 +<br>1.0%<br>of $I_{OUT}$ |       | $\mu\text{A}$       |

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| Parameter             | Description                      | Conditions                                | Min | Typ | Max | Unit |
|-----------------------|----------------------------------|-------------------------------------------|-----|-----|-----|------|
| I <sub>Q_OFF</sub>    | Quiescent current OFF mode       |                                           |     | 1   |     | μA   |
| t <sub>ON</sub>       | Turn-on time                     | 10 % to 90%                               |     |     | 300 | μs   |
|                       |                                  | SLEEP mode                                |     |     | 390 |      |
| t <sub>OFF</sub>      | Turn off time                    | 90 % to 10%<br>Pull-down resistor enabled |     |     | 1   | ms   |
| R <sub>OFF</sub>      | Pull-down resistance in OFF mode | Can be disabled via LDO4_PD_DIS           |     | 55  |     | Ω    |
| <b>Bypass mode</b>    |                                  |                                           |     |     |     |      |
| R <sub>ON</sub>       | Bypass on-resistance             | V <sub>DD</sub> > 2.2 V                   |     | 0.5 | 0.7 | Ω    |
|                       |                                  | V <sub>DD</sub> > 1.8 V                   |     |     | 1.0 |      |
| I <sub>LIM</sub>      | Current limit in Bypass mode     |                                           |     | 175 |     | mA   |
| I <sub>Q_BYPASS</sub> | Quiescent current in Bypass mode |                                           |     | 50  | 100 | μA   |

**Note 1** Max output current is 30% when the input voltage is 1.5 V.

**Note 2** Programmable in 20 mV voltage steps.

**Note 3** Accuracy values not applicable if bypass mode has been configured.

**Note 4** Measured at point of load.

**Note 5** Internal regulator current flowing to ground.

### 5.8.5 LDO5

**Table 17: LDO5, T<sub>J</sub> = -40 °C to +125 °C**

| Parameter             | Description                       | Conditions                                                                                                                | Min           | Typ    | Max   | Unit |
|-----------------------|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------|---------------|--------|-------|------|
| V <sub>DD</sub>       | Input voltage                     | V <sub>DD</sub> = V <sub>SYS</sub>                                                                                        | 2.8           |        | 5.5   | V    |
|                       |                                   | If supplied from buck                                                                                                     | 1.5<br>Note 1 |        |       |      |
| V <sub>LDO</sub>      | Output voltage                    |                                                                                                                           | 0.9           | Note 2 | 3.6   | V    |
| V <sub>LDO_ACC</sub>  | Output accuracy                   | V <sub>DD</sub> = V <sub>SYS</sub> = 2.8 V to 5.5 V<br>I <sub>OUT</sub> = 100 mA<br>Including static line/load regulation | -3            |        | +3    | %    |
| C <sub>OUT</sub>      | Stabilization capacitor           | Including voltage and temperature coefficient at configured VLDO5                                                         | -55 %         | 1.0    | +35 % | μF   |
| R <sub>COU_TESR</sub> | Output capacitor ESR              | f > 1 MHz<br>Including wiring parasitics                                                                                  | 0             |        | 300   | mΩ   |
| I <sub>OUT_MAX</sub>  | Output current                    | V <sub>DD</sub> = V <sub>SYS</sub> = 2.8 V to 5.5 V                                                                       | 100           |        |       | mA   |
| I <sub>SHORT</sub>    | Short circuit current             |                                                                                                                           |               | 200    |       | mA   |
| I <sub>SLEEP</sub>    | Maximum forced sleep mode current | V <sub>DD</sub> ≥ 1.8 V                                                                                                   | 20            |        |       | mA   |

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| Parameter            | Description                         | Conditions                                                                                                                                            | Min | Typ                                   | Max | Unit              |
|----------------------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------------------------------------|-----|-------------------|
| V <sub>DROPOUT</sub> | Dropout voltage                     | V <sub>DD</sub> = V <sub>SYS</sub> > 2.8 V<br>I <sub>OUT</sub> = 100 mA<br>(V <sub>DD</sub> = 1.5 V, I <sub>OUT</sub> = I <sub>MAX</sub> /3)          |     | 100                                   | 150 | mV                |
| V <sub>S_LINE</sub>  | Static line regulation              | V <sub>DD</sub> = V <sub>SYS</sub> = 3.0 V to 5.5 V<br>I <sub>OUT</sub> = 100 mA                                                                      |     | 1                                     | 5   | mV                |
| V <sub>S_LOAD</sub>  | Static load regulation              | I <sub>OUT</sub> = 1 mA to 100 mA                                                                                                                     |     | 5                                     | 10  | mV                |
| V <sub>TR_LINE</sub> | Line transient response             | V <sub>DD</sub> = V <sub>SYS</sub> = 3.0 V to 3.6 V<br>I <sub>OUT</sub> = 100 mA<br>tr = tf = 10 μs                                                   |     | 5                                     | 10  | mV                |
| V <sub>TR_LOAD</sub> | Load transient response             | V <sub>DD</sub> = 3.6 V<br>I <sub>OUT</sub> = 1 mA to 100 mA<br>tr = tf = 1 μs                                                                        |     | 30                                    | 50  | mV                |
| PSRR<br>Note 3       | PSRR                                | f = 10 Hz to 10 kHz, 25 °C<br>V <sub>DD</sub> = 3.6 V, I <sub>OUT</sub> = I <sub>MAX</sub> /2<br>V <sub>DD</sub> - V <sub>LDO</sub> ≥ 0.6 V           | 50  | 60                                    |     | dB                |
| N                    | Output noise                        | V <sub>DD</sub> = V <sub>SYS</sub> = 3.6 V,<br>V <sub>LDO</sub> = 2.8 V<br>I <sub>OUT</sub> = 5 mA to I <sub>MAX</sub><br>f = 10 Hz to 100 kHz, 25 °C |     | 70                                    |     | μV <sub>rms</sub> |
| I <sub>Q_ON</sub>    | Quiescent current in ON mode        | Note 4                                                                                                                                                |     | 9 +<br>0.9 %<br>of I <sub>OUT</sub>   |     | μA                |
| I <sub>Q_SLEEP</sub> | Quiescent current forced sleep mode |                                                                                                                                                       |     | 1.5 +<br>1.6 %<br>of I <sub>OUT</sub> |     | μA                |
| I <sub>Q_OFF</sub>   | Quiescent current OFF mode          |                                                                                                                                                       |     | 1                                     |     | μA                |
| t <sub>ON</sub>      | Turn-on time                        | 10 % to 90 %                                                                                                                                          |     |                                       | 350 | μs                |
|                      |                                     | SLEEP mode                                                                                                                                            |     |                                       | 450 |                   |
| t <sub>OFF</sub>     | Turn off time                       | 90 % to 10 %<br>Pull-down resistor enabled                                                                                                            |     |                                       | 1   | ms                |
| R <sub>OFF</sub>     | Pull-down resistance in OFF mode    | Can be disabled via<br>LDO5_PD_DIS                                                                                                                    |     | 55                                    |     | Ω                 |

**Note 1** Max output current is 30% when the input voltage is 1.5 V.

**Note 2** Programmable in 50 mV voltage steps.

**Note 3** Measured at point of load.

**Note 4** Internal regulator current flowing to ground.

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### 5.8.6 LDO6

**Table 18: LDO6,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter                        | Description                       | Conditions                                                                                                                                                                       | Min                           | Typ                    | Max  | Unit                |
|----------------------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|------------------------|------|---------------------|
| $V_{DD}$                         | Input voltage                     | $V_{DD} = V_{SYS}$                                                                                                                                                               | 2.8                           |                        | 5.5  | V                   |
|                                  |                                   | If supplied from buck                                                                                                                                                            | 1.5<br><a href="#">Note 1</a> |                        |      |                     |
| $V_{LDO}$                        | Output voltage                    |                                                                                                                                                                                  | 0.9                           | <a href="#">Note 2</a> | 3.6  | V                   |
| $V_{LDO\_ACC}$                   | Output accuracy                   | $V_{DD} = V_{SYS} = 2.8\text{ V}$ o $5.5\text{ V}$<br>$I_{OUT} = 200\text{ mA}$<br>Including static line/load regulation                                                         | -3                            |                        | +3   | %                   |
| $C_{OUT}$                        | Stabilization capacitor           | Including voltage and temperature coefficient at configured VLDO6                                                                                                                | -55%                          | 2.2                    | +35% | $\mu\text{F}$       |
| $R_{COUT\_ESR}$                  | Output capacitor ESR              | $f > 1\text{ MHz}$<br>Including wiring parasitics                                                                                                                                | 0                             |                        | 300  | m $\Omega$          |
| $I_{OUT\_MAX}$                   | Output current                    | $V_{DD} = V_{SYS} = 2.8\text{ V}$ to $5.5\text{ V}$                                                                                                                              | 200                           |                        |      | mA                  |
| $I_{SHORT}$                      | Short circuit current             |                                                                                                                                                                                  |                               | 400                    |      | mA                  |
| $I_{SLEEP}$                      | Maximum forced sleep mode current | $V_{DD} \geq 1.8\text{ V}$                                                                                                                                                       | 30                            |                        |      | mA                  |
| $V_{DROPOUT}$                    | Dropout voltage                   | $V_{DD} = V_{SYS} > 2.8\text{ V}$<br>$I_{OUT} = 200\text{ mA}$<br>( $V_{DD} = 1.5\text{ V}$ , $I_{OUT} = I_{MAX}/3$ )                                                            |                               | 100                    | 150  | mV                  |
| $V_{S\_LINE}$                    | Static line regulation            | $V_{DD} = V_{SYS} = 3.0\text{ V}$ to $5.5\text{ V}$<br>$I_{OUT} = 200\text{ mA}$                                                                                                 |                               | 1                      | 5    | mV                  |
| $V_{S\_LOAD}$                    | Static load regulation            | $I_{OUT} = 1\text{ mA}$ to $200\text{ mA}$                                                                                                                                       |                               | 5                      | 10   | mV                  |
| $V_{TR\_LINE}$                   | Line transient response           | $V_{DD} = V_{SYS} = 3.0\text{ V}$ to $3.6\text{ V}$<br>$I_{OUT} = 100\text{ mA}$<br>$t_r = t_f = 10\text{ }\mu\text{s}$                                                          |                               | 5                      | 10   | mV                  |
| $V_{TR\_LOAD}$                   | Load transient response           | $V_{DD} = 3.6\text{ V}$<br>$I_{OUT} = 1\text{ mA}$ to $200\text{ mA}$<br>$t_r = t_f = 1\text{ }\mu\text{s}$                                                                      |                               | 30                     | 50   | mV                  |
| $PSRR$<br><a href="#">Note 3</a> | PSRR                              | $V_{DD} = 3.6\text{ V}$ ,<br>$I_{OUT} = I_{MAX}/2$<br>$V_{DD} - V_{LDO} \geq 0.6\text{ V}$ , $25\text{ }^{\circ}\text{C}$                                                        |                               |                        |      | dB                  |
|                                  |                                   | $f = 10\text{ Hz}$ to $1\text{ kHz}$ ,                                                                                                                                           | 70                            | 80                     |      |                     |
|                                  |                                   | $f = 1\text{ kHz}$ to $10\text{ kHz}$                                                                                                                                            | 60                            | 70                     |      |                     |
|                                  |                                   | $f = 10\text{ kHz}$ to $100\text{ kHz}$                                                                                                                                          | 40                            | 50                     |      |                     |
| N                                | Output noise                      | $V_{DD} = V_{SYS} = 3.6\text{ V}$ ,<br>$V_{LDO} = 2.8\text{ V}$<br>$I_{OUT} = 5\text{ mA}$ to $I_{MAX}$<br>$f = 10\text{ Hz}$ to $100\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$ |                               | 35                     |      | $\mu\text{V}_{rms}$ |

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| Parameter            | Description                         | Conditions                                 | Min | Typ                             | Max | Unit |
|----------------------|-------------------------------------|--------------------------------------------|-----|---------------------------------|-----|------|
| I <sub>Q_ON</sub>    | Quiescent current in ON mode        | Note 4                                     |     | 9+0.45<br>% of I <sub>OUT</sub> |     | μA   |
| I <sub>Q_SLEEP</sub> | Quiescent current forced sleep mode |                                            |     | 2+1.0<br>% of I <sub>OUT</sub>  |     | μA   |
| I <sub>Q_OFF</sub>   | Quiescent current OFF mode          |                                            |     | 1                               |     | μA   |
| t <sub>ON</sub>      | Turn-on time                        | 10 % to 90 %                               |     |                                 | 200 | μs   |
|                      |                                     | SLEEP mode                                 |     |                                 | 260 |      |
| t <sub>OFF</sub>     | Turn off time                       | 90 % to 10 %<br>Pull-down resistor enabled |     |                                 | 1   | ms   |
| R <sub>OFF</sub>     | Pull-down resistance in OFF mode    | Can be disabled via LDO6_PD_DIS            |     | 55                              |     | Ω    |

**Note 1** Max output current is 30% when the input voltage is 1.5 V.

**Note 2** Programmable in 50 mV voltage steps.

**Note 3** Measured at point of load.

**Note 4** Internal regulator current flowing to ground.

### 5.8.7 LDO7

Table 19: LDO7, T<sub>J</sub> = -40 °C to 125 °C

| Parameter             | Description                       | Conditions                                                                                                                                   | Min           | Typ    | Max   | Unit |
|-----------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|---------------|--------|-------|------|
| V <sub>DD</sub>       | Input voltage                     | V <sub>DD</sub> = V <sub>SYS</sub>                                                                                                           | 2.8           |        | 5.5   | V    |
|                       |                                   | If supplied from buck                                                                                                                        | 1.5<br>Note 1 |        |       |      |
| V <sub>LDO</sub>      | Output voltage                    |                                                                                                                                              | 0.9           | Note 2 | 3.6   | V    |
| V <sub>LDO_ACC</sub>  | Output accuracy<br>Note 3         | V <sub>DD</sub> = V <sub>SYS</sub> = 2.8 V to 5.5 V<br>I <sub>OUT</sub> = 200 mA<br>Including static line/load regulation                    | -3            |        | +3    | %    |
| C <sub>OUT</sub>      | Stabilization capacitor           | Including voltage and temperature coefficient at configured VLDO7                                                                            | -55 %         | 2.2    | +35 % | μF   |
| R <sub>COUT_ESR</sub> | ESR of capacitor                  | f > 1 MHz<br>Including track impedance                                                                                                       | 0             |        | 300   | mΩ   |
| I <sub>OUT_MAX</sub>  | Maximum output current            | V <sub>DD</sub> = V <sub>SYS</sub> = 2.8 V to 5.5 V                                                                                          | 200           |        |       | mA   |
| I <sub>SHORT</sub>    | Short circuit current             |                                                                                                                                              |               | 400    |       | mA   |
| I <sub>SLEEP</sub>    | Maximum forced sleep mode current | V <sub>DD</sub> ≥ 1.8 V                                                                                                                      | 30            |        |       | mA   |
| V <sub>DROPOUT</sub>  | Dropout voltage                   | V <sub>DD</sub> = V <sub>SYS</sub> > 2.8 V<br>I <sub>OUT</sub> = 200 mA<br>(V <sub>DD</sub> = 1.5 V, I <sub>OUT</sub> = I <sub>MAX</sub> /3) |               | 100    | 150   | mV   |

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| Parameter             | Description                         | Conditions                                                                                                                                            | Min | Typ                                 | Max | Unit              |
|-----------------------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------------------------|-----|-------------------|
| V <sub>S_LINE</sub>   | Static line regulation              | V <sub>DD</sub> = V <sub>SYS</sub> = 3.0V to 5.5 V<br>I <sub>OUT</sub> = 200 mA                                                                       |     | 1                                   | 5   | mV                |
| V <sub>S_LOAD</sub>   | Static load regulation              | I <sub>OUT</sub> = 1 mA to 200 mA                                                                                                                     |     | 5                                   | 10  | mV                |
| V <sub>TR_LINE</sub>  | Line transient response             | V <sub>DD</sub> = V <sub>SYS</sub> = 3.0 V to 3.6 V<br>I <sub>OUT</sub> = 100 mA<br>tr = tf = 10 μs                                                   |     | 5                                   | 10  | mV                |
| V <sub>TR_LOAD</sub>  | Load transient response             | V <sub>DD</sub> = 3.6 V<br>I <sub>OUT</sub> = 1 mA to 200 mA<br>tr = tf = 1 μs                                                                        |     | 30                                  | 50  | mV                |
| PSRR<br>Note 4        | PSRR                                | f = 10 Hz to 10 kHz, 25 °C<br>V <sub>DD</sub> = 3.6 V, I <sub>OUT</sub> = I <sub>MAX</sub> /2<br>V <sub>DD</sub> - V <sub>LDO</sub> ≥ 0.6 V           | 50  | 60                                  |     | dB                |
| N                     | Output noise                        | V <sub>DD</sub> = V <sub>SYS</sub> = 3.6 V,<br>V <sub>LDO</sub> = 2.8 V<br>I <sub>OUT</sub> = 5 mA to I <sub>MAX</sub><br>f = 10 Hz to 100 kHz, 25 °C |     | 70                                  |     | μV <sub>rms</sub> |
| I <sub>Q_ON</sub>     | Quiescent current in ON mode        | Note 5                                                                                                                                                |     | 9+0.4<br>% of<br>I <sub>OUT</sub>   |     | μA                |
| I <sub>Q_SLEEP</sub>  | Quiescent current forced sleep mode |                                                                                                                                                       |     | 1.5+1.0<br>% of<br>I <sub>OUT</sub> |     | μA                |
| I <sub>Q_OFF</sub>    | Quiescent current OFF mode          |                                                                                                                                                       |     | 1                                   |     | μA                |
| t <sub>ON</sub>       | Turn-on time                        | 10 % to 90 %                                                                                                                                          |     |                                     | 300 | μs                |
|                       |                                     | SLEEP mode                                                                                                                                            |     |                                     | 390 |                   |
| t <sub>OFF</sub>      | Turn off time                       | 90 % to 10 %<br>Pull-down resistor enabled                                                                                                            |     |                                     | 1   | ms                |
| R <sub>OFF</sub>      | Pull-down resistance in OFF mode    | Can be disabled via<br>LDO7_PD_DIS                                                                                                                    |     | 55                                  |     | Ω                 |
| <b>Bypass mode</b>    |                                     |                                                                                                                                                       |     |                                     |     |                   |
| R <sub>ON</sub>       | Bypass on-resistance                | V <sub>DD</sub> > 2.2 V                                                                                                                               |     | 0.5                                 | 0.7 | Ω                 |
|                       |                                     | V <sub>DD</sub> > 1.8 V                                                                                                                               |     |                                     | 1.0 |                   |
| I <sub>LIM</sub>      | Current limit in Bypass mode        |                                                                                                                                                       |     | 280                                 |     | mA                |
| I <sub>Q_BYPASS</sub> | Quiescent current                   |                                                                                                                                                       |     | 50                                  | 100 | μA                |

**Note 1** Max output current is 30% when the input voltage is 1.5 V.

**Note 2** Programmable in 50 mV voltage steps.

**Note 3** Accuracy values not applicable if bypass mode has been configured.

**Note 4** Measured at point of load.

**Note 5** Internal regulator current flowing to ground.

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### 5.8.8 LDO8

**Table 20: LDO8,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter       | Description                         | Conditions                                                                                                                                                                   | Min           | Typ                      | Max   | Unit                |
|-----------------|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|--------------------------|-------|---------------------|
| $V_{DD}$        | Input voltage                       | $V_{DD} = V_{SYS}$                                                                                                                                                           | 2.8           |                          | 5.5   | V                   |
|                 |                                     | If supplied from buck                                                                                                                                                        | 1.5<br>Note 1 |                          |       |                     |
| $V_{LDO}$       | Output voltage                      |                                                                                                                                                                              | 0.9           | Note 2                   | 3.6   | V                   |
| $V_{LDO\_ACC}$  | Output accuracy<br>Note 3           | $V_{DD} = V_{SYS} = 2.8\text{ V to }5.5\text{ V}$<br>$I_{OUT} = 200\text{ mA}$<br>Including static line/load regulation                                                      | -3            |                          | +3    | %                   |
| $C_{OUT}$       | Stabilization capacitor             | Including voltage and temperature coefficient at configured VLDO8                                                                                                            | -55 %         | 2.2                      | +35 % | $\mu\text{F}$       |
| $R_{COUT\_ESR}$ | ESR of capacitor                    | $f > 1\text{ MHz}$<br>Including track impedance                                                                                                                              | 0             |                          | 300   | m $\Omega$          |
| $I_{OUT\_MAX}$  | Maximum output current              | $V_{DD} = V_{SYS} = 2.8\text{ V to }5.5\text{ V}$                                                                                                                            | 200           |                          |       | mA                  |
| $I_{SHORT}$     | Short circuit current               |                                                                                                                                                                              |               | 400                      |       | mA                  |
| $I_{SLEEP}$     | Maximum forced sleep mode current   | $V_{DD} \geq 1.8\text{ V}$                                                                                                                                                   | 30            |                          |       | mA                  |
| $V_{DROPOUT}$   | Dropout voltage                     | $V_{DD} = V_{SYS} > 2.8\text{ V}$<br>$I_{OUT} = 200\text{ mA}$<br>( $V_{DD} = 1.5\text{ V}$ , $I_{OUT} = I_{MAX}/3$ )                                                        |               | 100                      | 150   | mV                  |
| $V_{S\_LINE}$   | Static line regulation              | $V_{DD} = V_{SYS} = 3.0\text{ V to }5.5\text{ V}$<br>$I_{OUT} = 200\text{ mA}$                                                                                               |               | 1                        | 5     | mV                  |
| $V_{S\_LOAD}$   | Static load regulation              | $I_{OUT} = 1\text{ mA to }200\text{ mA}$                                                                                                                                     |               | 5                        | 10    | mV                  |
| $V_{TR\_LINE}$  | Line transient response             | $V_{DD} = V_{SYS} = 3.0\text{ V to }3.6\text{ V}$<br>$I_{OUT} = 100\text{ mA}$<br>$t_r = t_f = 10\text{ }\mu\text{s}$                                                        |               | 5                        | 10    | mV                  |
| $V_{TR\_LOAD}$  | Load transient response             | $V_{DD} = 3.6\text{ V}$<br>$I_{OUT} = 1\text{ mA to }200\text{ mA}$<br>$t_r = t_f = 1\text{ }\mu\text{s}$                                                                    |               | 30                       | 50    | mV                  |
| PSRR<br>Note 4  | PSRR                                | $f = 10\text{ Hz to }10\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 3.6\text{ V}$ , $I_{OUT} = I_{MAX}/2$<br>$V_{DD} - V_{LDO} \geq 0.6\text{ V}$                | 50            | 60                       |       | dB                  |
| N               | Output noise                        | $V_{DD} = V_{SYS} = 3.6\text{ V}$ ,<br>$V_{LDO} = 2.8\text{ V}$<br>$I_{OUT} = 5\text{ mA to }I_{MAX}$<br>$f = 10\text{ Hz to }100\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$ |               | 70                       |       | $\mu\text{V}_{rms}$ |
| $I_{Q\_ON}$     | Quiescent current in ON mode        | Note 5                                                                                                                                                                       |               | 9 + 0.4 % of $I_{OUT}$   |       | $\mu\text{A}$       |
| $I_{Q\_SLEEP}$  | Quiescent current forced sleep mode |                                                                                                                                                                              |               | 1.5 + 1.0 % of $I_{OUT}$ |       | $\mu\text{A}$       |

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| Parameter                          | Description                      | Conditions                                 | Min | Typ | Max   | Unit |
|------------------------------------|----------------------------------|--------------------------------------------|-----|-----|-------|------|
| I <sub>Q_OFF</sub>                 | Quiescent current OFF mode       |                                            |     | 1   |       | μA   |
| t <sub>ON</sub>                    | Turn-on time                     | 10 % to 90 %                               |     |     | 300   | μs   |
|                                    |                                  | SLEEP mode                                 |     |     | 390   |      |
| t <sub>OFF</sub>                   | Turn off time                    | 90 % to 10 %<br>Pull-down resistor enabled |     |     | 1     | ms   |
| R <sub>OFF</sub>                   | Pull-down resistance in OFF mode | Can be disabled via LDO8_PD_DIS            |     | 55  |       | Ω    |
| <b>Vibration Motor Driver Mode</b> |                                  |                                            |     |     |       |      |
| VIB_SET                            | Output voltage (average)         | 6-bit resolution                           | 0   |     | 3     | V    |
| I <sub>MAX</sub>                   | Maximum output current           |                                            |     |     | 300   | mA   |
| I <sub>SHORT</sub>                 | Short circuit current            |                                            |     | 400 |       | mA   |
| R <sub>LOAD</sub>                  | Load resistance                  |                                            | 8   | 10  | 10000 | Ω    |
| Z <sub>LOAD</sub>                  | Load impedance                   |                                            |     | 200 |       | μH   |
| R <sub>PU</sub>                    | Pull-up resistor                 |                                            |     | 0.5 |       | Ω    |
| R <sub>PD</sub>                    | Pull-down resistor               |                                            |     | 5   |       | Ω    |
| <b>Bypass Mode</b>                 |                                  |                                            |     |     |       |      |
| R <sub>ON</sub>                    | Bypass on-resistance             | V <sub>DD</sub> > 2.2 V                    |     | 0.5 | 0.7   |      |
|                                    |                                  | V <sub>DD</sub> > 1.8 V                    |     |     | 1.0   | Ω    |
| I <sub>LIM</sub>                   | Current limit in Bypass mode     |                                            |     | 400 |       | mA   |
| I <sub>Q_BYPASS</sub>              | Quiescent current in Bypass mode |                                            |     | 50  | 100   | μA   |

**Note 1** Max output current is 30% when the input voltage is 1.5 V.

**Note 2** Programmable in 50 mV voltage steps.

**Note 3** Accuracy values not applicable if bypass mode has been configured.

**Note 4** Measured at point of load.

**Note 5** Internal regulator current flowing to ground.

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### 5.8.9 LDO9

**Table 21: LDO9,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter       | Description                         | Conditions                                                                                                                                                                     | Min           | Typ                 | Max   | Unit                |
|-----------------|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------------|-------|---------------------|
| $V_{DD}$        | Input voltage                       | $V_{DD} = V_{SYS}$                                                                                                                                                             | 2.8           |                     | 5.5   | V                   |
|                 |                                     | If supplied from buck                                                                                                                                                          | 1.5<br>Note 1 |                     |       |                     |
| $V_{LDO}$       | Output voltage                      |                                                                                                                                                                                | 0.95          | Note 2              | 3.6   | V                   |
| $V_{LDO\_ACC}$  | Output accuracy<br>Note 3           | $V_{DD} = V_{SYS} = 2.8\text{ V to } 5.5\text{ V}$<br>$I_{OUT} = 200\text{ mA}$<br>Including static line/load regulation                                                       | -3            |                     | +3    | %                   |
| $C_{OUT}$       | Stabilization capacitor             | Including voltage and temperature coefficient at configured VLDO9                                                                                                              | -55 %         | 2.2                 | +35 % | $\mu\text{F}$       |
| $R_{COUT\_ESR}$ | ESR of capacitor                    | $f > 1\text{ MHz}$                                                                                                                                                             | 0             |                     | 300   | m $\Omega$          |
| $I_{OUT\_MAX}$  | Maximum output current              | $V_{DD} = V_{SYS} = 2.8\text{ V to } 5.5\text{ V}$                                                                                                                             | 200           |                     |       | mA                  |
| $I_{SHORT}$     | Short circuit current               |                                                                                                                                                                                |               | 400                 |       | mA                  |
| $I_{SLEEP}$     | Maximum forced sleep mode current   | $V_{DD} \geq 1.8\text{ V}$                                                                                                                                                     | 30            |                     |       | mA                  |
| $V_{DROPOUT}$   | Dropout voltage                     | $V_{DD} = V_{SYS} > 2.8\text{ V}$<br>$I_{OUT} = 200\text{ mA}$<br>( $V_{DD} = 1.5\text{ V}$ , $I_{OUT} = I_{MAX}/3$ )                                                          |               | 100                 | 150   | mV                  |
| $V_{S\_LINE}$   | Static line regulation              | $V_{DD} = V_{SYS} = 3.0\text{ V to } 5.5\text{ V}$<br>$I_{OUT} = 200\text{ mA}$                                                                                                |               | 1                   | 5     | mV                  |
| $V_{S\_LOAD}$   | Static load regulation              | $I_{OUT} = 1\text{ mA to } 200\text{ mA}$                                                                                                                                      |               | 5                   | 10    | mV                  |
| $V_{TR\_LINE}$  | Line transient response             | $V_{DD} = V_{SYS} = 3.0\text{ V to } 3.6\text{ V}$<br>$I_{OUT} = 100\text{ mA}$<br>$t_r = t_f = 10\text{ }\mu\text{s}$                                                         |               | 5                   | 10    | mV                  |
| $V_{TR\_LOAD}$  | Load transient response             | $V_{DD} = 3.6\text{ V}$<br>$I_{OUT} = 1\text{ mA to } 200\text{ mA}$<br>$t_r = t_f = 1\text{ }\mu\text{s}$                                                                     |               | 30                  | 50    | mV                  |
| PSRR<br>Note 4  | PSRR                                | $f = 10\text{ Hz to } 10\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 3.6\text{ V}$ , $I_{OUT} = I_{MAX}/2$<br>$V_{DD} - V_{LDO} \geq 0.6\text{ V}$                 | 60            | 70                  |       | dB                  |
| N               | Output noise                        | $V_{DD} = V_{SYS} = 3.6\text{ V}$ ,<br>$V_{LDO} = 2.8\text{ V}$<br>$I_{OUT} = 5\text{ mA to } I_{MAX}$<br>$f = 10\text{ Hz to } 100\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$ |               | 35                  |       | $\mu\text{V}_{rms}$ |
| $I_{Q\_ON}$     | Quiescent current in ON mode        | Note 5                                                                                                                                                                         |               | 9+0.4% of $I_{OUT}$ |       | $\mu\text{A}$       |
| $I_{Q\_SLEEP}$  | Quiescent current forced sleep mode |                                                                                                                                                                                |               | 2+1.0% of $I_{OUT}$ |       | $\mu\text{A}$       |

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| Parameter          | Description                      | Conditions                                 | Min | Typ | Max        | Unit |
|--------------------|----------------------------------|--------------------------------------------|-----|-----|------------|------|
| I <sub>Q_OFF</sub> | Quiescent current OFF mode       |                                            |     | 1   |            | μA   |
| t <sub>ON</sub>    | Turn-on time                     | 10 % to 90 %<br>SLEEP mode                 |     |     | 200<br>260 | μs   |
| t <sub>OFF</sub>   | Turn off time                    | 90 % to 10 %<br>Pull-down resistor enabled |     |     | 1          | ms   |
| R <sub>OFF</sub>   | Pull-down resistance in OFF mode | Can be disabled via LDO9_PD_DIS            |     | 55  |            | Ω    |

**Note 1** Max output current is 30 % when the input voltage is 1.5 V.

**Note 2** Programmable in 50 mV voltage steps.

**Note 3** At trimmed output voltage.

**Note 4** Measured at point of load.

**Note 5** Internal regulator current flowing to ground.

### 5.8.10 LDO10

**Table 22: LDO10, T<sub>J</sub> = -40 °C to 125 °C**

| Parameter                        | Description                | Conditions                                                                                                                                   | Min           | Typ    | Max  | Unit |
|----------------------------------|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|---------------|--------|------|------|
| V <sub>DD</sub>                  | Input voltage              | V <sub>DD</sub> = V <sub>SYS</sub>                                                                                                           | 2.8           |        | 5.5  | V    |
|                                  |                            | If supplied from buck                                                                                                                        | 1.5<br>Note 1 |        |      |      |
| V <sub>LDO</sub>                 | Output voltage             |                                                                                                                                              | 0.9           | Note 2 | 3.6  | V    |
| V <sub>LDO_ACC</sub>             | Output accuracy            | V <sub>DD</sub> = V <sub>SYS</sub> = 2.8 to 5.5 V<br>I <sub>OUT</sub> = 300 mA<br>Including static line/load regulation                      | -3            |        | +3   | %    |
| C <sub>OUT</sub>                 | Stabilization capacitor    | Including voltage and temperature coefficient configured VLDO10                                                                              | -55%          | 2.2    | +35% | μF   |
| R <sub>COU<sub>T</sub>_ESR</sub> | Output capacitor ESR       | f > 1 MHz<br>Including wiring parasitics                                                                                                     | 0             |        | 300  | mΩ   |
| I <sub>OUT_MAX</sub>             | Output current             | V <sub>DD</sub> = V <sub>SYS</sub> = 2.8 V to 5.5 V                                                                                          | 300           |        |      | mA   |
| I <sub>SHORT</sub>               | Short circuit current      |                                                                                                                                              |               | 600    |      | mA   |
| I <sub>SLEEP</sub>               | Maximum sleep mode current | V <sub>DD</sub> ≥ 1.8 V                                                                                                                      | 30            |        |      | mA   |
| V <sub>DROPOUT</sub>             | Dropout voltage            | V <sub>DD</sub> = V <sub>SYS</sub> > 2.8 V<br>I <sub>OUT</sub> = 300 mA<br>(V <sub>DD</sub> = 1.5 V, I <sub>OUT</sub> = I <sub>MAX</sub> /3) |               | 100    | 150  | mV   |
| V <sub>S_LINE</sub>              | Static line regulation     | V <sub>DD</sub> = V <sub>SYS</sub> = 3.0 V to 5.5 V<br>I <sub>OUT</sub> = 300 mA                                                             |               | 2      | 10   | mV   |
| V <sub>S_LOAD</sub>              | Static load regulation     | I <sub>OUT</sub> = 1 mA to 300 mA                                                                                                            |               | 5      | 20   | mV   |

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| Parameter            | Description                         | Conditions                                                                                                                                            | Min | Typ                                  | Max | Unit              |
|----------------------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------------------------------|-----|-------------------|
| V <sub>TR_LINE</sub> | Line transient response             | V <sub>DD</sub> = V <sub>SYS</sub> = 3.0 V to 3.6 V<br>I <sub>OUT</sub> = 300 mA<br>tr = tf = 10 μs                                                   |     | 5                                    | 10  | mV                |
| V <sub>TR_LOAD</sub> | Load transient response             | V <sub>DD</sub> = 3.6 V<br>I <sub>OUT</sub> = 1 mA to 300 mA<br>tr = tf = 1 μs                                                                        |     | 30                                   | 50  | mV                |
| PSRR<br>Note 3       | PSRR                                | V <sub>DD</sub> = 3.6 V<br>I <sub>OUT</sub> = I <sub>MAX</sub> /2<br>V <sub>DD</sub> - V <sub>LDO</sub> ≥ 0.6 V, 25 °C                                |     |                                      |     | dB                |
|                      |                                     | f = 10 Hz to 1 kHz,                                                                                                                                   | 70  | 80                                   |     |                   |
|                      |                                     | f = 1 kHz to 10 kHz                                                                                                                                   | 60  | 70                                   |     |                   |
|                      |                                     | f = 10 kHz to 100 kHz                                                                                                                                 | 40  | 50                                   |     |                   |
| N                    | Output noise                        | V <sub>DD</sub> = V <sub>SYS</sub> = 3.6 V,<br>V <sub>LDO</sub> = 2.8 V<br>I <sub>OUT</sub> = 5 mA to I <sub>MAX</sub><br>f = 10 Hz to 100 kHz, 25 °C |     | 35                                   |     | μV <sub>rms</sub> |
| I <sub>Q_ON</sub>    | Quiescent current in ON mode        | Note 4                                                                                                                                                |     | 9 +<br>0.34 %<br>of I <sub>OUT</sub> |     | μA                |
| I <sub>Q_SLEEP</sub> | Quiescent current forced sleep mode |                                                                                                                                                       |     | 2 +<br>0.7 %<br>of I <sub>OUT</sub>  |     | μA                |
| I <sub>Q_OFF</sub>   | Quiescent current OFF mode          |                                                                                                                                                       |     | 1                                    |     | μA                |
| t <sub>ON</sub>      | Turn-on time                        | 10 % to 90 %                                                                                                                                          |     |                                      | 200 | μs                |
|                      |                                     | SLEEP mode                                                                                                                                            |     |                                      | 300 |                   |
| t <sub>OFF</sub>     | Turn off time                       | 90 % to 10 %<br>Pull-down resistor enabled                                                                                                            |     |                                      | 1   | ms                |
| R <sub>OFF</sub>     | Pull-down resistance in OFF mode    | Can be disabled via<br>LDO10_PD_DIS                                                                                                                   |     | 55                                   |     | Ω                 |

**Note 1** Max output current is 30 % when the input voltage is 1.5 V.

**Note 2** Programmable in 50 mV voltage steps.

**Note 3** Measured at point of load.

**Note 4** Internal regulator current flowing to ground.

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### 5.8.11 LDO11

**Table 23: LDO11,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter                      | Description                               | Conditions                                                                                                                                                                     | Min                           | Typ                           | Max   | Unit                |
|--------------------------------|-------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|-------------------------------|-------|---------------------|
| $V_{DD}$                       | Input voltage                             | $V_{DD} = V_{SYS}$                                                                                                                                                             | 2.8                           |                               | 5.5   | V                   |
|                                |                                           | If supplied from buck                                                                                                                                                          | 1.5<br><a href="#">Note 1</a> |                               |       |                     |
| $V_{LDO}$                      | Output voltage                            |                                                                                                                                                                                | 0.9                           | <a href="#">Note 2</a>        | 3.6   | V                   |
| $V_{LDO\_ACC}$                 | Output accuracy<br><a href="#">Note 3</a> | $V_{DD} = V_{SYS} = 2.8\text{ V to } 5.5\text{ V}$<br>$I_{OUT} = 200\text{ mA}$<br>Including static line/load regulation                                                       | -3                            |                               | +3    | %                   |
| $C_{OUT}$                      | Stabilization capacitor                   | Including voltage and temperature coefficient at configured VLDO11                                                                                                             | -55 %                         | 2.2                           | +35 % | $\mu\text{F}$       |
| $R_{COUT\_ESR}$                | ESR of capacitor                          | $f > 1\text{ MHz}$<br>Including track impedance                                                                                                                                | 0                             |                               | 300   | m $\Omega$          |
| $I_{OUT\_MAX}$                 | Maximum output current                    | $V_{DD} = V_{SYS} = 2.8\text{ V to } 5.5\text{ V}$                                                                                                                             | 300                           |                               |       | mA                  |
| $I_{SHORT}$                    | Short circuit current                     |                                                                                                                                                                                |                               | 600                           |       | mA                  |
| $I_{SLEEP}$                    | Maximum sleep mode current                | $V_{DD} \geq 1.8\text{ V}$                                                                                                                                                     | 30                            |                               |       | mA                  |
| $V_{DROPOUT}$                  | Dropout voltage                           | $V_{DD} = V_{SYS} > 2.8\text{ V}$<br>$I_{OUT} = 300\text{ mA}$<br>( $V_{DD} = 1.5\text{ V}$ , $I_{OUT} = I_{MAX}/3$ )                                                          |                               | 100                           | 150   | mV                  |
| $V_{S\_LINE}$                  | Static line regulation                    | $V_{DD} = V_{SYS} = 2.8\text{ V to } 5.5\text{ V}$<br>$V_{LDO} = 1.86\text{ V}$<br>$I_{OUT} = 300\text{ mA}$                                                                   |                               | 2                             | 15    | mV                  |
| $V_{S\_LOAD}$                  | Static load regulation                    | $I_{OUT} = 1\text{ mA to } 300\text{ mA}$                                                                                                                                      |                               | 5                             | 20    | mV                  |
| $V_{TR\_LINE}$                 | Line transient response                   | $V_{DD} = V_{SYS} = 2.8\text{ V to } 5.5\text{ V}$<br>$V_{LDO} = 1.86\text{ V}$<br>$I_{OUT} = 300\text{ mA}$<br>$t_r = t_f = 10\text{ }\mu\text{s}$                            |                               | 5                             | 10    | mV                  |
| $V_{TR\_LOAD}$                 | Load transient response                   | $V_{DD} = 3.6\text{ V}$<br>$I_{OUT} = 1\text{ mA to } 300\text{ mA}$<br>$t_r = t_f = 1\text{ }\mu\text{s}$                                                                     |                               | 30                            | 50    | mV                  |
| PSRR<br><a href="#">Note 4</a> | PSRR                                      | $f = 10\text{ Hz to } 10\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 3.6\text{ V}$ , $I_{OUT} = I_{MAX}/2$<br>$V_{DD} - V_{LDO} \geq 0.6\text{ V}$                 | 60                            | 70                            |       | dB                  |
| N                              | Output noise                              | $V_{DD} = V_{SYS} = 3.6\text{ V}$ ,<br>$V_{LDO} = 2.8\text{ V}$<br>$I_{OUT} = 5\text{ mA to } I_{MAX}$<br>$f = 10\text{ Hz to } 100\text{ kHz}$ , $25\text{ }^{\circ}\text{C}$ |                               | 70                            |       | $\mu\text{V}_{rms}$ |
| $I_{Q\_ON}$                    | Quiescent current in ON mode              | <a href="#">Note 5</a>                                                                                                                                                         |                               | 9 +<br>0.45 %<br>of $I_{OUT}$ |       | $\mu\text{A}$       |

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| Parameter             | Description                         | Conditions                                 | Min | Typ                           | Max | Unit |
|-----------------------|-------------------------------------|--------------------------------------------|-----|-------------------------------|-----|------|
| I <sub>Q_SLEEP</sub>  | Quiescent current forced sleep mode |                                            |     | 2 + 0.7 % of I <sub>OUT</sub> |     | μA   |
| I <sub>Q_OFF</sub>    | Quiescent current OFF mode          |                                            |     | 1                             |     | μA   |
| t <sub>ON</sub>       | Turn-on time                        | 10 % to 90 %                               |     |                               | 200 | μs   |
|                       |                                     | SLEEP mode                                 |     |                               | 260 |      |
| t <sub>OFF</sub>      | Turn off time                       | 90 % to 10 %<br>Pull-down resistor enabled |     |                               | 1   | ms   |
| R <sub>OFF</sub>      | Pull-down resistance in OFF mode    | Can be disabled via LDO11_PD_DIS           |     | 55                            |     | Ω    |
| <b>Bypass Mode</b>    |                                     |                                            |     |                               |     |      |
| R <sub>ON</sub>       | Bypass on-resistance                | V <sub>DD</sub> > 2.2 V                    |     | 0.3                           | 0.7 | Ω    |
|                       |                                     | V <sub>DD</sub> > 1.8 V                    |     |                               | 1.0 |      |
| I <sub>LIM</sub>      | Current limit in Bypass mode        |                                            |     | 270                           |     | mA   |
| I <sub>Q_BYPASS</sub> | Quiescent current in Bypass mode    |                                            |     | 50                            | 100 | μA   |

**Note 1** Max output current is 30% when the input voltage is 1.5 V.

**Note 2** Programmable in 50 mV voltage steps.

**Note 3** Accuracy values not applicable if bypass mode has been configured.

**Note 4** Measured at point of load.

**Note 5** Internal regulator current flowing to ground.

### 5.8.12 LDOCORE

**Table 24: LDOCORE, T<sub>J</sub> = -40 °C to 125 °C**

| Parameter             | Description             | Conditions                                    | Min   | Typ | Max   | Unit |
|-----------------------|-------------------------|-----------------------------------------------|-------|-----|-------|------|
| V <sub>DDCORE</sub>   | Output voltage          | <a href="#">Note 1</a>                        | 2.45  | 2.5 | 2.55  | V    |
|                       |                         | RESET mode                                    |       | 2.2 |       | V    |
| C <sub>OUT</sub>      | Stabilization capacitor | Including voltage and temperature coefficient | -55 % | 2.2 | +35 % | μF   |
| R <sub>COUT_ESR</sub> | Output capacitor ESR    | f > 1 MHz<br>Including wiring parasitics      | 0     |     | 300   | mΩ   |
| V <sub>DROPOUT</sub>  | Dropout voltage         | <a href="#">Note 2</a>                        |       | 50  | 100   | mV   |

**Note 1** Setting VDD\_FAULT\_LOWER ≥ 2.65 V avoids LDOCORE dropout, see Section 5.14.

**Note 2** The LDOCORE supply, VSYS or CHG\_WAKE, must be maintained above V<sub>DDCORE</sub> + V<sub>DROPOUT</sub>.

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### Note

LDOCORE is only used to supply internal circuits.

## 5.9 DC/DC Buck Converters

### 5.9.1 BUCKCORE1 and BUCKCORE2

Table 25: BUCKCORE1,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

| Parameter       | Description             | Conditions                                                                                                                                                                                | Min   | Typ    | Max                           | Unit             |
|-----------------|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|-------------------------------|------------------|
| $V_{DD}$        | Input voltage           | $V_{DD} = V_{SYS}$                                                                                                                                                                        | 2.8   |        | 5.5                           | V                |
| $C_{OUT}$       | Output capacitor        | Including voltage and temperature coefficient                                                                                                                                             |       |        |                               | $\mu\text{F}$    |
|                 |                         | Half-current mode                                                                                                                                                                         | -50 % | 2 x 22 | +30 %, <a href="#">Note 1</a> |                  |
|                 |                         | Full-current mode                                                                                                                                                                         |       | 2 x 47 |                               |                  |
| $R_{COUT\_ESR}$ | Output capacitor ESR    | Including wiring parasitics<br>$f > 100\text{ kHz}$                                                                                                                                       |       |        |                               | $\text{m}\Omega$ |
|                 |                         | Half-current mode<br>$C_{OUT} = 2 \times 22\text{ }\mu\text{F}$                                                                                                                           |       | 15     | 50                            |                  |
|                 |                         | Full-current mode<br>$C_{OUT} = 2 \times 47\text{ }\mu\text{F}$                                                                                                                           |       | 7.5    | 25                            |                  |
| $L_{BUCK}$      | Inductor value          | Including current and temperature dependence                                                                                                                                              | 0.7   | 1.0    | 1.3                           | $\mu\text{H}$    |
| $L_{ESR}$       | Inductor resistance     |                                                                                                                                                                                           |       | 55     | 100                           | $\text{m}\Omega$ |
| <b>PWM Mode</b> |                         |                                                                                                                                                                                           |       |        |                               |                  |
| $V_{BUCK}$      | Output voltage          | Programmable in 10 mV steps<br><a href="#">Note 2</a>                                                                                                                                     | 0.3   |        | 1.57                          | V                |
| $V_{BUCK\_ACC}$ | Output voltage accuracy | Excluding static line/load regulation and voltage ripple<br>$T_A = 25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 4.2\text{ V}$<br>$V_{BUCK} = 1.03\text{ V}$                                   | -1    |        | +1                            | %                |
|                 |                         | Excluding static line/load regulation and voltage ripple<br>$T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$<br>$V_{DD} = 4.2\text{ V}$<br>$V_{BUCK} = 1.03\text{ V}$ | -1.5  |        | +1.5                          |                  |
|                 |                         | Including static line/load regulation and voltage ripple<br>$I_{OUT} = I_{MAX}$<br>$V_{BUCK} = 1.03\text{ V}$<br>$L_{BUCK}, L_{ESR} = \text{Typ}$                                         | -2    |        | +2                            |                  |

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| Parameter                           | Description                                   | Conditions                                                                                                                                                                                             | Min   | Typ  | Max   | Unit          |
|-------------------------------------|-----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|---------------|
|                                     |                                               | Including static line/load regulation and voltage ripple<br>$I_{OUT} = I_{MAX}$<br><a href="#">Note 3</a>                                                                                              | -3    |      | +3    |               |
| $V_{TR\_LD}$                        | Transient load regulation                     | $V_{DD} = 3.6\text{ V}$<br>$V_{BUCK} = 1.2\text{ V}$<br>$I_{OUT} = 200\text{ mA} / 0.8 * I_{MAX}$<br>$di/dt = 3\text{ A}/\mu\text{s}$<br>$L_{BUCK} = 1.0\text{ }\mu\text{H}$<br><a href="#">Note 4</a> | -4    |      | +4    | %             |
| $V_{TR\_LINE}$                      | Transient line regulation                     | $V_{DD} = 3.0\text{ V to } 3.6\text{ V}$<br>$I_{OUT} = 500\text{ mA}$<br>$t_r = t_f = 10\text{ }\mu\text{s}$                                                                                           |       | 0.2  | 3     | mV            |
|                                     | Parasitic track resistance                    | From output capacitor to sense connection at point-of-load                                                                                                                                             |       | 10   |       | m $\Omega$    |
|                                     | Parasitic track inductance                    | From output capacitor to sense connection at point-of-load                                                                                                                                             |       | 5    |       | nH            |
| $Z_{FB}$                            | Feedback Comparator input impedance           |                                                                                                                                                                                                        | 500   |      |       | k $\Omega$    |
| $I_{MAX}$                           | Output current                                | Half-current mode                                                                                                                                                                                      | 1250  |      |       | mA            |
|                                     |                                               | Full-current mode                                                                                                                                                                                      | 2500  |      |       |               |
| $I_{LIM}$<br><a href="#">Note 5</a> | Current limit (programmable)                  | BCORE1_ILIM=0000                                                                                                                                                                                       | -20 % | 500  | +20 % | mA            |
|                                     |                                               | BCORE1_ILIM=1111                                                                                                                                                                                       | -20 % | 2000 | +20 % | mA            |
| $I_{Q\_OFF}$                        | Quiescent current in OFF mode                 |                                                                                                                                                                                                        |       |      | 1     | $\mu\text{A}$ |
| $I_{Q\_ON}$                         | Quiescent current in PWM mode                 | Half-current mode<br>$I_{OUT} = 0\text{ mA}$                                                                                                                                                           |       | 9.0  |       | mA            |
|                                     |                                               | Full-current mode                                                                                                                                                                                      |       | 11.0 |       |               |
| $f$                                 | Switching frequency<br><a href="#">Note 6</a> | OSC_FRQ = 0000                                                                                                                                                                                         | 2.85  | 3    | 3.15  | MHz           |
| D                                   | Switching duty cycle                          |                                                                                                                                                                                                        | 10.5  |      | 84    | %             |
| $t_{ON}$                            | Turn on time                                  | $V_{BUCK} = 1.15\text{ V}$<br>BUCK_SLOWSTART = disabled<br>$SLEW\_RATE = 10\text{ mV}/1\text{ }\mu\text{s}$<br>$BUCK<x>_{ILIM} = 1500\text{ mA}$                                                       |       | 0.37 | 1.2   | ms            |
| $R_{PD}$                            | Output pull-down resistor                     | $V_{BUCK} = 0.5\text{ V}$<br>Can be disabled via BCORE1_PD_DIS                                                                                                                                         |       | 80   | 200   | $\Omega$      |

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| Parameter             | Description                              | Conditions                                                                                               | Min | Typ | Max  | Unit |
|-----------------------|------------------------------------------|----------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| R <sub>PMOS</sub>     | PMOS ON resistance                       | Half-current mode<br>Including pin and routing<br>V <sub>sys</sub> = 3.6 V                               |     | 160 |      | mΩ   |
|                       |                                          | Full-current mode<br>Including pin and routing<br>V <sub>sys</sub> = 3.6 V                               |     | 80  |      |      |
| R <sub>NMOS</sub>     | NMOS ON resistance                       | Half-current mode<br>Including pin and routing<br>V <sub>sys</sub> = 3.6 V                               |     | 60  |      | mΩ   |
|                       |                                          | Full-current mode<br>Including pin and routing<br>V <sub>sys</sub> = 3.6 V                               |     | 30  |      |      |
| η                     | Efficiency<br><a href="#">Note 7</a>     | V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 1.2 V<br>I <sub>OUT</sub> = 0.1 to 0.7 * I <sub>MAX</sub> |     | 84  |      | %    |
| <b>PFM Mode</b>       |                                          |                                                                                                          |     |     |      |      |
| V <sub>BUCK</sub>     | Output voltage                           | Programmable in 10 mV steps                                                                              | 0.3 |     | 1.57 | V    |
| I <sub>AUTO_THR</sub> | Typical automatic mode switching current |                                                                                                          |     | 260 |      | mA   |
| I <sub>OUT_PFM</sub>  | Output current                           |                                                                                                          |     | 300 |      | mA   |
| I <sub>LIM_PFM</sub>  | Current limit                            |                                                                                                          |     | 600 |      | mA   |
| I <sub>Q_PFM</sub>    | Quiescent current                        | I <sub>OUT</sub> = 0                                                                                     |     |     |      | μA   |
|                       |                                          | Forced PFM mode                                                                                          |     | 27  | 32   |      |
|                       |                                          | AUTO mode                                                                                                |     | 35  | 42   |      |
|                       | Frequency of operation                   |                                                                                                          | 0   |     | 3    | MHz  |
| η                     | Efficiency<br><a href="#">Note 7</a>     | V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 1.2 V<br>I <sub>OUT</sub> = 10 mA                         |     | 86  |      | %    |

**Note 1** The purpose of the specified maximum C<sub>OUT</sub> value is to ensure that the specified turn-on time, t<sub>ON</sub>, can be met. Additional output rail capacitors can be added to reduce voltage ripple or to improve transient load regulation. However, this will compromise t<sub>ON</sub> performance, create larger in-rush currents and will affect DVC slew rates.

**Note 2** If BUCK<x>\_MODE = 10 (synchronous) then the buck operates in PFM mode when V<sub>BUCK</sub> < 0.7 V. For complete control of the buck mode (PWM versus PFM) use BUCK<x>\_MODE = 00.

**Note 3** Minimum tolerance 35 mV.

**Note 4** Measured at C<sub>OUT</sub>, depends on parasitics of PCB and external components when remote sensing.

**Note 5** Current limit values are doubled in full-current mode.

**Note 6** Generated from internal 6 MHz oscillator and can be adjusted by ± 10 % via control OSC\_FRQ.

**Note 7** Depends on external components and PCB routing.

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### 5.9.2 BUCKPRO

Table 26: BUCKPRO,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

| Parameter             | Description               | Conditions                                                                                                                                                                           | Min   | Typ    | Max                           | Unit |
|-----------------------|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|-------------------------------|------|
| V <sub>DD</sub>       | Input voltage             | V <sub>DD</sub> = V <sub>SYS</sub>                                                                                                                                                   | 2.8   |        | 5.5                           | V    |
| C <sub>OUT</sub>      | Output capacitor          | Including voltage and temperature coefficient                                                                                                                                        |       |        |                               | μF   |
|                       |                           | Half-current mode                                                                                                                                                                    | -50 % | 2 * 22 | +30 %, <a href="#">Note 1</a> |      |
|                       |                           | Full-current mode                                                                                                                                                                    |       | 2 * 47 |                               |      |
| R <sub>COUT_ESR</sub> | Output capacitor ESR      | Including wiring parasitics<br>f > 100 kHz                                                                                                                                           |       |        |                               | mΩ   |
|                       |                           | Half-current mode<br>C <sub>OUT</sub> = 2 * 22 μF                                                                                                                                    |       | 15     | 50                            |      |
|                       |                           | Full-current mode<br>C <sub>OUT</sub> = 2 * 47 μF                                                                                                                                    |       | 7.5    | 25                            |      |
| L <sub>BUCK</sub>     | Inductor value            | Including current and temperature dependence                                                                                                                                         | 0.7   | 1.0    | 1.3                           | μH   |
| L <sub>ESR</sub>      | Inductor resistance       |                                                                                                                                                                                      |       | 55     | 100                           | mΩ   |
| PWM Mode              |                           |                                                                                                                                                                                      |       |        |                               |      |
| V <sub>BUCK</sub>     | Output voltage            | Programmable in 10 mV steps<br><a href="#">Note 2</a>                                                                                                                                | 0.53  |        | 1.8                           | V    |
| V <sub>BUCK_ACC</sub> | Output voltage accuracy   | Including static line/load regulation and voltage ripple<br>I <sub>OUT</sub> = I <sub>MAX</sub><br><a href="#">Note 3</a>                                                            | -3    |        | +3                            | %    |
|                       |                           | Excluding static line/load regulation and voltage ripple<br>T <sub>A</sub> = 25 °C<br>V <sub>BUCK</sub> > 1 V<br>V <sub>DD</sub> = 5 V                                               | -1    |        | +1                            |      |
| V <sub>TR_LD</sub>    | Transient load regulation | V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 1.2 V<br>I <sub>OUT</sub> = 200 mA / 0.8 * I <sub>MAX</sub><br>dI/dt = 3 A/μs<br>L <sub>BUCK</sub> = 1.0 μH<br><a href="#">Note 4</a> |       | 20     | 50                            | mV   |
| V <sub>TR_LINE</sub>  | Transient line regulation | V <sub>DD</sub> = 3.0 V to 3.6 V<br>I <sub>OUT</sub> = 500 mA<br>tr = tf = 10 μs                                                                                                     |       | 0.2    | 3                             | mV   |
| I <sub>MAX</sub>      | Output current            | Half-current mode                                                                                                                                                                    | 1250  |        |                               | mA   |
|                       |                           | Full-current mode                                                                                                                                                                    | 2500  |        |                               |      |
| I <sub>LIM</sub>      | Current limit             | BPRO_ILIM=0000                                                                                                                                                                       | -20 % | 500    | +20 %                         | mA   |

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| Parameter             | Description                              | Conditions                                                                                                  | Min   | Typ  | Max   | Unit |
|-----------------------|------------------------------------------|-------------------------------------------------------------------------------------------------------------|-------|------|-------|------|
| Note 7                | (programmable)                           | BPRO_ILIM=1111                                                                                              | -20 % | 2000 | +20 % | mA   |
| I <sub>Q_OFF</sub>    | Quiescent current in OFF mode            |                                                                                                             |       |      | 1     | μA   |
| I <sub>Q_ON</sub>     | Quiescent current in PWM mode            | Half-current mode                                                                                           |       | 9.0  |       | mA   |
|                       |                                          | Full-current mode                                                                                           |       | 11.0 |       |      |
| f                     | Switching frequency<br>Note 5            | OSC_FRQ = 0000                                                                                              | 2.85  | 3    | 3.15  | MHz  |
| D                     | Switching duty cycle                     |                                                                                                             | 10.6  |      | 84    | %    |
| R <sub>PD</sub>       | Output pull-down resistor                | @ V <sub>OUT</sub> = 0.5 V<br>Can be disabled via BPRO_PD_DIS                                               |       | 80   | 200   | Ω    |
| R <sub>PMOS</sub>     | PMOS ON resistance                       | Half-current mode<br>Including pin and routing<br>V <sub>SYS</sub> = 3.6 V                                  |       | 160  |       | mΩ   |
|                       |                                          | Full-current mode<br>Including pin and routing<br>V <sub>SYS</sub> = 3.6 V                                  |       | 80   |       |      |
| R <sub>NMOS</sub>     | NMOS ON resistance                       | Half-current mode<br>Including pin and routing<br>V <sub>SYS</sub> = 3.6 V                                  |       | 60   |       | mΩ   |
|                       |                                          | Full-current mode<br>Including pin and routing<br>V <sub>SYS</sub> = 3.6 V                                  |       | 30   |       |      |
| η                     | Efficiency<br>Note 6                     | V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 1.2 V<br>I <sub>OUT</sub> = 0.1 mA to 0.7 * I <sub>MAX</sub> |       | 84   |       | %    |
| <b>PFM Mode</b>       |                                          |                                                                                                             |       |      |       |      |
| V <sub>BUCK</sub>     | Output voltage                           | Programmable in 10 mV steps                                                                                 | 0.53  |      | 1.8   | V    |
| I <sub>AUTO_THR</sub> | Typical automatic mode switching current |                                                                                                             |       | 260  |       | mA   |
| I <sub>OUT_PFM</sub>  | Output current                           |                                                                                                             |       | 300  |       | mA   |
| I <sub>LIM</sub>      | Current limit                            |                                                                                                             |       | 600  |       | mA   |
| I <sub>Q_PFM</sub>    | Quiescent current                        | I <sub>OUT</sub> = 0 mA                                                                                     |       |      |       | μA   |
|                       |                                          | Forced PFM mode                                                                                             |       | 22   | 25    |      |
|                       |                                          | AUTO mode                                                                                                   |       | 30   | 35    |      |
| f                     | Frequency of operation                   |                                                                                                             | 0     |      | 3     | MHz  |
| η                     | Efficiency<br>Note 6                     | V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 1.2 V<br>I <sub>OUT</sub> = 10 mA                            |       | 86   |       | %    |
| <b>VTT Mode</b>       |                                          |                                                                                                             |       |      |       |      |
| V <sub>DD</sub>       | Input voltage                            | V <sub>DD</sub> = V <sub>SYS</sub>                                                                          | 2.8   |      | 5.5   | V    |

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| Parameter             | Description               | Conditions                                                                                                                                                                                                 | Min   | Typ    | Max                           | Unit |
|-----------------------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|-------------------------------|------|
| C <sub>OUT</sub>      | Output capacitor          | Including voltage and temperature coefficient                                                                                                                                                              | -50 % | 2 * 47 | +30 %, <a href="#">Note 1</a> | μF   |
| R <sub>COUT_ESR</sub> | Output capacitor ESR      | ESR of C <sub>OUT</sub><br>@ f > 100 kHz + track impedance                                                                                                                                                 |       | 7.5    | 25                            | mΩ   |
| L <sub>BUCK</sub>     | Inductor value            | Including current and temperature dependence                                                                                                                                                               |       | 0.25   |                               | μH   |
| L <sub>ESR</sub>      | Inductor resistance       |                                                                                                                                                                                                            |       | 55     | 100                           | mΩ   |
| V <sub>BUCK</sub>     | Output voltage            | V <sub>BUCK</sub> = V <sub>DDQ</sub> /2                                                                                                                                                                    | 0.675 |        | 1.3                           | V    |
| V <sub>BUCK_ACC</sub> | Output voltage accuracy   | Relative to VTTR<br>Including static line and load regulation                                                                                                                                              | - 3   |        | 4                             | %    |
| V <sub>TR_LD</sub>    | Transient load regulation | Half-current mode<br>V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 0.7 V<br>I <sub>OUT</sub> = 10 mA to 1 A<br>I <sub>OUT</sub> = -750 mA to -10 mA<br>L <sub>BUCK</sub> = 0.24 μH<br>dI/dt = 3 A/μs      |       | 20     | 40                            | mV   |
|                       |                           | Full-current mode<br>V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 0.75 V<br>I <sub>OUT</sub> = 10 mA to 1.4 A<br>I <sub>OUT</sub> = -10 mA to -1.4 A<br>L <sub>BUCK</sub> = 0.24 μH<br>dI/dt = 3 A/μs    |       | 20     | 40                            |      |
|                       |                           | Full-current mode<br>V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 0.7 V<br>I <sub>OUT</sub> = 10 mA to 1.1 A<br>I <sub>OUT</sub> = -10 mA to -1.1 A<br>L <sub>BUCK</sub> = 0.24 μH<br>dI/dt = 3 A/μs     |       | 20     | 40                            |      |
|                       |                           | Full-current mode<br>V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 0.675 V<br>I <sub>OUT</sub> = 10 mA to 900 mA<br>I <sub>OUT</sub> = -10 mA to -900 mA<br>L <sub>BUCK</sub> = 0.24 μH<br>dI/dt = 3 A/μs |       | 20     | 40                            |      |
| I <sub>MAX</sub>      | Maximum output current    | Half-current mode<br>V <sub>BUCK</sub> = 0.7 V                                                                                                                                                             | -550  |        | 1250                          | mA   |
|                       |                           | Full-current mode<br>V <sub>BUCK</sub> = 0.75                                                                                                                                                              | -1400 |        | 2500                          |      |
|                       |                           | Full-current mode<br>V <sub>BUCK</sub> = 0.7 V                                                                                                                                                             | -1100 |        | 2500                          |      |
|                       |                           | Full-current mode<br>V <sub>BUCK</sub> = 0.675 V                                                                                                                                                           | -900  |        | 2500                          |      |

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| Parameter          | Description         | Conditions                                                                                                                                              | Min   | Typ         | Max   | Unit          |
|--------------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------------|-------|---------------|
| $t_{ON}$           | Turn-on time        | $V_{BUCK} = 0.75\text{ V}$<br>$BUCK\_SLOWSTART = \text{disabled}$<br>$SLEW\_RATE = 10\text{ mV}/1\text{ }\mu\text{s}$<br>$BUCK4\_ILIM = 1500\text{ mA}$ |       | 0.33        | 1.2   | Ms            |
| <b>VTTR Buffer</b> |                     |                                                                                                                                                         |       |             |       |               |
| $V_{DDQ}$          | Feedback voltage    | $V_{DD} = V_{SYS}$                                                                                                                                      | 1.35  |             | 2.6   | V             |
| $V_{VTTR}$         | Output voltage      | $I_{OUT} = 0\text{ mA}$ to $I_{VTTR}$                                                                                                                   | 0.675 | $V_{DDQ}/2$ | 1.3   | V             |
| $V_{VTTR\_ACC}$    | Voltage accuracy    | $V_{VTTR\_ACC}$ related to $V_{DDQ}$ input voltage                                                                                                      | -1    | $V_{DDQ}/2$ | +1    | %             |
| $C_{OUT}$          | Output capacitor    | Including voltage and temperature coefficient                                                                                                           | -50 % | 0.1         | +30 % | $\mu\text{F}$ |
| $I_{OUT}$          | Sink/source current |                                                                                                                                                         | -10   |             | 10    | mA            |

**Note 1** The purpose of the specified maximum  $C_{OUT}$  value is to ensure that the specified turn-on time,  $t_{ON}$ , can be met. Additional output rail capacitors can be added to reduce voltage ripple or to improve transient load regulation. However, this will compromise  $t_{ON}$  performance, create larger in-rush currents and will affect DVC slew rates.

**Note 2** If  $BUCK<X>\_MODE = 10$  (synchronous) then the buck operates in PFM mode when  $V_{BUCK} < 0.7\text{ V}$ . For complete control of the buck mode (PWM versus PFM) use  $BUCK<X>\_MODE = 00$ .

**Note 3** Minimum tolerance 35 mV.

**Note 4** Measured at  $C_{OUT}$ , depends on parasitics of PCB and external components when remote sensing.

**Note 5** Generated from internal 6 MHz oscillator and can be adjusted by  $\pm 10\%$  via control  $OSC\_FRQ$ .

**Note 6** Depends on external components and PCB routing.

**Note 7** Current limit values are doubled in full-current mode.

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### 5.9.3 BUCKMEM

Table 27: BUCKMEM,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

| Parameter                           | Description                                   | Conditions                                                                                                                                                      | Min   | Typ    | Max                           | Unit             |
|-------------------------------------|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|-------------------------------|------------------|
| $V_{DD}$                            | Input voltage                                 | $V_{DD} = V_{SYS}$                                                                                                                                              | 2.8   |        | 5.5                           | V                |
| $C_{OUT}$                           | Output capacitor                              | Including voltage and temperature coefficient                                                                                                                   | -50 % | 2 * 22 | +30 %, <a href="#">Note 1</a> | $\mu\text{F}$    |
|                                     |                                               | Merged mode                                                                                                                                                     |       | 2 * 47 |                               |                  |
| $R_{COUT\_ESR}$                     | Output capacitor ESR                          | Including wiring parasitics $f > 100\text{ kHz}$                                                                                                                |       |        |                               |                  |
|                                     |                                               | $C_{OUT} = 2 * 22\text{ }\mu\text{F}$                                                                                                                           |       | 15     | 50                            | $\text{m}\Omega$ |
|                                     |                                               | $C_{OUT} = 2 * 47\text{ }\mu\text{F}$                                                                                                                           |       | 7.5    | 25                            |                  |
| $L_{BUCK}$                          | Inductor value                                | Including current and temperature dependence                                                                                                                    | 0.7   | 1.0    | 1.3                           | $\mu\text{H}$    |
| $L_{ESR}$                           | Inductor resistance                           |                                                                                                                                                                 |       | 55     | 100                           | $\text{m}\Omega$ |
| $V_{BUCK}$                          | Output voltage                                | Programmable in 20 mV steps                                                                                                                                     | 0.8   |        | 3.34, <a href="#">Note 7</a>  | V                |
| $V_{BUCK\_ACC}$                     | Output voltage accuracy                       | Including static line/load regulation and voltage ripple<br>$I_{OUT} = I_{MAX}$<br><a href="#">Note 2</a>                                                       | -3    |        | +3                            | %                |
|                                     |                                               | Excluding static line/load regulation and voltage ripple<br>$T_A = 25\text{ }^{\circ}\text{C}$<br>$V_{DD} = 5\text{ V}$<br>$V_{BUCK} > 1\text{ V}$              | -2    |        | +2                            |                  |
| $V_{TR\_LD}$                        | Transient load regulation                     | $V_{DD} = 3.6\text{ V}$<br>$V_{BUCK} = 1.2\text{ V}$<br>$I_{OUT} = 200\text{ mA} / 0.8 * I_{MAX}$<br>$dI/dt = 3\text{ A}/\mu\text{s}$<br><a href="#">Note 3</a> | -4    |        | +4                            | %                |
| $V_{TR\_LINE}$                      | Transient line regulation                     | $V_{DD} = 3.0\text{ V}$ to $3.6\text{ V}$<br>$I_{OUT} = 500\text{ mA}$<br>$t_r = t_f = 10\text{ }\mu\text{s}$                                                   |       | 0.2    | 3                             | mV               |
| $I_{MAX}$                           | Output current                                |                                                                                                                                                                 | 1500  |        |                               | mA               |
| $I_{LIM}$<br><a href="#">Note 4</a> | Current limit (programmable)                  | BMEM_ILIM = 0000                                                                                                                                                | -20 % | 1500   | +20 %                         | mA               |
|                                     |                                               | BMEM_ILIM = 1111                                                                                                                                                | -20 % | 3000   | +20 %                         | mA               |
| $I_{Q\_OFF}$                        | Quiescent current in OFF mode                 |                                                                                                                                                                 |       |        | 1                             | $\mu\text{A}$    |
| $I_{Q\_ON}$                         | Quiescent current in PWM mode                 | $I_{OUT} = 0\text{ mA}$                                                                                                                                         |       | 9      |                               | mA               |
| $f_{SW}$                            | Switching frequency<br><a href="#">Note 5</a> | OSC_FRQ = 0000                                                                                                                                                  | 2.85  | 3      | 3.15                          | MHz              |

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| Parameter           | Description                              | Conditions                                                                                                                         | Min  | Typ | Max                            | Unit          |
|---------------------|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|------|-----|--------------------------------|---------------|
| D                   | Switching duty cycle                     |                                                                                                                                    | 14.5 |     | 100                            | %             |
|                     | Output pull-down resistor                | $V_{\text{BUCK}} = 0.5 \text{ V}$<br>Disabled via<br>BMEM_PD_DIS                                                                   |      | 80  | 200                            | $\Omega$      |
| $R_{\text{PMOS}}$   | PMOS ON resistance                       | Including pin and routing<br>$V_{\text{SYS}} = 3.6 \text{ V}$                                                                      |      | 160 |                                | m $\Omega$    |
| $R_{\text{NMOS}}$   | NMOS ON resistance                       | Including pin and routing<br>$V_{\text{SYS}} = 3.6 \text{ V}$                                                                      |      | 60  |                                | m $\Omega$    |
| $\eta$              | Efficiency<br><a href="#">Note 6</a>     | $V_{\text{DD}} = 3.6 \text{ V}$<br>$V_{\text{BUCK}} = 1.2 \text{ V}$<br>$I_{\text{OUT}} = 0.1 \text{ mA to } 0.7 * I_{\text{MAX}}$ |      | 83  |                                | %             |
| <b>PFM Mode</b>     |                                          |                                                                                                                                    |      |     |                                |               |
| $V_{\text{BUCK}}$   | Output voltage                           | Programmable in 20 mV steps                                                                                                        | 0.8  |     | 3.34<br><a href="#">Note 7</a> | V             |
|                     | Typical automatic mode switching current |                                                                                                                                    |      | 260 |                                | mA            |
| $I_{\text{MAX}}$    | Output current                           |                                                                                                                                    |      | 300 |                                | mA            |
| $I_{\text{LIM}}$    | Current limit                            |                                                                                                                                    |      | 600 |                                | mA            |
| $I_{\text{Q\_PFM}}$ | Quiescent current                        | $I_{\text{OUT}} = 0 \text{ mA}$                                                                                                    |      |     |                                | $\mu\text{A}$ |
|                     |                                          | Forced PFM mode                                                                                                                    |      | 22  | 25                             |               |
|                     |                                          | AUTO mode                                                                                                                          |      | 30  | 35                             |               |
| f                   | Frequency of operation                   |                                                                                                                                    | 0    |     | 3                              | MHz           |
| $\eta$              | Efficiency<br><a href="#">Note 6</a>     | $V_{\text{DD}} = 3.6 \text{ V}$<br>$V_{\text{BUCK}} = 1.2 \text{ V}$<br>$I_{\text{OUT}} = 10 \text{ mA}$                           |      | 86  |                                | %             |

**Note 1** The purpose of the specified maximum  $C_{\text{OUT}}$  value is to ensure that the specified turn-on time,  $t_{\text{ON}}$ , can be met. Additional output rail capacitors can be added to reduce voltage ripple or to improve transient load regulation. However, this will compromise  $t_{\text{ON}}$  performance, create larger in-rush currents and will affect DVC slew rates.

**Note 2** Minimum tolerance 35 mV.

**Note 3** Measured at  $C_{\text{OUT}}$ , depends on parasitics of PCB and external components when remote sensing.

**Note 4** The current limits are automatically doubled when BUCKMEM is merged with BUCKIO.

**Note 5** Generated from internal 6 MHz oscillator and can be adjusted by  $\pm 10 \%$  via control OSC\_FRQ.

**Note 6** Depends on external components and PCB routing.

**Note 7** Maximum  $V_{\text{DD}} - 0.7 \text{ V}$ .

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### 5.9.4 BUCKIO

**Table 28: BUCKIO,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter       | Description                   | Conditions                                                                                                  | Min   | Typ    | Max             | Unit          |
|-----------------|-------------------------------|-------------------------------------------------------------------------------------------------------------|-------|--------|-----------------|---------------|
| $V_{DD}$        | Input voltage                 | $V_{DD} = V_{SYS}$                                                                                          | 2.8   |        | 5.5             | V             |
| $C_{OUT}$       | Output capacitor              | Including voltage and temperature coefficient                                                               | -50%  | 2x22   | +30%,<br>Note 1 | $\mu\text{F}$ |
| $R_{COUT\_ESR}$ | Output capacitor ESR          | $f > 100\text{ kHz}$<br>All caps + track impedance                                                          |       | 15     | 50              | m $\Omega$    |
| $L_{BUCK}$      | Inductor value                | Including current and temperature dependence                                                                | 0.7   | 1.0    | 1.3             | $\mu\text{H}$ |
| $L_{ESR}$       | Inductor resistance           |                                                                                                             |       | 55     | 100             | m $\Omega$    |
| <b>PWM Mode</b> |                               |                                                                                                             |       |        |                 |               |
| $V_{BUCK}$      | Output voltage                | Programmable in 20 mV steps<br>Note 2                                                                       | 0.8   |        | 3.34<br>Note 3  | V             |
| $V_{BUCK\_ACC}$ | Output voltage accuracy       | Including static line/load regulation and voltage ripple @ $I_{OUT} = I_{MAX}$                              | -3    | Note 4 | +3              | %             |
|                 |                               | $T_A = 25\text{ }^{\circ}\text{C}$<br>$I_{OUT} = 0$<br>$V_{OUT} > 1\text{ V}$<br>$V_{DD} = 5\text{ V}$      | -2    |        | +2              |               |
| $V_{TR\_LD}$    | Transient load regulation     | $I_{OUT} = 200\text{ mA}/0.8 * I_{MAX}$<br>$dI/dt = 3\text{ A}/\mu\text{s}$                                 | -4    | Note 5 | +4              | %             |
| $V_{TR\_LINE}$  | Transient line regulation     | $V_{DD} = 3.0\text{ V}$ to $3.6\text{ V}$<br>$I_{OUT} = 500\text{ mA}$<br>$tr = tf = 10\text{ }\mu\text{s}$ |       | 0.2    | 3               | mV            |
| $I_{MAX}$       | Output current                |                                                                                                             | 1500  |        |                 | mA            |
| $I_{LIM}$       | Current limit (programmable)  | BIO_ILIM=0000                                                                                               | -20 % | 1500   | 20 %            | mA            |
|                 |                               | BIO_ILIM=1111                                                                                               | -20 % | 3000   | 20 %            | mA            |
| $I_{Q\_OFF}$    | Quiescent current in OFF mode |                                                                                                             |       |        | 1               | $\mu\text{A}$ |
| $I_{Q\_ON}$     | Quiescent current in PWM mode |                                                                                                             |       | 9      |                 | mA            |
| $f_{SW}$        | Switching frequency           |                                                                                                             | 2.85  | 3      | 3.15            | MHz           |
| D               | Switching duty cycle          |                                                                                                             | 14.5  |        | 100             | %             |
|                 | Output pull-down resistor     | $V_{OUT} = 0.5\text{ V}$<br>Can be disabled via BIO_PD_DIS                                                  |       | 80     | 200             | $\Omega$      |
| $R_{PMOS}$      | PMOS ON resistance            | Including pin and routing<br>$V_{SYS} = 3.6\text{ V}$                                                       |       | 160    |                 | m $\Omega$    |

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| Parameter          | Description                              | Conditions                                                                                               | Min | Typ | Max | Unit |
|--------------------|------------------------------------------|----------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| R <sub>NMOS</sub>  | NMOS ON resistance                       | Including pin and routing<br>V <sub>SYS</sub> = 3.6 V                                                    |     | 60  |     | mΩ   |
| η                  | Efficiency<br><a href="#">Note 6</a>     | V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 1.8 V<br>I <sub>OUT</sub> = 0.1 to 0.7 * I <sub>MAX</sub> |     | 87  |     | %    |
| <b>PFM Mode</b>    |                                          |                                                                                                          |     |     |     |      |
|                    | Typical automatic mode switching current |                                                                                                          |     | 260 |     | mA   |
| I <sub>MAX</sub>   | Output current                           |                                                                                                          |     | 300 |     | mA   |
| I <sub>LIM</sub>   | Current limit                            |                                                                                                          |     | 600 |     | mA   |
| I <sub>Q_PFM</sub> | Quiescent current                        | I <sub>OUT</sub> = 0 mA                                                                                  |     |     |     | μA   |
|                    |                                          | Forced PFM mode                                                                                          |     | 22  | 25  |      |
|                    |                                          | AUTO mode                                                                                                |     | 30  | 35  |      |
| f                  | Frequency of operation                   |                                                                                                          | 0   |     | 3   | MHz  |
| η                  | Efficiency<br><a href="#">Note 6</a>     | V <sub>DD</sub> = 3.6 V<br>V <sub>BUCK</sub> = 1.8 V<br>I <sub>OUT</sub> = 10 mA                         |     | 90  |     | %    |

**Note 1** The purpose of the specified maximum C<sub>OUT</sub> value is to ensure that the specified turn-on time, t<sub>ON</sub>, can be met. Additional output rail capacitors can be added to reduce voltage ripple or to improve transient load regulation. However, this will compromise t<sub>ON</sub> performance, create larger in-rush currents and will affect DVC slew rates.

**Note 2** If BUCK<x>\_MODE = 10 (synchronous) then the buck operates in PFM mode when V<sub>BUCK</sub> < 0.7 V. For complete control of the buck mode (PWM versus PFM) use BUCK<x>\_MODE = 00.

**Note 3** Maximum V<sub>DD</sub> - 0.7 V.

**Note 4** Minimum tolerance 35 mV.

**Note 5** Measured at C<sub>OUT</sub>, depends on parasitics of PCB and external components when remote sensing.

**Note 6** Depends on external components and PCB routing.

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### 5.9.5 BUCKPERI

**Table 29: BUCKPERI,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter       | Description                   | Conditions                                                                                                    | Min   | Typ                    | Max                           | Unit          |
|-----------------|-------------------------------|---------------------------------------------------------------------------------------------------------------|-------|------------------------|-------------------------------|---------------|
| $V_{DD}$        | Input voltage                 | $V_{DD} = V_{SYS}$                                                                                            | 2.8   |                        | 5.5                           | V             |
| $C_{OUT}$       | Output capacitor              | Including voltage and temperature coefficient                                                                 | -50 % | 2 x 22                 | +30 %, <a href="#">Note 1</a> | $\mu\text{F}$ |
| $R_{COUT\_ESR}$ | Output capacitor ESR          | $f > 100\text{ kHz}$<br>All caps + track impedance                                                            |       | 15                     | 50                            | m $\Omega$    |
| $L_{BUCK}$      | Inductor value                | Including current and temperature dependence                                                                  | 0.7   | 1.0                    | 1.3                           | $\mu\text{H}$ |
| $L_{ESR}$       | Inductor resistance           |                                                                                                               |       | 55                     | 100                           | m $\Omega$    |
| $V_{BUCK}$      | Output voltage                | Programmable in 20 mV steps<br><a href="#">Note 2</a>                                                         | 0.8   |                        | 3.34 <a href="#">Note 3</a>   | V             |
| $V_{BUCK\_ACC}$ | Output voltage accuracy       | Including static line/load regulation and voltage ripple<br>$I_{OUT} = I_{MAX}$                               | -3    | <a href="#">Note 4</a> | +3                            | %             |
|                 |                               | $T_A = 25\text{ }^{\circ}\text{C}$<br>$I_{OUT} = 0$<br>$V_{OUT} > 1\text{ V}$<br>$V_{DD} = 5\text{ V}$        | -2    |                        | +2                            |               |
| $V_{TR\_LD}$    | Transient load regulation     | $I_{OUT} = 200\text{ mA}/0.8 * I_{MAX}$<br>$dI/dt = 3\text{ A}/\mu\text{s}$                                   | -4    | <a href="#">Note 5</a> | +4                            | %             |
| $V_{TR\_LINE}$  | Transient line regulation     | $V_{DD} = 3.0\text{ V}$ to $3.6\text{ V}$<br>$I_{OUT} = 500\text{ mA}$<br>$t_r = t_f = 10\text{ }\mu\text{s}$ |       | 0.2                    | 3                             | mV            |
| $I_{MAX}$       | Output current                |                                                                                                               | 1500  |                        |                               | mA            |
| $I_{LIM}$       | Current limit (programmable)  | BPERI_ILIM = 0000                                                                                             | -20%  | 1500                   | +20%                          | mA            |
|                 |                               | BPERI_ILIM = 1111                                                                                             | -20%  | 3000                   | +20%                          | mA            |
| $I_{Q\_OFF}$    | Quiescent current in OFF mode |                                                                                                               |       | 1                      | $\mu\text{A}$                 |               |
| $I_{Q\_ON}$     | Quiescent current in PWM mode |                                                                                                               |       | 9                      |                               | mA            |
| $f_{SW}$        | Switching frequency           |                                                                                                               | 2.85  | 3                      | 3.15                          | MHz           |
| D               | Switching duty cycle          |                                                                                                               | 14.5  |                        | 100                           | %             |
|                 | Output pull-down resistor     | $V_{OUT} = 0.5\text{ V}$<br>Can be disabled via BPERI_PD_DIS                                                  |       | 80                     | 200                           | $\Omega$      |
| $R_{PMOS}$      | PMOS ON resistance            | Including pin and routing<br>$V_{SYS} = 3.6\text{ V}$                                                         |       | 160                    |                               | m $\Omega$    |
| $R_{NMOS}$      | NMOS ON resistance            | Including pin and routing<br>$V_{SYS} = 3.6\text{ V}$                                                         |       | 60                     |                               | m $\Omega$    |

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| Parameter       | Description                              | Conditions                                                                                       | Min | Typ | Max | Unit          |
|-----------------|------------------------------------------|--------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| $\eta$          | Efficiency<br><a href="#">Note 6</a>     | $V_{DD} = 3.6\text{ V}$<br>$V_{BUCK} = 2.86\text{ V}$<br>$I_{OUT} = 0.1\text{ to }0.7 * I_{MAX}$ |     | 91  |     | %             |
| <b>PFM Mode</b> |                                          |                                                                                                  |     |     |     |               |
|                 | Typical automatic mode switching current |                                                                                                  |     | 260 |     | mA            |
| $I_{MAX}$       | Output current                           |                                                                                                  |     | 300 |     | mA            |
| $I_{LIM}$       | Current limit                            |                                                                                                  |     | 600 |     | mA            |
| $I_{Q\_PFM}$    | Quiescent current                        | $I_{OUT} = 0\text{ mA}$                                                                          |     |     |     | $\mu\text{A}$ |
|                 |                                          | Forced PFM mode                                                                                  |     | 22  | 25  |               |
|                 |                                          | AUTO mode                                                                                        |     | 30  | 35  |               |
| f               | Frequency of operation                   |                                                                                                  | 0   |     | 3   | MHz           |
| $\eta$          | Efficiency<br><a href="#">Note 6</a>     | $V_{DD} = 3.6\text{ V}$<br>$V_{BUCK} = 2.86\text{ V}$<br>$I_{OUT} = 10\text{ mA}$                |     | 93  |     | %             |

**Note 1** The purpose of the specified maximum  $C_{OUT}$  value is to ensure that the specified turn-on time,  $t_{ON}$ , can be met. Additional output rail capacitors can be added to reduce voltage ripple or to improve transient load regulation. However, this will compromise  $t_{ON}$  performance, create larger in-rush currents and will affect DVC slew rates.

**Note 2** If  $BUCK<x>_{MODE} = 10$  (synchronous) then the buck operates in PFM mode when  $V_{BUCK} < 0.7\text{ V}$ . For complete control of the buck mode (PWM versus PFM) use  $BUCK<x>_{MODE} = 00$ .

**Note 3** Maximum  $V_{DD} - 0.7\text{ V}$ .

**Note 4** Minimum tolerance 35 mV.

**Note 5** Measured at  $C_{OUT}$ , depends on parasitics of PCB and external components when remote sensing.

**Note 6** Depends on external components and PCB routing.

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### 5.9.6 Typical Characteristics

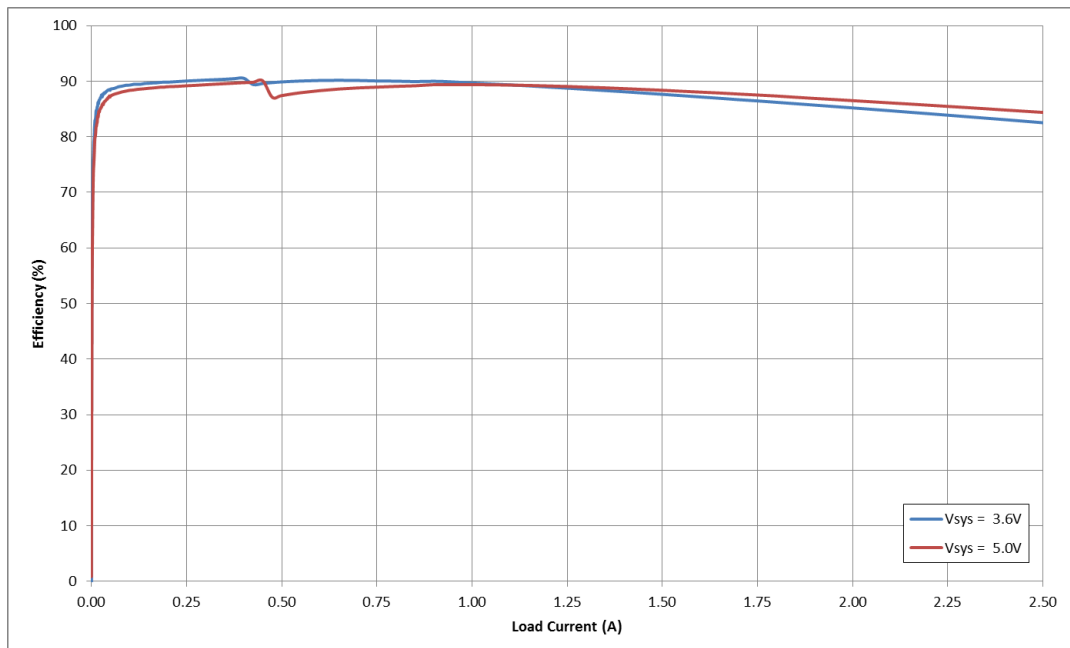


Figure 7: BUCKCORE1 Efficiency in AUTO Mode,  $V_{OUT} = 1.2\text{ V}$

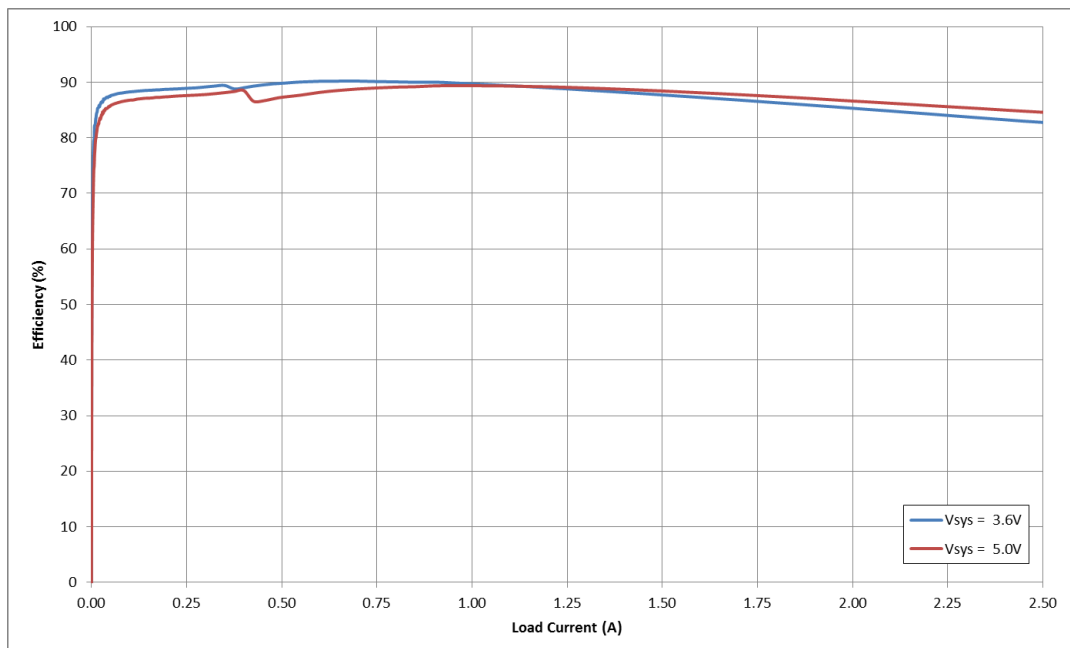


Figure 8: BUCKCORE2 Efficiency in AUTO Mode,  $V_{OUT} = 1.2\text{ V}$

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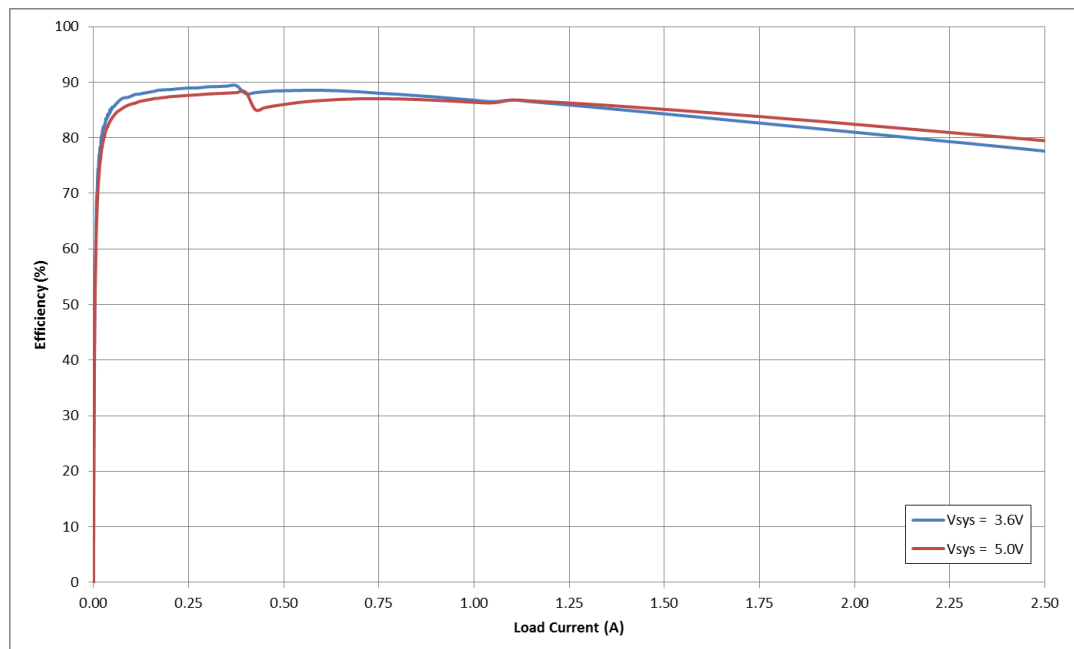


Figure 9: BUCKPRO Efficiency in AUTO Mode,  $V_{OUT} = 1.2\text{ V}$

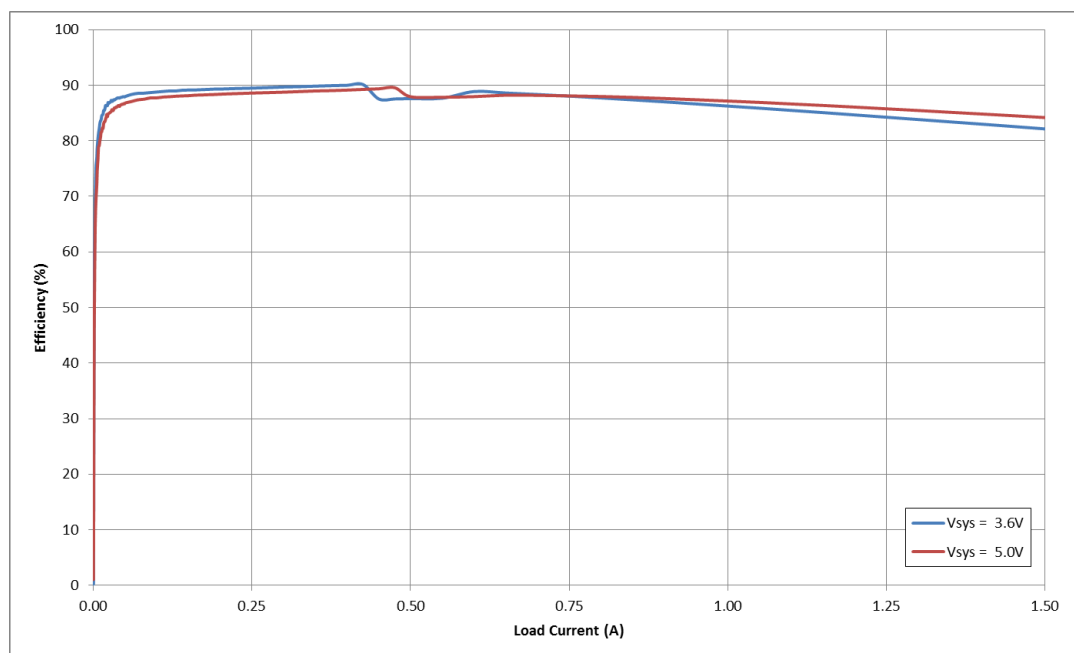


Figure 10: BUCKMEM Efficiency in AUTO Mode,  $V_{OUT} = 1.2\text{ V}$

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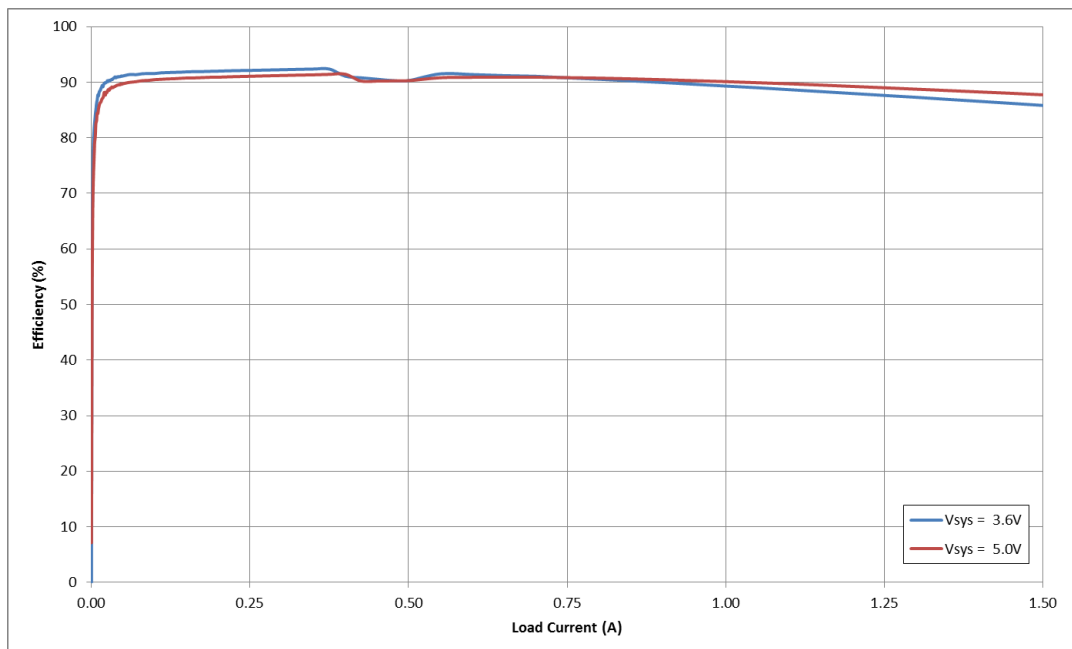


Figure 11: BUCKIO Efficiency in AUTO Mode,  $V_{OUT} = 1.8\text{ V}$

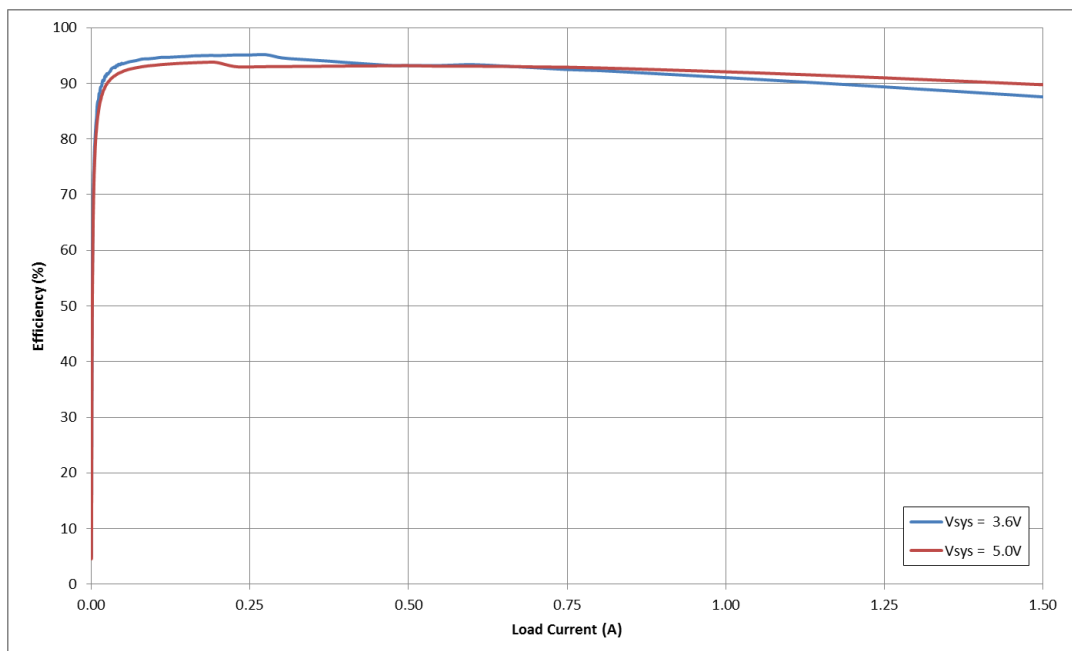


Figure 12: BUCKPERI Efficiency in AUTO Mode,  $V_{OUT} = 2.86\text{ V}$

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### 5.10 Buck Rail Switches

**Table 30: Buck Rail Switches,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter  | Description                | Conditions                                    | Min  | Typ                    | Max  | Unit              |
|------------|----------------------------|-----------------------------------------------|------|------------------------|------|-------------------|
| $V_{DD}$   | Input voltage              | $V_{DD} = V_{DDCORE}$                         | 2.45 | 2.5                    | 2.55 | V                 |
| $C_{OUT}$  | Output capacitor           | Including voltage and temperature coefficient | -30% | 47                     |      | nF                |
| $V_{CP}$   | Output voltage             | $I_{OUT} = 10\text{ }\mu\text{A}$             | 4.5  | 4.6                    |      | V                 |
| $t_{ON}$   | Charge pump turn on time   | 20 to 80% of $V_{CP}$                         |      |                        | 0.6  | ms                |
| $V_{BUCK}$ | NMOS input voltage         |                                               |      |                        | 2.8  | V                 |
|            | Gate driver source current | $V_{gate} = 4.4\text{ V}$                     |      |                        | 5    | $\mu\text{A}$     |
|            | Gate driver sink current   | $V_{gate} = 0.5\text{ V}$                     |      |                        | 180  | $\mu\text{A}$     |
|            | Voltage slew rate          |                                               | 1    | <sup>1</sup><br>Note 1 | 50   | mV/ $\mu\text{s}$ |
|            | Output pull-down resistor  | @ $V_{OUT} = 0.1\text{ V}$                    |      | 370                    |      | $\Omega$          |

**Note 1** OTP programmable via SWITCH\_SR (register SWITCH\_CONT).

### 5.11 Backup Battery Charger

**Table 31: Backup Battery Charger,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter       | Description                          | Conditions                                              | Min  | Typ                        | Max  | Unit          |
|-----------------|--------------------------------------|---------------------------------------------------------|------|----------------------------|------|---------------|
| BCHG_ISET       | Backup battery charging current      | $V_{SYS} = 3.6\text{ V}$ ,<br>$V_{BBAT} = 2.5\text{ V}$ | 100  | Note 1                     | 6000 | $\mu\text{A}$ |
| BCHG_VSET       | Charger termination voltage          | $V_{SYS} = 3.6\text{ V}$                                | 1.1  | Note 2                     | 3.1  | V             |
|                 | Backup battery short circuit current | $V_{BBAT} = 0\text{ V}$                                 |      | 6.8                        |      | mA            |
| $C_{OUT}$       | Stabilization capacitor              |                                                         | -55% | 470                        | +35% | nF            |
| $R_{COUT\_ESR}$ | ESR of capacitor                     | $f > 1\text{ MHz}$                                      |      |                            | 100  | m $\Omega$    |
| $V_{DROPOUT}$   | Dropout voltage                      | $I_{OUT} = 5\text{ mA}$                                 |      | 150                        | 200  | mV            |
| $I_Q$           | Quiescent current                    | $I_{OUT} > 50\text{ }\mu\text{A}$                       |      | 5.25+1.75%<br>of $I_{OUT}$ |      | $\mu\text{A}$ |
|                 |                                      | $I_{OUT} < 50\text{ }\mu\text{A}$                       |      | 5.25+1.5%<br>of $I_{OUT}$  |      | $\mu\text{A}$ |

**Note 1** Programmable in 100  $\mu\text{A}$  increments from 100  $\mu\text{A}$  to 1000  $\mu\text{A}$  and 1 mA increments from 1 mA to 6 mA.

**Note 2** Programmable in steps of 100 mV /200 mV.

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### 5.12 General Purpose ADC

Table 32: General Purpose ADC,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

| Parameter           | Description                                               | Conditions                                                                                                                                     | Min  | Typ       | Max   | Unit          |
|---------------------|-----------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------|-------|---------------|
| $V_{DD}$            | ADC reference voltage                                     | $V_{DD} = V_{DDCORE}$                                                                                                                          | 2.45 | 2.5       | 2.55  | V             |
|                     | Off current                                               |                                                                                                                                                |      |           | 1     | $\mu\text{A}$ |
|                     | ADC resolution                                            |                                                                                                                                                |      | 10        |       | bit           |
|                     | ADC integral non linearity                                |                                                                                                                                                |      | $\pm 2$   |       | LSB           |
|                     | ADC differential non linearity                            |                                                                                                                                                |      | $\pm 0.8$ |       | LSB           |
|                     | ADC absolute accuracy                                     | Note 4                                                                                                                                         |      | 13        | 15    | mV            |
| $R_{SRC}$<br>Note 1 | Maximum source impedance                                  |                                                                                                                                                |      |           | 120   | k $\Omega$    |
| $C_{IN}$            | Input capacitance                                         | Total input capacitance                                                                                                                        |      | 10.5      |       | pF            |
|                     | $V_{SYS}$ voltage range<br>Channel 0                      | $V_{SYS}$ minus $V_{DDCORE}$<br>$V_{SYS} = 3.125 \cdot (\text{ADC}/255) + 2.5$ (Auto)<br>$V_{SYS} = 3.125 \cdot (\text{ADC}/1023) + 2.5$ (Man) | 2.5  |           | 5.5   | V             |
|                     | ADCIN1 to 3 voltage range<br>Channel 1 to 3               | $V_{IN} = (\text{ADC} \cdot 2.5)/255$ (Auto)<br>$V_{IN} = (\text{ADC} \cdot 2.5)/1023$ (Man)                                                   | 0    |           | 2.5   | V             |
|                     | Internal temperature sensor<br>voltage range<br>Channel 4 | $T_J = -0.398 \cdot \text{ADC} + 330$                                                                                                          | 0    |           | 0.833 | V             |
|                     | $V_{BBAT}$ voltage range<br>Channel 5                     | $V_{BBAT} = (\text{ADC} \cdot 5)/1023$                                                                                                         | 0    |           | 5.0   | V             |
|                     | Regulator monitor voltage range<br>Channel 8 to 10        | $V_{REG} = (\text{ADC} \cdot 5)/255$                                                                                                           | 0    |           | 5.0   | V             |
|                     | Inter channel isolation                                   | Note 2                                                                                                                                         |      | 60        |       | dB            |
|                     | ADCIN1,2 current source<br>Note 3                         |                                                                                                                                                | -3%  | 1-40      | 3%    | $\mu\text{A}$ |
|                     | COMP1V2 comparator level<br>Channel 2                     |                                                                                                                                                |      | 1.2       |       | V             |

**Note 1**  $R_{SRC}$  is the impedance of the external source the ADC is sampling.

**Note 2** 80 dB for channel A2 (ADC\_IN2).

**Note 3** Variance guaranteed for 10  $\mu\text{A}$  to 40  $\mu\text{A}$  and up to 2 V output voltage.

**Note 4** Excludes reference voltage variation.

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### 5.13 32 kHz Oscillator

Table 33: 32 kHz Oscillator,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$

| Parameter          | Description                                               | Conditions                                  | Min              | Typ    | Max              | Unit          |
|--------------------|-----------------------------------------------------------|---------------------------------------------|------------------|--------|------------------|---------------|
| $V_{DDRTC}$        | Supply voltage                                            |                                             | 1.5              |        | 2.75             | V             |
| $f_{OSC}$          | Oscillator crystal frequency                              |                                             |                  | 32.768 |                  | kHz           |
| $R_{OSC}$          | Crystal series resistance                                 |                                             |                  |        | 100              | k $\Omega$    |
| $f_{OUT}$          | Output frequency                                          |                                             |                  | 32.768 |                  | kHz           |
| $T_{START}$        | Start-up time for cell over the voltage range             | $V_{BBAT} = 1.5\text{ V to } 2.75\text{ V}$ |                  | 0.5    | 2.0              | s             |
|                    | Current consumption from backup device during RTC mode    |                                             |                  | 0.5    |                  | $\mu\text{A}$ |
|                    | Current consumption from $V_{DDREF}$ with OUT_32K enabled |                                             |                  | 8      |                  | $\mu\text{A}$ |
|                    | Cycle-to-cycle jitter (rms)                               | 1000 pulse                                  |                  | 20     | 35               | ns            |
|                    | Period jitter (rms)                                       | 10000 pulse                                 |                  | 12     | 20               |               |
| <b>Bypass Mode</b> |                                                           |                                             |                  |        |                  |               |
| $F_{IN}$           | Input frequency                                           |                                             | -5%              | 32     | +5%              | kHz           |
| D                  | Input duty cycle                                          |                                             | 40               |        | 60               | %             |
| $V_{IH}$           | XTAL_IN<br>Input high voltage                             | RTC_EN = 0                                  | 1.8              |        | $V_{SYS}$        | V             |
|                    |                                                           | RTC_EN = 1<br>$V_{BBAT} < V_{SYS}$          | 1.1              |        |                  |               |
|                    |                                                           | RTC_EN = 1<br>$V_{BBAT} > V_{SYS}$          | $0.7 * V_{BBAT}$ |        | $V_{BBAT}$       |               |
| $V_{IL}$           | XTAL_OUT<br>Input low voltage                             | RTC_EN = 0                                  | -0.3             |        | 0.6              | V             |
|                    |                                                           | RTC_EN = 1<br>$V_{BBAT} < V_{SYS}$          |                  |        | 0.4              |               |
|                    |                                                           | RTC_EN = 1<br>$V_{BBAT} > V_{SYS}$          |                  |        | $0.2 * V_{BBAT}$ |               |
| SR                 | Input slew rate                                           | 2 pF input capacitance                      | 0.1              |        |                  | V/ns          |

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### 5.14 Internal Oscillator

**Table 34: Internal Oscillator,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter | Description                   | Conditions     | Min | Typ | Max | Unit |
|-----------|-------------------------------|----------------|-----|-----|-----|------|
| $f_{osc}$ | Internal oscillator frequency | OSC_FRQ = 0000 | 5.7 | 6.0 | 6.3 | MHz  |

**Note 1** Oscillator frequency can be further adjusted by about  $\pm 10\%$ , see Section 6.15.

### 5.15 POR, Reference Generation, and Voltage Supervision

**Table 35: POR, Reference Generation and Voltage/Temperature Supervision,  $T_J = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**

| Parameter                                        | Description                            | Conditions | Min    | Typ                                       | Max  | Unit          |
|--------------------------------------------------|----------------------------------------|------------|--------|-------------------------------------------|------|---------------|
| $V_{POR\_LOWER}$                                 | Deep discharge lockout lower threshold |            |        | 2.0                                       |      | V             |
| $V_{POR\_UPPER}$                                 | Deep discharge lockout upper threshold |            |        | 2.3                                       |      | V             |
| $V_{DD\_FAULT\_LOWER}$<br><a href="#">Note 1</a> | Under-voltage lower threshold          |            | 2.5    | 2.8                                       | 3.25 | V             |
| $V_{DD\_FAULT\_LOWER\_ACC}$                      | Under-voltage lower threshold accuracy |            |        | $\pm 2$                                   |      | %             |
| $V_{DD\_FAULT\_UPPER}$<br><a href="#">Note 2</a> | Under-voltage upper threshold          |            |        | $V_{DD\_FAULT\_LOWER} + V_{DD\_HST\_ADJ}$ |      | V             |
| $V_{REF}$                                        | Reference voltage                      |            | -1.25% | 1.2                                       | +1%  | V             |
| $V_{REF}$ decoupling capacitor                   |                                        |            |        | 0.22                                      |      | $\mu\text{F}$ |
| $V_{LNREF}$ decoupling capacitor                 |                                        |            |        | 0.22                                      |      | $\mu\text{F}$ |
| $I_{REF}$                                        | Reference current resistor             |            | -1%    | 200                                       | +1%  | k $\Omega$    |

**Note 1** During production  $V_{DD\_FAULT\_LOWER}$  voltage is configured via OTP over the range 2.5 V to 3.25 V in 50 mV steps.

**Note 2** During production the hysteresis between  $V_{DD\_FAULT\_LOWER}$  and  $V_{DD\_FAULT\_UPPER}$  is configured via OTP over the range 100 mV to 450 mV in 50 mV steps, the hysteresis can be further changed through control  $V_{DD\_HYST\_ADJ}$ .

### 5.16 Thermal Supervision

| Parameter | Description           | Conditions             | Min | Typ | Max | Unit               |
|-----------|-----------------------|------------------------|-----|-----|-----|--------------------|
| TEMP_WARN | Thermal warning       | <a href="#">Note 1</a> | 120 | 125 | 130 | $^{\circ}\text{C}$ |
| TEMP_CRIT | Thermal shutdown      | <a href="#">Note 1</a> | 135 | 140 | 145 | $^{\circ}\text{C}$ |
| TEMP_POR  | Thermal POR threshold | <a href="#">Note 1</a> | 145 | 150 | 155 | $^{\circ}\text{C}$ |

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**System PMIC for Mobile and Automotive Applications**

**Note 1** Thermal thresholds are non-overlapping.

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### 6 Functional Description

The DA9063 provides separate power domains for the host processor, memory, and peripherals to enable a flexible low-power system design. Multiple low-power modes permit varying combinations of peripherals to be powered off to conserve battery power. Other system components, such as DRAM and FLASH memory, RF transceivers, audio codec, and companion chips, are supplied from optimized regulators designed for dedicated power requirements. The DA9063 power supplies can be programmed to default voltages via OTP and provide system-configuration flexibility by selecting the power-up sequence of the regulators and switching converters.

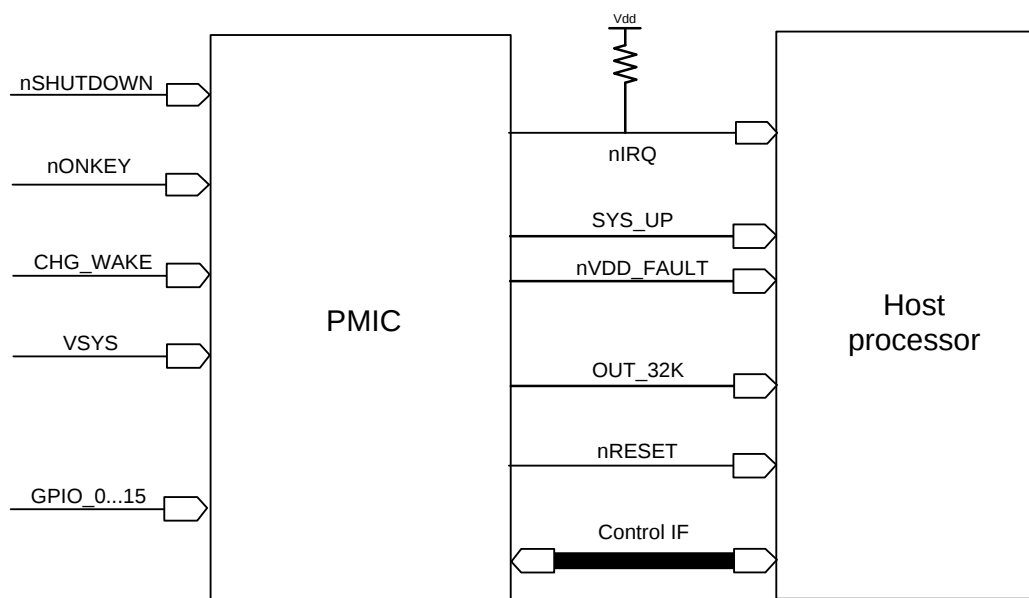


Figure 13: Control Ports and Interface

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### 6.1 Power Manager IO Ports

The power manager input ports are supplied from either the internal rail VDDCORE or VDD\_IO2, selected via PM\_I\_V. The output ports are supplied from VDD\_IO1 or VDD\_IO2, selected via PM\_O\_V (nVDD\_FAULT, GP\_FB1 via GPIO controls). During the initial start-up sequence all power manager IO ports (with the exception of nRESET and nIRQ) are in a high impedance (tri-state) mode until they are configured from OTP prior to reaching POWERDOWN mode. Output ports are push-pull except for nRESET and nIRQ, which can also be configured as open-drain via PM\_O\_TYPE. The nONKEY and CHG\_WAKE signals for the RTC block are supplied from VDDREF.

#### 6.1.1 On/Off Port (nONKEY)

The nONKEY signal is a wake-up interrupt/event intended to power-on the application supplied by DA9063. The level of the debounced signal is provided by status flag nONKEY (asserted at low level). The nONKEY unit is always enabled so that the application can be powered-on when the GPIO extender is disabled. The IRQ assertion and wake-up event can be suppressed via the interrupt mask M\_nONKEY.

nONKEY provides four modes of operation selected by field nONKEY\_PIN in register CONFIG\_I.

**Table 36: nONKEY\_PIN Settings**

| nONKEY_PIN | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00         | An E_nONKEY event is generated when the debounced signal from port nONKEY goes low (asserting edge). If not masked, an interrupt is signaled to the host via nIRQ (with wake-up during POWERDOWN mode).                                                                                                                                                                                                                                                                                                                                                                                                           |
| 01         | If (after powering up from POWERDOWN mode) the debounced signal from port nONKEY is low after an asserting edge for less than the key-press time (selected by KEY_DELAY, default 2 s), an E_nONKEY event is generated at the releasing edge. If the signal is low for longer than selected by KEY_DELAY, the DA9063 asserts the event E_nONKEY plus control nONKEY_LOCK when it reaches the selected key-press time.                                                                                                                                                                                              |
| 10         | If (after powering up from POWERDOWN mode) the debounced signal from port nONKEY is low after an asserting edge for less than the key-press time (selected by KEY_DELAY, default 2 s), an E_nONKEY event is generated at the releasing edge. If the signal is low for longer than selected by KEY_DELAY, the DA9063 asserts the event E_nONKEY plus control nONKEY_LOCK when it reaches the selected key-press time and powers down by clearing control SYSTEM_EN.                                                                                                                                                |
| 11         | If (after powering up from POWERDOWN mode) the debounced signal from port nONKEY is low after an asserting edge for less than the key-press time (selected by KEY_DELAY, default 2 s), an E_nONKEY event is generated at the releasing edge. Control SYSTEM_EN is cleared and STANDBY asserted, which triggers a partial power down from a short press. If the signal is low for longer than selected by KEY_DELAY, the DA9063 asserts the event E_nONKEY plus control nONKEY_LOCK and clear SYSTEM_EN plus STANDBY when it reaches the selected pressing time (powers down to full POWERDOWN from a long press). |

For nONKEY\_PIN settings other than '00', the wake-up is not suppressed by an asserted M\_nONKEY. With an asserted nONKEY\_LOCK, the wake-up is only executed if the debounced nONKEY signal is asserted for more than the key-press time (selected by KEY\_DELAY, default 2 s). This behaves similarly to a keypad lock since any short (unintended) pressing of nONKEY does not wake the application. If the application also has wake-up from a short nONKEY press, the host has to clear nONKEY\_LOCK before entering POWERDOWN mode. In mode '10' when nONKEY key press is longer than the time selected by KEY\_DELAY, SYSTEM\_EN is re-asserted in mode '11'. SYSTEM\_EN is re-asserted from any consecutive pressing of nONKEY. nONKEY\_LOCK is automatically cleared by the DA9063 when powering up from POWERDOWN mode. POWERDOWN mode is described in Section 6.2.2.

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### Note

During RTC/DELIVERY-MODE, the functionality of nONKEY is restricted to a termination of this mode. To enable this feature, the pull-up resistor of nONKEY has to be connected to V<sub>sys</sub>. Asserting nONKEY stops the RTC/DELIVERY-MODE and triggers a start-up of the DA9063.

### 6.1.2 Wake-up Port (CHG\_WAKE)

The CHG\_WAKE signal is a rising edge sensitive, wake-up interrupt/event intended to wake the DA9063 from an event on the companion charger (for example, supply insertion). The CHG\_WAKE port is always enabled so that the application can be powered-on with a disabled GPIO extender. The IRQ assertion and wake-up event can be suppressed via the interrupt mask M\_WAKE. During RTC/DELIVERY mode, asserting CHG\_WAKE terminates this mode.

### 6.1.3 Hardware Reset (nOFF, nSHUTDOWN, nONKEY, GPIO14, GPIO15, WATCHDOG)

The DA9063 nOFF port is an active-low input (no debouncing) typically initiated by an asserted error detection line. It asserts nSHUTDOWN in the fault register. The sequencer asserts port nRESET, and all domains and supplies of the DA9063 except LDOCORE (and possibly LDO1) are disabled in a fast emergency shutdown.

The DA9063 nSHUTDOWN port is an active-low input typically asserted from a host processor (or a push button switch). It asserts nSHUTDOWN in the fault register. The sequencer asserts port nRESET and then powers down all domains in reverse sequencer order down to slot 0 and all supplies of the DA9063 except LDOCORE (and possibly LDO1) are disabled. HOST\_SD\_MODE determines if normal power sequence timing or a fast shutdown is implemented.

The DA9063 includes a third hardware reset trigger that follows the debounced nONKEY signal after being asserted for a period greater than KEY\_DELAY + SHUT\_DELAY. The same can be achieved by a long parallel connection of GPI14 and GPI15 to ground. The long nONKEY shutdown and GPIO14/15 shutdown are enabled by the power manager control register bits nONKEY\_SD and GPI14\_15\_SD.

If the hardware reset was initiated by a (debounced) press of nONKEY (or GPIO14 and GPIO15 together) longer than SD\_DELAY, the DA9063 initially only asserts control bit KEY\_RESET in the fault register and signals a non-maskable interrupt allowing the host to clear the armed reset sequence within 1 s. If the host does not clear KEY\_RESET then a shutdown to RESET mode is executed. KEY\_SD\_MODE determines if normal power sequence timing or a fast shutdown is implemented.

The DA9063 then waits for a valid wake-up event (for example, a key press) or starts the power sequencer automatically if AUTO\_BOOT is configured.

If the WATCHDOG has been disabled, this hardware reset can be used to turn off the application in the event of a software lock-up without removing the battery. This type of reset should only be used for severe hardware or software problems as it will completely reset the processor and could result in data loss.

### 6.1.4 Reset Output (nRESET)

The nRESET signal is an active-low output signal from DA9063 to the host processor that can either be push-pull or open drain (selected via PM\_O\_TYPE), which tells the host to enter the reset state. nRESET is always asserted at the beginning of a DA9063 cold start from NO-POWER, DELIVERY, and RTC modes. It is asserted in ACTIVE mode before the DA9063 starts powering down to RESET mode (triggered from user, host, or an error condition detected by the DA9063). nRESET may also

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be asserted (depending on nRES\_MODE setting) as a soft reset before the sequencer starts powering down without progressing to RESET mode.

An assertion of nRESET from voltage supervised regulators being out-of-range can be enabled via control MON\_RES (minimum assertion time 1 ms).

After being asserted, nRESET remains low until the reset timer has been started from the selected trigger signal and expires. The reset release timer trigger signal can be selected via RESET\_EVENT to be EXT\_WAKEUP, SYS\_UP, PWR\_UP, or leaving PMIC RESET state. The expiry time can be configured via RESET\_TIMER from 1 ms to 1 s.

### 6.1.5 System Enable (SYS\_EN)

SYS\_EN is an input signal from the host processor to the DA9063 that enables the regulators in domain SYSTEM. The feature is enabled using GPIO8\_PIN and configured as active-low or -high by GPIO8\_TYPE. It asserts SYSTEM\_EN and simultaneously generates an IRQ. It also triggers a wake-up event in POWERDOWN mode if enabled via GPIO8\_WEN. De-asserting SYS\_EN (changing from active to passive state) clears control SYSTEM\_EN which triggers a power down sequence into hibernate/standby mode (without IRQ assertion or wake-up event trigger). By setting nRES\_MODE, the port SYS\_EN can be used as a soft reset input with the assertion of nRESET before powering down. With the exception of supplies that have the xxxx\_CONF control bit asserted, all regulators in power domains POWER1, POWER, and SYSTEM are sequentially disabled in reverse order. Regulators with the <x>\_CONF bit set remain on but change the active voltage control registers from V<x>\_A to V<x>\_B (if V<x>\_B is not already selected).

The control register bit SYSTEM\_EN can also be used to power down domain SYSTEM by a software command. It can be read and changed via the control interfaces and can be initialized from OTP when leaving POWERDOWN mode. The DA9063 will not process any changes on port SYS\_EN or register control SYSTEM\_EN until the sequencer has stopped processing IDs.

### 6.1.6 Power Enable (PWR\_EN)

PWR\_EN is an input signal from the host processor to the DA9063. The input signal can be configured as active-high or -low via GPIO9\_TYPE, and to trigger a wake-up event from POWERDOWN mode if configured via GPIO9\_WEN. Initialization, IRQ assertion and the direct control via register bit POWER\_EN is similar to the function of SYS\_EN in domain SYSTEM as described in Section 6.1.5. To ensure correct sequencing, SYSTEM\_EN (SYS\_EN) must be active before asserting PWR\_EN/POWER\_EN. When de-asserting PWR\_EN/POWER\_EN, the sequencer sequentially powers down POWER1 and POWER domains.

### 6.1.7 Power1 Enable (PWR1\_EN)

PWR1\_EN is an input signal from a host to the DA9063. The input signal can be configured as active-high or -low via GPIO10\_TYPE, and to trigger a wake-up event in POWERDOWN mode if enabled via GPIO10\_WEN. Initialization, IRQ assertion and the direct control via register bit POWER1\_EN is similar to the function of SYS\_EN in domain SYSTEM as described in Section 6.1.5. POWER1 is a general purpose power domain.

### 6.1.8 GP\_FB1, General Purpose Signal 1 (EXT\_WAKEUP/READY)

This port supports two different modes selected by the control PM\_FB1\_PIN.

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**Table 37: PM\_FB1\_PIN Settings**

| PM_FB1_PIN | Description                                                                                                                                                                                                                                                                                                                                         |
|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0          | EXT_WAKEUP. This output signal to the host processor indicates a valid wake-up event during POWERDOWN mode. External signals that can trigger wake-up events are debounced before the EXT_WAKEUP signal is asserted. EXT_WAKEUP is released when register control SYSTEM_EN is asserted (minimum pulse duration = 500 $\mu$ s).                     |
| 1          | READY. The READY signal indicates on-going DVC or power sequencer activities. The READY signal is asserted (typically active-low) from the DA9063 power sequencer when the processing of IDs commences, and is released when the target power state (final sequencer slot) has been reached. READY is also asserted during DVC voltage transitions. |

The active level is configured via the control GPIO13\_MODE. The logical threshold voltage is selected by GPIO13\_TYPE.

### 6.1.9 GP\_FB2, General Purpose Signal 2 (PWR\_OK/KEEP\_ACT)

The GP\_FB2 port supports two different modes selected by the control PM\_FB2\_PIN.

**Table 38: PM\_FB2\_PIN Settings**

| PM_FB2_PIN | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0          | PWR_OK. In this mode the port is a regulator status indicator. The port is an open drain output asserted if none of the selected regulators are out-of-range. The regulator monitoring via ADC must be enabled and all regulators to be monitored must have supervision enabled with the selected persistence, and mask bit M_REG_UVOV must be asserted. In case at least one of the supervised regulators is out-of-range or regulator monitoring is disabled, the PWR_OK signal is low. |
| 1          | KEEP_ACT. If enabled, every assertion of the port (rising to active level edge sensitive) sets the watchdog trigger, similar to writing to bit WATCHDOG via the power manager bus. The host has to release KEEP_ACT before the next assertion during continuous watchdog supervision (if enabled). The minimum assertion and de-assertion cycle time is 150 $\mu$ s.                                                                                                                      |

The output active level (and driver type) can be configured via GP\_FB2\_TYPE.

Alternatively, with BCORE\_MERGE = 1, FB in register BCORE1\_CFG set to 0b000 and MERGE\_SENSE = 0, the GP\_FB2 pin becomes a voltage feedback signal for BUCKCORE.

### 6.1.10 GP\_FB3, General Purpose Signal 3 (OUT32K\_2/nVIB\_BRAKE)

The GP\_FB3 port supports two different modes selected by the control PM\_FB3\_PIN.

**Table 39: PM\_FB3\_PIN Settings**

| PM_FB3_PIN | Description                                                                                                                                                                                                                                                                                                                                       |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0          | OUT32K_2. This provides a second 32K signal output (push-pull).                                                                                                                                                                                                                                                                                   |
| 1          | nVIB_BRAKE. If LDO8 is configured as a vibrator motor driver, GP_FB3 can be configured to provide an external brake signal. The vibrator motor can be started or stopped by a change in the level on the nVIB_BRAKE signal. If the port is not used as a brake command, the vibration motor runs continuously at the speed configured by VIB_SET. |

GP\_FB3\_TYPE defines the active level.

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### 6.1.11 Supply Rail Fault (nVDD\_FAULT)

nVDD\_FAULT gives the status of the system supply monitoring, see Section 6.18. The assertion of nVDD\_FAULT indicates that the main supply input voltage has been low ( $V_{SYS} < V_{DD\_FAULT\_LOWER}$ ) for more than 100 ms and informs the host processor that the power will shut down. It can be configured to drive a GPO from the GPIO<x>\_OUT controls. The driver type (push-pull, open-drain) selection and pull-up resistor control function normally. The GPIO<x>\_MODE can be used to invert the incoming nVDD\_FAULT signal.

The nVDD\_FAULT port can alternatively be controlled by the state of the debounced  $V_{SYS}$  monitor inside the ADC (selected via GPIO12\_PIN). The signal is asserted when the ADC detects three consecutive results below the configurable threshold VSYS\_MON (it becomes passive after three consecutive results above VSYS\_MON). This provides a variable power good signal to trigger boot activities on external ICs.

The active level/debounce, wake-up, and IO supply voltage can be selected via the controls GPIO12\_MODE, GPIO12\_WEN and GPIO12\_TYPE, respectively.

### 6.1.12 Interrupt Request (nIRQ)

The nIRQ is an output signal that can either be push-pull or open drain (selected via PM\_O\_TYPE). If an active high IRQ signal is required, it can be achieved by asserting control IRQ\_TYPE (recommended for push-pull mode). This port indicates that an interrupt-causing event has occurred and that event/status information is available in the EVENT and STATUS registers. Events are triggered by a status change at the monitored signals. When an event bit is set, the nIRQ signal is asserted (unless this interrupt is masked by a bit in the IRQ mask register). The nIRQ is not released until all event registers with asserted bits have been read and cleared. New events that occur during reading an event register are held until the event register is cleared, ensuring that the host processor does not miss them. The same happens to all events occurring while the sequencer processes time slots (that is, the generation of interrupts is delayed).

### 6.1.13 Real Time Clock Output (OUT\_32K)

OUT\_32K is a buffered output of the DA9063 32 kHz oscillator. If enabled via CRYSTAL, the 32 kHz oscillator always runs on the DA9063 following the initial start-up from NO-POWER or DELIVERY mode until the device has reached NO-POWER (or DELIVERY) mode again. The signal output buffer can be disabled manually via EN\_32KOUT and paused during POWERDOWN mode by setting OUT32K\_PAUSE. The 32K signal can additionally be made available at port GP\_FB3.

### 6.1.14 IO Supply Voltage (VDD\_IO1 and VDD\_IO2)

VDD\_IO1 and VDD\_IO2 are two independent IO supply rail inputs of the DA9063 that can be individually assigned to the power manager interfaces (see control bit GPI\_V), power manager IOs (see control bits PM\_O\_V, PM\_I\_V) and GPIOs (bits GPIOx\_TYPE). The rail assignment determines the IO voltage levels and logical thresholds, see Section 5.4. The selection of the supply rail for GPIOs is also partially used for their alternate functions, see Table 1 and Table 2. As an example, GPIO13\_TYPE determines the supply rail when this pin is configured as the GP\_FB1 output.

#### Note

Maximum speed at 4-WIRE interface is only available if the selected supply rail is greater than 1.6 V, see Table 44.

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### 6.2 Operating Modes

#### 6.2.1 ACTIVE Mode

A running application is typically in ACTIVE mode. The DA9063 transitions to ACTIVE mode after the host processor performs at least one initial 'alive' watchdog write (or alternatively an initial assertion of the KEEP\_ACT port) inside the target time window. If the WATCHDOG function is disabled by setting TWDSSCALE to zero, the DA9063 transitions to ACTIVE mode when all of the sequencer IDs in the POWER domain are complete.

In ACTIVE mode, the PMIC core functions as LDOCORE, calendar counter and internal oscillator are running. Typically additional features are enabled, such as the GPADC. The DA9063 can send interrupt requests to the host via a dedicated interrupt port (nIRQ) and status information can be read from the host processor via the power manager interface. Temperature and voltages inside and outside the DA9063 can be monitored and fault conditions can be flagged to the host processor.

#### 6.2.2 POWERDOWN Mode

The DA9063 is in POWERDOWN mode when the power domain SYSTEM is disabled (even partially). This can be achieved when progressing from NO-POWER/DELIVERY/RTC mode or by returning from ACTIVE mode. A return from ACTIVE mode is initiated by low power mode instructions from the host (for example, releasing signal SYS\_EN or clearing register bit SYSTEM\_EN), from the user by asserting nONKEY (if nONKEY\_PIN='1x') or as an interim state during a shutdown to RESET mode.

During POWERDOWN mode LDOCORE, VREF reference voltage, the nONKEY pin, CHG\_WAKE port, and the calendar counter are active. Dedicated power supplies can be kept enabled during POWERDOWN mode if their xxx\_CONF bits are asserted (supply voltage settings are taken from the respective Vxxx\_B registers).

GPIO ports, the GPADC, and the control interfaces also remain active in POWERDOWN mode if not configured otherwise via register PD\_DIS. Disabling these blocks during POWERDOWN mode reduces quiescent current, especially if all blocks that require an oscillator clock are disabled (CLDR\_PAUSE, HS2WIRE\_DIS, PMIF\_DIS, GPADC\_PAUSE, GPI\_DIS, PMCONT\_DIS). If required, the application supervision by the WATCHDOG timer can be continued in POWERDOWN mode via WATCHDOG\_PD. If the host will not communicate with the DA9063 during POWERDOWN mode, then the control interfaces may also be temporarily disabled (see controls PMIF\_DIS/HS2WIRE\_DIS).

If the sequencer pointer has stopped at position PART\_DOWN (inside domain SYSTEM) it results in a partial power down. When on the way down the sequencer pointer reaches position 0, relevant regulators/rail switches with corresponding position 0 IDs that have cleared control Bxxx\_CONF/LDOxx\_CONF/xxx\_SW\_CONF are disabled, otherwise the regulator voltages change to the values defined in VBxxx\_B/VLDOxx\_B when control DEF\_SUPPLY is asserted. When DEF\_SUPPLY is released, slot 0 is not processed by the sequencer, hence regulators/rail switches with an ID pointing to slot 0 remain unchanged. Following the next wake-up event Vxxx\_A voltage levels and the sequencer power domain controls/timers are set to their default OTP values if OTPREAD\_EN is asserted.

Position 0 also allows an automatic transition into a dedicated RTC mode, where all features of the DA9063 (including LDOCORE) are disabled except for the RTC oscillator and calendar. This mode is armed via control RTC\_MODE\_PD and terminated by an RTC alarm/tick asserting nONKEY/CHG\_WAKE, or if VDDREF rises above 2.6 V, this automatically re-enables LDOCORE and the full-power manager logic.

If POWERDOWN mode is reached in response to a long nONKEY press, RTC mode is not entered until the key is released. When nONKEY\_SD is asserted and the key is continuously pressed for

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longer than the time selected by KEY\_DELAY + SHUT\_DELAY, it asserts KEY\_RESET to indicate that the transition to RESET mode was triggered by a long nONKEY, see Section 6.1.1.

When the device is in POWERDOWN or RESET mode, asserting ECO\_MODE enables low power. This is achieved internally by using a pulsed mode for VDDCORE and reference voltage generation. This maintains basic functionality but full parametric compliance is no longer guaranteed (as it affects ADC precision, buck performance, LDO voltage resolution, and so on). When the DA9063 is connected to a 32 kHz crystal (and enabled via control CRYSTAL), the pulsed mode timing is generated from this source. Otherwise the pulsed mode is driven from a (free-running) low-power on-chip oscillator.

### 6.2.3 RESET Mode

The DA9063 is in RESET mode when a complete application shutdown is required. The RESET mode can be triggered by the user, a host processor or by an action on the DA9063, as outlined below:

- By the user:
  - from a long press of nONKEY (interruptible by host)
  - from a long parallel assertion of GPIO14 and GPIO15 (interruptible by host)
- By pressing a reset switch connected to port nSHUTDOWN (non-interruptible)
- Forced from the host processor (non-interruptible) by:
  - asserting port nSHUTDOWN (falling edge)
  - writing to register bit SHUTDOWN
- By an error condition that forces a RESET mode (non-interruptible):
  - no WATCHDOG write (KEEP\_ACT signal assertion) from the host inside the watchdog time window (if watchdog was enabled)
  - an under-voltage detected at V<sub>sys</sub> (V<sub>sys</sub> < VDD\_FAULT\_LOWER)
  - an internal die over-temperature
- Forced by the error detection line (non-interruptible):
  - by asserting port nOFF (falling edge)

The controls INT\_SD\_MODE, HOST\_SD\_MODE, and KEY\_SD\_MODE can be used to individually configure the shutdown sequences from an internal fault, host or user trigger. In each case, the sequence can be configured to implement either the reverse timing of the power-up sequence or an immediate transition into RESET mode, skipping any delay from the sequencer or dummy slot timers. Asserting nOFF always triggers a fast emergency shutdown. To allow the host to determine the reason for the reset, the source is recorded in FAULT\_LOG (as either the KEY\_RESET or nSHUT\_DOWN bit). The host processor clears FAULT\_LOG by writing asserted bits with a 1.

#### Note

- KEY\_SD\_MODE = 1 enables a full POR following a long press of ONKEY or a long assertion of GPIO14 and 15.
- In the case of an aborted OTP read, the DA9063 enters RESET mode without asserting any bits in FAULT\_LOG.

A shutdown to RESET mode begins with the DA9063 asserting the nRESET port. Then domain SYSTEM is completely powered down (sequencer position 0) at which time the device has reached RESET mode: this is a low current consumption state. The only circuits in RESET mode remaining active are LDOCORE (at a reduced level of 2.2 V), the control interfaces and GPIOs, the calendar counter, the VREF reference, and the comparators for over-temperature and V<sub>sys</sub> level. Except for LDO1 and the backup battery charger, other regulators and blocks are automatically disabled to

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avoid draining the battery. During the DA9063 RESET mode, the host processor can be held in a RESET state via port nRESET.

When entering RESET mode, all user and system events are cleared. When leaving RESET mode, the complete DA9063 register configuration is reloaded from OTP (with the exception of AUTO\_BOOT in case of a VDD\_START fault).

### Note

FAULT\_LOG, GP\_ID\_10 to GP\_ID\_19 and other non-OTP loaded registers (for example, RTC calendar and alarm) remain unchanged when leaving RESET mode.

nRESET is always asserted low after a cold start from NO-POWER, RTC, or DELIVERY mode and can also be asserted (depending on configuration of nRES\_MODE) before the sequencer starts to power down towards POWERDOWN mode.

Some reset conditions such as shutdown via register write, watchdog error, or over-temperature automatically expire (that is, are automatically cleared by the device as it shuts down). Other RESET triggers such as via port nOFF or nSHUTDOWN need to be released before the DA9063 can move from RESET to POWERDOWN mode. In the case that the application requires regulators to discharge in advance of a consecutive power-up sequence, a minimum duration of the RESET mode can be selected via RESET\_DUR.

If the reset was initiated by user action from a long nONKEY key-press (or GPI14 and GPI15), bit KEY\_RESET is set and the nIRQ port asserted. After 1 s the shutdown sequence is started, unless this is inhibited by the host clearing KEY\_RESET within this 1 s period (by writing a 1 to the related bit in register FAULT\_LOG). When the RESET condition has been removed, the DA9063 requires the presence of a good supply ( $V_{SYS} > VDD\_FAULT\_UPPER$  and able to provide enough power) before it can start-up again and move into POWERDOWN mode.

RESET mode is also used during an automatic transition by the device into RTC mode, as described in Section 6.2.4.

### 6.2.4 RTC Mode

The RTC mode is an ultra-low power mode intended to maintain only the application's system time inside the RTC block. It can be armed by asserting control RTC\_EN from OTP or host register write. With RTC\_MODE\_PD enabled, the device enters RTC mode when the power sequencer reaches slot 0 in a power down sequence. All regulators (including LDOCORE) and most features on the DA9063 are disabled. Only the FAULT\_LOG register, calendar counter, and their related registers (including the alarms) are maintained. With RTC\_EN = 1, the DA9063 automatically enters RTC mode when a VDD\_FAULT condition is present, when RTC\_MODE\_SD is asserted, or when  $V_{DDREF}$  drops below the POR threshold.

RTC mode is automatically terminated when asserting nONKEY or CHG\_WAKE, or from an RTC tick/alarm. The same occurs when  $V_{DDREF}$  has risen above 2.6 V (for example, from insertion of an external supply or a pre-charged battery). LDOCORE is then switched on and a start-up sequence is triggered.

### 6.2.5 DELIVERY Mode

The DELIVERY mode provides the lowest possible quiescent current, allowing connected pre-charged batteries (backup or main battery) to maintain charge prior to the end-user starting the device for the first time. It is armed by setting RTC\_EN = 0 and then entered by the same conditions as RTC mode. During DELIVERY mode, only the nONKEY, CHG\_WAKE, and the  $V_{DDREF}$  detection circuitry is enabled. Connecting only a backup battery results in DELIVERY mode.

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### 6.2.6 NO-POWER Mode

In the absence of a (charged) backup battery, the DA9063 enters NO-POWER mode when VDDCORE drops below the VPOR\_LOWER threshold. As long as VDDCORE stays below the VPOR\_UPPER threshold, an internal power-on-reset (nPOR) signal remains asserted. In this mode, only the VDDCORE threshold comparator is active. This comparator simply checks for a condition that allows the DA9063 to turn on again. When a good supply is subsequently available again on V<sub>DDREF</sub> (> 2.4 V), VDDCORE is able to rise above VPOR\_UPPER and the DA9063 leaves NO-POWER mode.

### 6.2.7 Power Commander Mode

This is a special mode for evaluation and configuration development. In Power Commander mode, the DA9063 is configured to load the control register default values from the HS 2-WIRE interface, instead of from the OTP cells, so that un-programmed DA9063 samples will power up, allowing evaluation and verification of a proposed user configuration.

Power Commander mode is enabled by connecting TP to a 3.3 V to 5.0 V voltage.

#### Note

In Power Commander mode, GPI14 and 15 are configured for HS-2-WIRE interface operation (with VDDCORE as the supply) and GPO12 is configured as an output for nVDD\_FAULT. Any register writes or OTP loads which can change this configuration are ignored until DA9063 has exited from Power Commander mode.

After leaving the POR state, the DA9063 informs the system that it is waiting for a programming sequence by driving nVDD\_FAULT low. The software running on the PC monitors nVDD\_FAULT and responds by downloading the values into the configuration registers within DA9063. nVDD\_FAULT is automatically released after the download is complete.

There are two programming sequences performed in Power Commander mode. The first takes place between RESET and POWERDOWN mode and the second between POWERDOWN and SYSTEM mode.

#### Note

To correctly configure DA9063, addresses 0x0A to 0x36, 0x82 to 0xCF, and 0x104 to 0x12E should be programmed during the first sequence. Registers 0x0E, 0x82, and 0xA3 to 0xB3 should be programmed during the second sequence.

When the first programming sequence is complete, DA9063 will be in POWERDOWN mode. Progression from this mode is determined by the values programmed for SYS\_EN and AUTO\_BOOT. If DA9063 has been directed to progress from POWERDOWN mode then it drives pin nVDD\_FAULT low for a second time to request that the SW performs the second programming sequence.

Once the second programming sequence is complete, the progress of the power-up sequence is controlled by the values loaded during the programming sequence.

The programmed configuration can be identified by reading the fuse register CONFIG\_ID.

#### Note

During Power Commander mode, the fault detection status bit VDD\_FAULT and the level at the related pin nVDD-FAULT do not match and do not indicate a low voltage level at VDDOUT. An enabled shutdown from a 5 s assertion of GPIO14/15 will be ignored during POWER Commander mode. Any nIRQ and event assertion when accessing the HS 2-WIRE interface (E\_GPI14) is suppressed in this mode.

## System PMIC for Mobile and Automotive Applications

### 6.3 Start-Up from NO-POWER Mode

#### 6.3.1 Power-On-Reset (nPOR)

The DA9063 generates an internal power-on-reset nPOR (active low) following the initial connection of a supply to  $V_{DDREF}$ .

While the  $V_{DDCORE}$  voltage is below the threshold  $V_{POR\_UPPER}$ , the internal signal nPOR is driven low and the DA9063 will not start-up. This is NO-POWER mode. When the  $V_{DDCORE}$  voltage rises above  $V_{POR\_UPPER}$ , the following occur:

- The nPOR is driven high (flagged by the POR bit being set in register `FAULT_LOG`).
- The oscillator is enabled.
- The VREF reference is enabled.
- The complete OTP block is read and stored in the register bank.
- The DA9063 progresses into POWERDOWN mode.

From POWERDOWN mode, the DA9063 continues through the power-up sequence if either:

- the power domain SYSTEM was enabled by the input port, `SYS_EN`, or,
- the power domain SYSTEM was enabled in OTP settings and `AUTO_BOOT` was enabled.

With `AUTO_BOOT` disabled and the power domain SYSTEM enabled in OTP settings, a non-suppressed wake-up event allows the DA9063 to continue through the power-up sequence.

### 6.4 Exiting Reset Mode and Application Wake-up

Application startup requires a sufficient  $V_{SYS}$  supply, as determined by the `VDD_START` feature, and a wake-up event.

#### 6.4.1 VDD\_START

The DA9063 `VDD_START` feature prevents endless looping of false starts in a weakly-powered system. `VDD_START` limits the number of automatic restart attempts to three. With reference to Figure 14:

- Figure 14(a): The PMIC starts from NO-POWER mode.
- Figure 14(b): First startup attempt. The PMIC transitions to the ACTIVE state when  $V_{SYS}$  rises above  $V_{DD\_FAULT\_UPPER}$ .
- Figure 14(c): If, during the first startup attempt, the  $V_{SYS}$  supply drops below  $V_{DD\_FAULT\_LOWER}$  for more than 100 ms, the PMIC shuts down to the SHUTDOWN state.  $V_{DD\_FAULT\_UPPER}$  is increased automatically by 250 mV. However, the increased  $V_{DD\_FAULT\_UPPER}$  is limited to a maximum of 3.70 V.
- Figure 14(d): Second startup attempt. If  $V_{SYS}$  rises above the new  $V_{DD\_FAULT\_UPPER}$  threshold, then the PMIC will power-up to the ACTIVE state.
- Figure 14(e): If, during the second startup attempt, the  $V_{SYS}$  supply drops below  $V_{DD\_FAULT\_LOWER}$  for more than 100 ms, the PMIC shuts down to the SHUTDOWN state.  $V_{DD\_FAULT\_UPPER}$  is increased automatically by a further 250 mV (500 mV above its original setting). However, the increased  $V_{DD\_FAULT\_UPPER}$  is limited to a maximum of 3.70 V.
- Figure 14(f): Third startup attempt. If  $V_{SYS}$  rises above the new  $V_{DD\_FAULT\_UPPER}$  threshold, then the PMIC will power-up to the ACTIVE state.

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- Figure 14(g): If, during the third startup attempt, the  $V_{SYS}$  supply drops below  $V_{DD\_FAULT\_LOWER}$  for more than 100 ms, the PMIC shuts down. From then on, `AUTO_BOOT` and wake-up from non-user events are temporarily disabled. 'User events' are defined in Table 40.

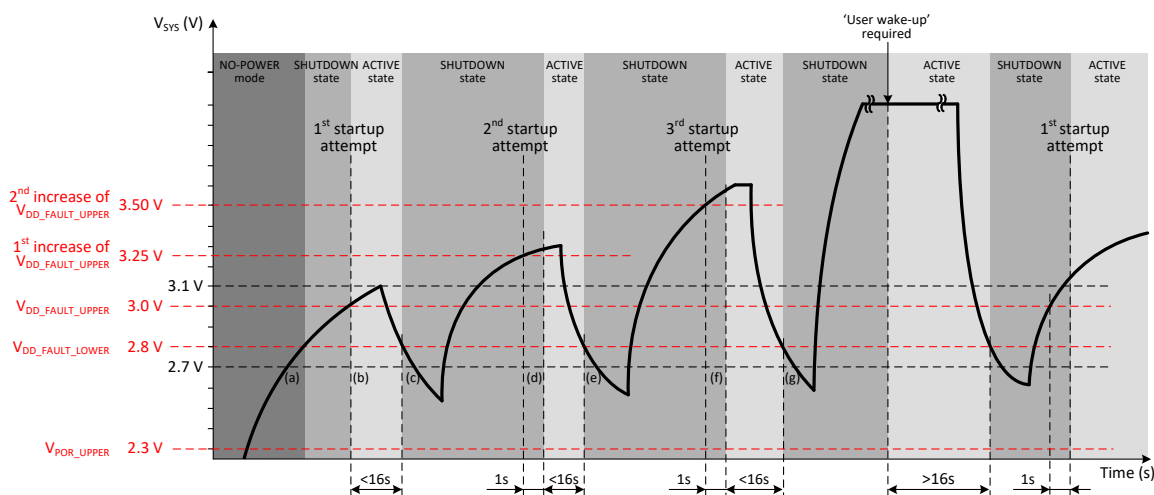


Figure 14: VDD\_START Faults

### NOTE

- During an attempt to restart, the entry into the ACTIVE state is delayed by 1 s.
- The ACTIVE state also includes POWER1 mode. The PMIC has the same VDD\_START behavior from the POWERDOWN and SYSTEM modes as from the ACTIVE state.
- `AUTO_BOOT` and wake-up from non-user events are re-enabled after the application has successfully powered up to the ACTIVE state for more than 16 s. This also resets the start-up threshold to  $V_{DD\_FAULT\_UPPER} + 0$  mV.

Until the host has been booted, an OTP-enabled flashing LED may be driven from GPIO11, 14, or 15 to indicate to the user that the device is supplied with (insufficient) power. When `CHG_WAKE` is connected to a charger, the VDD\_START-triggered LED flashing continues as long as an external supply is charging the battery. The flashing LED can be configured via controls `RESET_BLINKING`, `BLINK_DUR`, and `BLINK_FRQ`. After the application is running, the blinking LED can be stopped via a host register write.

### 6.4.2 Wake-Up Events

DA9063 offers two types of wake-up event, user events and system events (see Table 40). Non-suppressed user events (for example, `NONKEY`, `CHG_WAKE` or from GPIOs) are always processed and trigger a wake-up.

Wake-up events can be individually suppressed by setting the related `nIRQ` mask bit. When `NONKEY_LOCK` is asserted a wake-up requires the debounced signal from `NONKEY` to be low for a time longer than the configured `KEY_DELAY`. It is not recommended to mask system events, instead disable the unwanted event sources (for example, GPIOs, GPADC, 1.2 V comparator). The wake-up from GPIOs (or selected alternate features that use a shared GPI event) has to be enabled via `GPI<x>_WEN`.

After a valid wake-up condition is detected, a subset of the OTP configuration is read and the values are used to reconfigure the regulator voltage registers  $V_{xxx\_A}$ , the power domain enable settings (if not suppressed via `SYSTEM_EN_RD`) and the sequencer timer.

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DA9063 then asserts the EXT\_WAKEUP signal towards the host processors and configures regulators with an ID pointing at slot 0 to their target state. If the power domains are not pre-enabled from OTP settings, the host processor must control further application start-up (via the power domain enable ports, SYS\_EN, PWR\_EN and PWR1\_EN). Alternatively the DA9063 continues powering-up the OTP-enabled domains via the power domain sequencer, but the power sequencer will not start to enable the system supplies unless SYSTEM\_EN is asserted.

Progression to ACTIVE mode requires assertion of POWER\_EN from the host via port PWR\_EN, a register write, or enabled in OTP. After starting the WATCHDOG timer the host processor must assert the WATCHDOG bit within the configured time window. If this does not happen, the state-machine terminates ACTIVE mode and returns to RESET mode.

**Table 40: Wake-up Events**

| Signal : Event                                                               | Wake-up | User Event | System Event | IRQ |
|------------------------------------------------------------------------------|---------|------------|--------------|-----|
| V <sub>sys</sub> monitor : E_VDD_MON                                         | X       |            | X            | X   |
| VDD_FAULT pre-warning : E_VDD_WARN                                           | X       |            | X            | X   |
| RTC alarm : E_ALARM                                                          | X       |            | X            | X   |
| RTC periodic tick : E_TICK                                                   | X       |            | X            | X   |
| Voltage comparator flipped : E_COMP1V2                                       | X       |            | X            | X   |
| Pressed On key : E_nONKEY                                                    | X       | X          |              | X   |
| Wake-up from companion charger : E_WAKE                                      | X       | X          |              | X   |
| LDO over current detect : E_LDO_LIM                                          | X       |            | X            | X   |
| Regulator voltage out-of-range : E_REG_UVOV                                  | X       |            | X            | X   |
| Critical junction temperature : E_TEMP                                       | X       |            | X            | X   |
| Power sequencing ready : E_SEQ_RDY                                           |         |            | X            | X   |
| Voltage ramping ready : E_DVC_RDY                                            |         |            | X            | X   |
| Manual ADC result ready : E_ADC_RDY                                          |         |            | X            | X   |
| GPIOs passive to active transition : E_GPIx                                  | X       | X          |              | X   |
| ADC 1, 2, 3 threshold : via GPIO, 1, 2                                       | X       |            | X            | X   |
| SYS_EN, PWR_EN, PWR1_EN (passive to active transition)<br>: via GPIO8, 9, 10 | X       |            | X            | X   |
| HS-2-WIRE interface : via GPIO14                                             | X       |            | X            | X   |

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### 6.5 Power Supply Sequencer

The DA9063 power supplies are enabled with a sequencer that contains a programmable step timer, a programmable ID array of slot pointers, and four predefined pointers (SYSTEM\_END, POWER\_END, MAX\_COUNT, and PART\_DOWN), as illustrated by Figure 15. The sequencer is able to control up to 32 IDs (six bucks, 11 LDOs, 7 external FET/IC controls, a Wait ID (GPI10), an EN\_32K enable, and an ID to activate power down settings), which can be grouped to three power domains.

The power domains have configurable size and their borders are described by the location pointers SYSTEM\_END, POWER\_END, and MAX\_COUNT.

The lowest level power domain SYSTEM starts at step 1 and ends at the step that is described by the location pointer SYSTEM\_END. The second level domain POWER starts at the successive step and ends at POWER\_END. The third level domain POWER1 starts at the consecutive step and ends at MAX\_COUNT. The values of pointer SYSTEM\_END, POWER\_END, and MAX\_COUNT are predefined in OTP registers and should be configured as SYSTEM\_END < POWER\_END < MAX\_COUNT.

The domain system can be thought of as the minimum set of supplies required to enable the core of the target system.

If the control OTPREAD\_EN is enabled, the regulator voltages, sequence domain enables (if not suppressed via control SYSTEM\_EN\_RD), and the sequence timer are reset to their OTP values during the transition from power down to system.

The second level domain POWER includes supplies that are required on top to trigger the application and set the DA9063 into ACTIVE mode. POWER1 can be understood as one of the POWER domains that can be used for further sequenced control of supply blocks during ACTIVE mode (for example, for a sub-application like WLAN or a baseband chipset).

| Note                                                                                              |
|---------------------------------------------------------------------------------------------------|
| It is recommended that the system is configured to reach ACTIVE mode before running applications. |

#### 6.5.1 Powering Up

All buck converters and 11 LDOs of DA9063 have a unique sequencer ID. The power-up sequence is defined by an OTP register bank that contains a series of supplies (and other features), each of which point to a selected sequencer time slot. Several supplies can point to the same time slot which is therefore enabled in parallel by the sequencer. Time slots that have no IDs pointing at them are dummy steps that do nothing but insert a configurable time delay (marked in Figure 15 as D). Supplies/IDs that do not point to a sequencer time slot between 1 and MAX\_COUNT are not enabled by the power sequencer but can be controlled individually by the host (via the power manager interface).

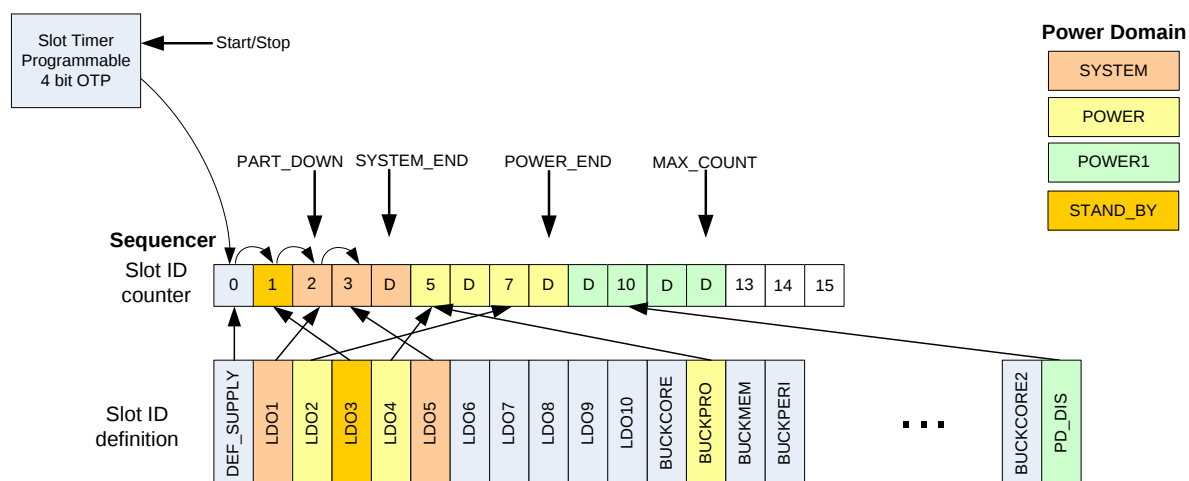
During power-up, the sequencer starts at slot 0. If DEF\_SUPPLY is asserted, it checks all regulators/rail switches for an ID pointing to slot 0. Cleared LDOxx\_AUTO/BUCKxxx\_AUTO/xxx\_SW\_AUTO bits are configured by setting the related control Bxxx\_CONF/LDOxx\_CONF/xxx\_SW\_CONF, otherwise the regulator is enabled. To minimize inrush currents, it is recommended to enable no more than a single default regulator via DEF\_SUPPLY. During power-up, the regulator output voltage is taken from the VBxxx\_A/VLDOxx\_A registers. During power-down, regulators/rail switches with a cleared control in Bxxx\_CONF/LDOxx\_CONF/xxx\_SW\_CONF are disabled, otherwise the regulator voltage is changed to VBxxx\_B/VLDOxx\_B when entering slot 0. When DEF\_SUPPLY is released, slot 0 is not processed by the sequencer (regulators/rail switches with an ID pointing at slot 0 remain unchanged).

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The progression of the sequencer to slot 1 is dependent on certain conditions:

- If **AUTO\_BOOT** and **SYSTEM\_EN** are both asserted (via port, by register write or in OTP), the sequencer asserts the **READY** signal (if **GP\_FB1** is so configured) and then continues by processing slot 1.
- If **AUTO\_BOOT** is not asserted, the sequencer remains in a holding start state, waiting for either:
  - the assertion of **SYSTEM\_EN**, or,
  - any other wake-up event if **SYSTEM\_EN** is already enabled.

All supplies (and other sequenced features) that are pointing at slot 1 are then processed. This is similar to the processing of slot 0 with the exception that **DEF\_SUPPLY** has no effect on slots apart from slot 0. From slot 1, the sequencer progresses until it reaches the position of pointer **SYSTEM\_END**. At this point, all IDs of the first power domain **SYSTEM** are enabled and, if **POWER\_EN** is not asserted, the DA9063 releases the **READY** signal (in combination with optional assertion of **E\_SEQ\_RDY**).



**Figure 15: Assignment of Actions to Sequencer Slot IDs**

**Table 41: Power Sequencer Controlled Actions**

| Action        | Sequencer Time Slot |
|---------------|---------------------|
| Control LDO1  | LDO1_STEP           |
| Control LDO2  | LDO2_STEP           |
| Control LDO3  | LDO3_STEP           |
| Control LDO4  | LDO4_STEP           |
| Control LDO5  | LDO5_STEP           |
| Control LDO6  | LDO6_STEP           |
| Control LDO7  | LDO7_STEP           |
| Control LDO8  | LDO8_STEP           |
| Control LDO9  | LDO9_STEP           |
| Control LDO10 | LDO10_STEP          |
| Control LDO11 | LDO11_STEP          |

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| Action                            | Sequencer Time Slot |
|-----------------------------------|---------------------|
| Control BUCKCORE1                 | BUCKCORE1_STEP      |
| Control BUCKCORE2                 | BUCKCORE2_STEP      |
| Control BUCKPRO                   | BUCKPRO_STEP        |
| Control BUCKIO                    | BUCK_IO_STEP        |
| Control BUCKMEM                   | BUCKMEM_STEP        |
| Control BUCKPERI                  | BUCKPERI_STEP       |
| Control CORE_SW                   | CORE_SW_STEP        |
| Control PERI_SW                   | BUCKPERI_STEP       |
| Assert/Release GPIO2              | GP_RISE1_STEP       |
| Release/Assert GPIO2              | GP_FALL1_STEP       |
| Assert/Release GPIO7              | GP_RISE2_STEP       |
| Release/Assert GPIO7              | GP_FALL2_STEP       |
| Assert/Release GPIO8              | GP_RISE3_STEP       |
| Release/Assert GPIO8              | GP_FALL3_STEP       |
| Assert/Release GPIO9              | GP_RISE4_STEP       |
| Release/Assert GPIO9              | GP_FALL4_STEP       |
| Assert/Release GPIO11             | GP_RISE5_STEP       |
| Release/Assert GPIO11             | GP_FALL5_STEP       |
| Wait for active state at GPI 10   | WAIT_STEP           |
| Wait for stable oscillator signal | EN32K_STEP          |
| PD_DIS                            | PD_DIS_STEP         |

On completion of domain SYSTEM, the sequencer waits for POWER\_EN to be asserted (via the PWR\_EN port, a register write or in OTP). When POWER\_EN is asserted, the signal READY is asserted (if not already asserted) and regulators/IDs of domain POWER are enabled sequentially. The sequencer stops at the position of pointer POWER\_END. At this point it also: releases the READY signal (if POWER1\_EN is not asserted); optionally asserts E\_SEQ\_RDY; enables the initial WATCHDOG timer and waits for the first associated alive feedback from the host processor. After this, the start-up of the DA9063 progresses into ACTIVE mode.

A third power domain, POWER1, can be enabled via POWER1\_EN (asserted by PWR1\_EN port, register write or in OTP). It enables all consecutive IDs until the position of pointer MAX\_COUNT has been reached. The READY signal is asserted as long as IDs are processed (if enabled) and E\_SEQ\_RDY is asserted when reaching MAX\_COUNT.

On start-up, and if OUT\_CLOCK is asserted, the sequencer waits at a slot containing ID EN32K\_STEP until the 32 kHz clock stabilizes, see Section 6.14.1.1.

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### 6.5.2 Power-Up Timing

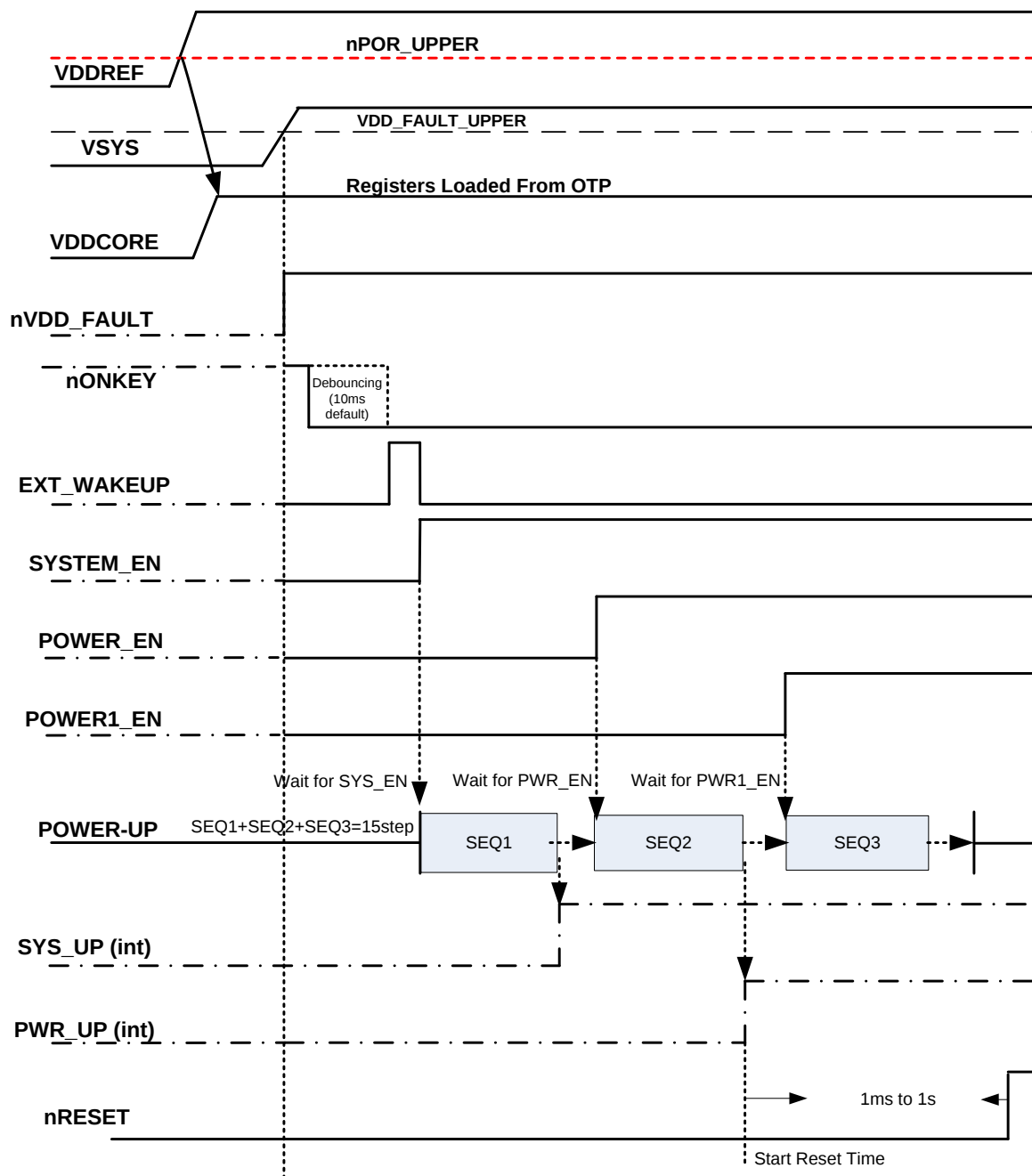


Figure 16: Power-Up Timing

### 6.5.3 Programmable Slot Delays

The delay between the slots of a sequence is controlled via the programmable value of **SEQ\_TIME** in register **SEQ\_TIMER**. This has a default delay of 128  $\mu\text{s}$  per slot (min. 32  $\mu\text{s}$ , max. 8 ms). The delay time between individual supplies can be extended by leaving a consecutive slot(s) with no IDs

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pointing to it: these are dummy slots. The dummy slots have an independent delay configured by SEQ\_DUMMY. These delay times, in register SEQ\_TIMER, are (re-)loaded from OTP every time domain SYSTEM begins to power-up.

### 6.5.4 Powering Down

When the DA9063 is powering down, the sequencer disables the supplies in reverse order and timing, asserts READY during sequencing, and triggers E\_SEQ\_RDY on reaching the target sequencer slot. Supplies that are configured to stay on (LDO<x>\_CONF, B<x>\_CONF, xxx\_SW\_CONF bit is set) are not disabled and are configured with the voltage setting from register VB<x>\_B/VLDO<x>\_B when the related time slot/ID is processed. The state of the regulators that are enabled for GPI control will not be changed by the sequencer when processing the related ID. This also applies for the selection of the related V<x>\_A or V<x>\_B voltage control register in case a regulator is enabled for GPI voltage selection.

If powering down is initiated by clearing POWER1\_EN, the sequencer stops controlling IDs before the domain pointer POWER\_END is reached. If POWER\_EN is cleared, the domain POWER1 is powered down followed by POWER before the sequencer reaches pointer SYSTEM\_END. These modes are used to temporarily disable optional features of a running application for reduced power (sleep mode).

If SYSTEM\_EN is cleared the sequencer processes all IDs lower than the pointer position down to slot 0. The sequencer can be forced to stop the intended power down sequence prior to maturity at pointer position PART\_DOWN via an asserted control STANDBY (PART\_DOWN has to point into domain SYSTEM). In these cases the power sequencer has reached the application's POWERDOWN mode (hibernate/standby), which enables the option to reset regulator settings for the consecutive power-up sequence from OTP (enabled by OTPREAD\_EN).

Wake-up events are enabled when the sequencer reaches slot 0 or pointer PART\_DOWN (ignored outside of POWERDOWN mode). The assertion of nIRQ from events during POWERDOWN mode may be delayed until ACTIVE mode is reached the next time if configured by nIRQ\_MODE. During processing slot 0, all supplies pointing into this step with a cleared control Bxxx\_CONF/LDOxx\_CONF/xxx\_SW\_CONF are disabled, otherwise the regulator voltage is changed to VBxxx\_B/VLDOxx\_B (if bit DEF\_SUPPLY is asserted). Asserting control register bit SHUTDOWN first powers down to slot 0 and then forces the DA9063 into RESET mode. Autonomous features such as the 32K output buffer or the Auto-ADC measurement can be disabled temporarily for POWERDOWN mode via register PD\_DIS. The timing for processing PD\_DIS can be defined by selecting a step inside the sequence. Features asserted in PD\_DIS are (re-)enabled when PD\_DIS is processed during a power-up sequence.

Control nRES\_MODE enables the assertion of nRESET before executing a power-down sequence and starting the reset timer during the consecutive powering up. This is also true for partial POWERDOWN mode, when the sequencer powers down to pointer position PART\_DOWN. The reset timer starts to run from the selected RESET\_EVENT and releases the nRESET port after the reset timer expires.

### 6.5.5 User Programmable Delay

A conditional mode transition can be achieved using ID WAIT\_STEP. If pointing into the power sequence the progress of an initiated mode transition can be synchronized, for example with the state of a host. This is indicated by toggling the signal at GPI10 to its configured active state. To begin the wait step, the event bit E\_GPI10 must be clear. This is the typical case for a system cold boot. The wait is terminated when an event is detected by the PMIC on GPI10. To use this feature during a warm boot, such as waking up after a power-down from ACTIVE to POWERDOWN, the E\_GPI10 bit must first be cleared of any previous GPI10 event. A safety timeout of 500 ms can be selected in TIME\_OUT to trigger a power-down to RESET mode (including the assertion of

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WAIT\_SHUT inside register FAULT\_LOG) if E\_GPI10 is not asserted in time. The ID WAIT\_STEP provides an alternate timer mode, selected by WAIT\_MODE and configured by WAIT\_TIME, which provides a delay timer for a selected sequencer step. To enable symmetric sequence behavior, ID WAIT\_STEP should not share a sequencer slot with other IDs. In the case of a shutdown sequence to RESET mode any waiting/delay at ID WAIT\_STEP is skipped.

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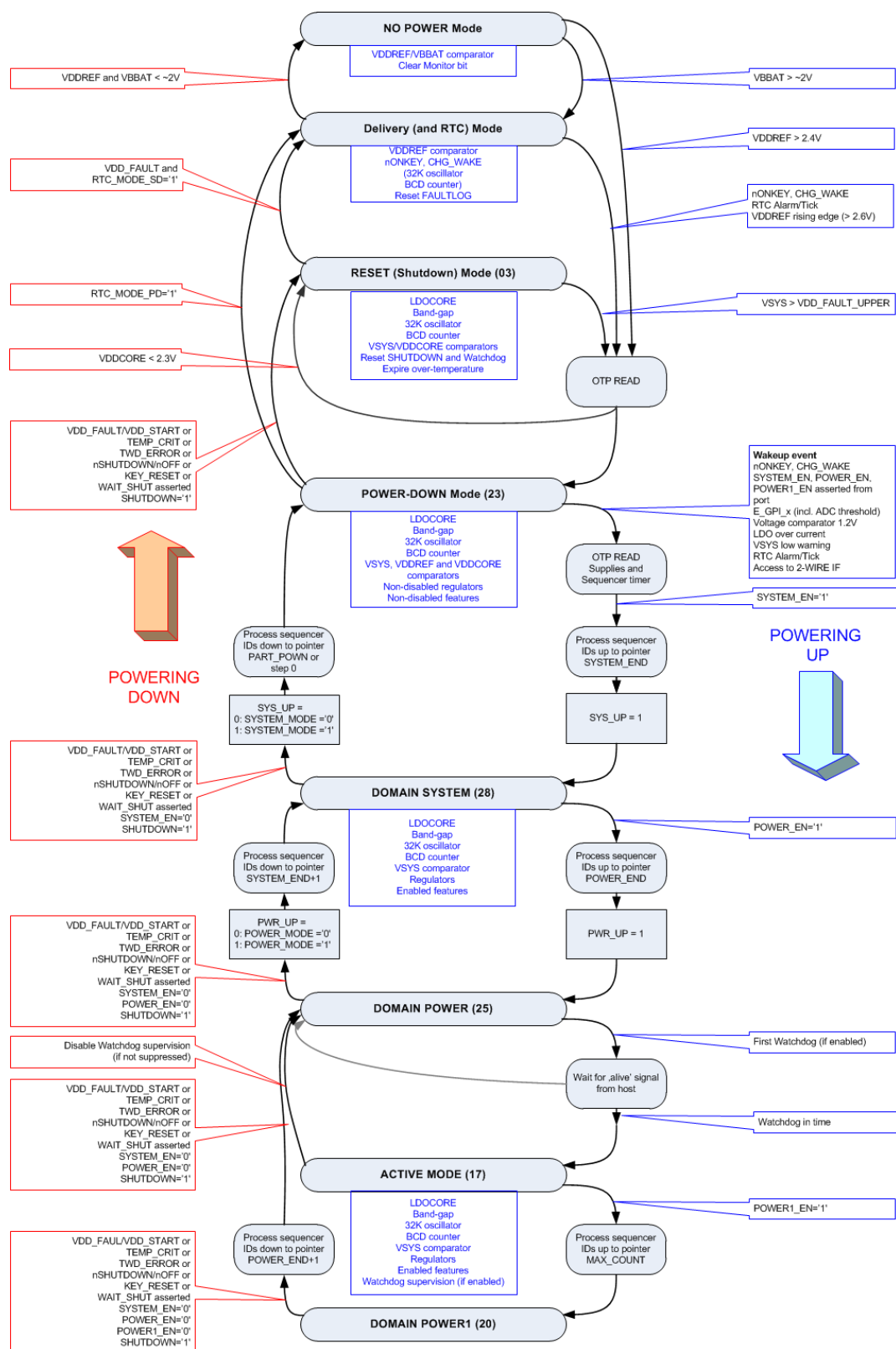


Figure 17: Power Mode Transitions

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### 6.6 System Monitor (Watchdog)

After powering up domain POWER, the DA9063 can initiate a watchdog monitor function. The host processor must write a 1 within a configured  $t_{WD\_MAX}$  time into control WATCHDOG, thereby indicating that the host is alive. If the host does not write 1 to this watchdog bit within the  $t_{WD\_MAX}$  time, the DA9063 asserts TWD\_ERROR in the FAULT\_LOG register and powers down to RESET mode.

After this first write, the host must continue to write to this watchdog bit within the configured time or DA9063 powers down as described above. The time window has a minimum time  $t_{WD\_MIN}$  fixed at 110 ms and a maximum time  $t_{WD\_MAX}$ , nominally 2.048 s. The  $t_{WD\_MAX}$  value can be extended by multiplying the nominal  $t_{WD\_MAX}$  by the value of register bits TWDSSCALE. TWDSSCALE is used to extend the  $t_{WD\_MAX}$  time by x1, x2, x4, x8, x16, x32, or x64.

Once in the ACTIVE state, the DA9063 continues to monitor the system unless it is disabled by setting TWDSSCALE to zero. When powering down from ACTIVE mode, the watchdog monitor is stopped unless it enters POWERDOWN mode via WATCHDOG\_PD.

If the WATCHDOG register bit is set to a 1 within the time window, the watchdog monitor resets the timer, sets the watchdog bit back to zero (this bit is always read as zero) and waits for the next watchdog signal. The watchdog trigger can also be asserted from the host by asserting KEEP\_ACT in hardware. This mode is selected with control PM\_FB2\_PIN and removes the above requirement for the periodic setting of the watchdog bit.

The watchdog feature can be disabled by setting TWDSSCALE to zero.

### 6.7 GPIO Extender

The DA9063 includes a GPIO extender that provides up to 16  $V_{DDREF}$ -tolerant general purpose input/output ports, each controlled via registers from the host, see [Table 42](#) and [Figure 18](#).

The GPIO ports are pin-shared with ports from GPADC, HS-2-WIRE-interface and signals from the power manager. Configuration settings and events from GPIx ports are also shared with alternative features. For example, if GPIO1\_PIN is configured to be ADCIN2, exceeding the configured ADC thresholds triggers a GPI1 event that generates a maskable GPI1 interrupt. The GPI active High/Low setting from the GPIOx\_TYPE register and the selection of pull-up resistor is also applicable to the alternative port functions selected via GPIOx\_PIN (for example, SYS\_EN, PWR\_EN and PWR1\_EN). This is also true for GPIOx\_WEN, which is used to enable triggering of a wake-up event (ADCIN1, ADCIN2, ADCIN3, SYS\_EN, PWR\_EN, PWR1\_EN, HS-2-WIRE interface). When GPI ports are enabled (including being enabled by changing the setting of GPIOx\_PIN), the GPI status bits are set to their non-active state. This ensures that any signals that are already active are detected and immediately generate any appropriate events.

In ACTIVE and POWERDOWN mode, the GPIO extender can continuously monitor the level of ports that are selected as general purpose inputs. GPIs are supplied from the internal rail VDDCORE or VDD\_IO2 (selected via GPI\_V) and can be configured to trigger events in active-high or active-low mode. The input signals can optionally be debounced (configurable via control DEBOUNCING, 10 ms default) and the resulting signal level is reflected by the status register GPIx. When the status has changed to its configured active state (edge sensitive) the assigned event register is set and the nIRQ signal is asserted (unless this nIRQ is masked). GPIs can be individually configured to generate a system wake-up via GPIxx\_WEN.

If enabled via regulator controls LDOx\_GPI/Bxxx\_GPI, the ports GPI1, GPI2, and GPI13 can be used to enable/disable regulators or rail switches (that is, controlling LDOx\_EN/Bxxx\_EN/xxx\_SW\_EN). The GPI active level is selected via the related GPIxx\_TYPE control. GPI ports that are selected for this hardware control of one or more regulators do not generate events (nIRQ). GPI1, 2, and 13 can alternatively be selected to toggle the VLDOx\_SEL/VBxxx\_SEL. Apart from changing the regulator

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output voltage, this feature also allows hardware control of regulator mode (sync/sleep mode) via selection of the settings contained in `xxxx_SL_A` and `xxxx_SL_B` (but only for those bucks configured with `Bxxxx_MODE = 00`). When a regulator is controlled via GPI, its enable and voltage register selection are no longer controlled by the power sequencer (processing the related ID only affects non-GPI controlled functionality). However, these settings can still be changed via register writes from the control interface.

Events on GPI10 can be used to control the progress of the power sequencer. Processing ID `WAIT_STEP` causes the sequencer to wait until GPI10 changes into its active state.

### Note

Supplies directly enabled/disabled from GPI1, 2, or 13 have to be excluded from the power sequencer control (IDs of these supplies should point into a slot higher than `MAX_COUNT`)

If defined as an output, GPO0, 1, 3 to 6, 10 to 11, and 13 to 15 can be configured to be open-drain instead of push-pull. The supply rail can be individually selected from either `VDD_IO1` or `VDD_IO2`. By disabling the internal 120 kΩ pull-up resistor when in open-drain mode, the GPO can also be supplied from an external rail (see registers `CONFIG_K` and `CONFIG_L`). The GPO output state reflects the respective register bit `GPIOn_MODE`.

When configured as outputs, GPO 2, 7, 8, 9, and 11 can be controlled by the DA9063 power sequencer. Five pairs of level asserting and level releasing IDs (`GP_RISE1_STEP/ GP_FALL1_STEP` to `GP_RISE5_STEP/ GP_FALL5_STEP`) may be assigned individually to slots of the power sequencer, which trigger the configured level transition on the GPOs when processing the related ID during powering up (see [Table 41](#) for assignments). The configured level change is inverted when processing the IDs during powering down. These are intended for use as enable signals either for external regulators or other devices in the system.

When the GPIO unit is off (POR), all ports are configured as open drain output with high level (pass device switched off, high impedance state). When leaving POR, the pull-up or pull-down resistors are configured from registers `CONFIG_K` and `CONFIG_L`. When the GPIO unit is temporarily disabled by the power sequencer (via `GPI_DIS` or `PMCONT_DIS`) level transitions on inputs are no longer detected and I/O drivers keep their configuration and programmed levels.

GPO12 can be driven by the state of `VDD_MON` to provide an active high 'Power good' signal (selected via `GPIO12_PIN`).

GPO10, 11, 14, and 15 are extended power GPO ports, where the maximum sink current is 11 mA and the maximum source current is 4 mA. This enables driving LEDs. The output ports GPO11, GPO14, and GPO15 can be toggled with a configurable periodic pulse configured via `BLINK_FRQ` and `BLINK_DUR` and include an optional PWM control. The generated PWM signals have a duty cycle from 0 % to 100 % with a repetition frequency of 21 kHz and 95 steps (using one 2 MHz clock for each step). The duty cycle is set by the controls `GPO11_PWM`, `GPO14_PWM`, and `GPO15_PWM`, with any value larger than 0 enabling the PWM mode of operation. The PWM control can also be made to dim the brightness between its current value and a new value at a rate of 32 ms per step. Selection of this mode is set by `GPO11_DIM`, `GPO14_DIM`, and `GPO15_DIM`. When set to zero the PWM ratio immediately changes. This creates a common anode tricolor LED brightness control. Flashing is driven from the crystal oscillator when control `CRYSTAL` has been asserted; otherwise an auxiliary on-chip oscillator is used.

LEDs are recommended to be low-side driven (using the GPIOs in sink mode) which is configured by setting `GPIOn_MODE = 1`.

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Table 42: GPIO Overview

| GPI<br>O | Alternate Port | Alternate Port Shared Resources                                   | GPI Wake-up                             | Remark                                                                                                                              |
|----------|----------------|-------------------------------------------------------------------|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 0        | ADCIN1         | E_GPIO0, M_GPIO0,<br>GPIO0_MODE                                   | x                                       | Auto measure ADC                                                                                                                    |
| 1        | ADCIN2         | E_GPIO1, M_GPIO1,<br>GPIO1_MODE                                   | Regulator control<br>x (in other modes) | Auto measure ADC/1.2V<br>comparator, HW control of<br>regulator                                                                     |
| 2        | ADCIN3         | E_GPIO2, M_GPIO2,<br>GPIO2_MODE                                   | Regulator control<br>x (in other modes) | Auto measure ADC, HW<br>control of regulator/ power<br>sequencer controlled GPO                                                     |
| 3        | CORE_SWG       |                                                                   | x                                       | Power sequencer controlled<br>ext. FET                                                                                              |
| 4        | CORE_SWS       |                                                                   | x                                       | Power sequencer controlled<br>ext. FET voltage sense                                                                                |
| 5        | PERI_SWG       |                                                                   | x                                       | Power sequencer controlled<br>ext. FET                                                                                              |
| 6        | PERI_SWS       |                                                                   | x                                       | Power sequencer controlled<br>ext. FET voltage sense                                                                                |
| 7        |                |                                                                   | x                                       | Power sequencer controlled<br>GPO                                                                                                   |
| 8        | SYS_EN         | E_GPIO8, M_GPIO8,<br>GPIO8_TYPE, GPIO8_WEN,<br>GPIO8_MODE         | x                                       | Power sequencer controlled<br>GPO                                                                                                   |
| 9        | PWR_EN         | E_GPIO9, M_GPIO9,<br>GPIO9_TYPE, GPIO9_WEN,<br>GPIO9_MODE         | x                                       | Power sequencer controlled<br>GPO                                                                                                   |
| 10       | PWR1_EN        | E_GPIO10, M_GPIO10,<br>GPIO10_TYPE,<br>GPIO10_WEN,<br>GPIO10_MODE | x                                       | High power GPO, input<br>signal for ID WAIT                                                                                         |
| 11       |                |                                                                   | x                                       | High power GPO (LED<br>flashing/PWM), Power<br>Sequencer controlled GPO                                                             |
| 12       | nVDD_FAULT     | GPIO12_TYPE,<br>GPIO12_WEN,<br>GPIO12_MODE                        | x                                       | VDD_MON state controlled<br>GPO (POWER_GOOD)                                                                                        |
| 13       | GP_FB1         | GPIO13_TYPE,<br>GPIO13_MODE                                       | Regulator control<br>x (in other modes) | HW control of regulator                                                                                                             |
| 14       | DATA           | E_GPIO14, M_GPIO14,<br>GPIO14_TYPE,<br>GPIO14_MODE                | x                                       | High power GPO (LED<br>flashing/PWM), Reset via<br>long assertion in parallel with<br>GPI15, 2nd 2-WIRE or DVC<br>Control Interface |

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| GPI O | Alternate Port | Alternate Port Shared Resources | GPI Wake-up | Remark                                                                                                                  |
|-------|----------------|---------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------|
| 15    | CLK            |                                 | X           | High power GPO (LED flashing/PWM), Reset via long assertion in parallel with GPI14, 2nd 2-WIRE or DVC Control Interface |

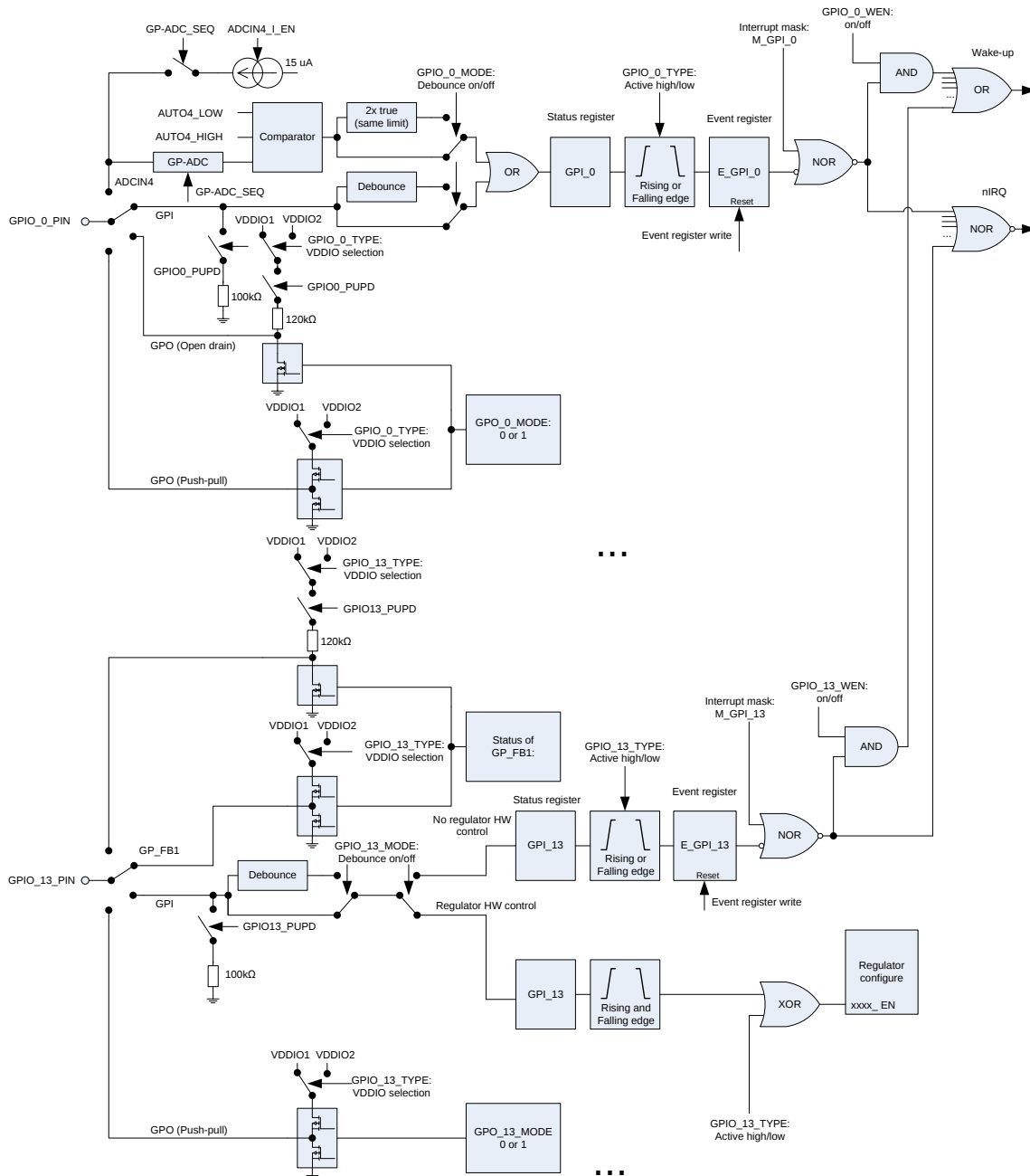


Figure 18: GPIO Principal Block Diagram (Example Paths)

## System PMIC for Mobile and Automotive Applications

### 6.8 Control Interfaces

The DA9063 is register controlled by the host software. The DA9063 offers two independent serial control interfaces to access these registers (Figure 19). The communication via the main power manager interface is selected via control IF\_TYPE during the initial OTP read to be either a 2-WIRE (I<sup>2</sup>C Compatible), or 4-WIRE (SPI compliant) connection. The alternate interface is a fixed 2-WIRE bus. Data is shifted into or out from DA9063 under the control of the host processor that also provides the serial clock. The interfaces are usually only configured once from OTP values, which are loaded during the initial start-up. The interface configuration can be changed by the host. However, care must be taken that changes are not made while the interface is active. If enabled, IF\_RESET forces a reset of all control interfaces when port nSHUTDOWN is asserted.

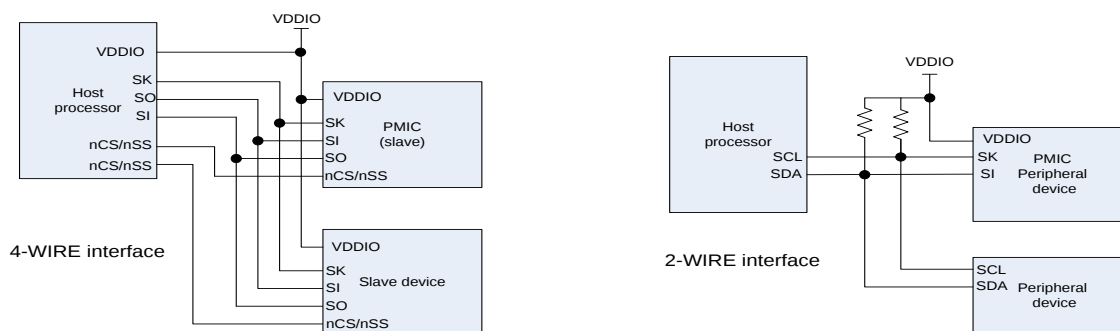
#### 6.8.1 Power Manager Interface (4- and 2-WIRE Control Bus)

This is the dedicated power control interface from the primary host processor. In 4-WIRE mode, the interface uses a chip-select line (nCS/nSS), a clock line (SK), a data input (SI), and a data output line (SO).

##### 6.8.1.1 4-WIRE Communication

In 4-WIRE mode, the DA9063 register map is split into four pages with each page containing up to 128 registers. The register at address zero on each page is used as a page control register. The default active page after reset includes registers 0x01 to 0x7F. Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting control REVERT. Unless REVERT was asserted after modifying the active page it is recommended to read back the page control register to ensure that future data exchange accesses the intended registers.

The 4-WIRE interface features a half-duplex operation (data can be transmitted and received within a single 16-bit frame) with an enhanced clock speed (up to 14 MHz). It operates at the provided host clock frequencies.



**Figure 19: Schematic of 4- and 2-WIRE Power Manager Bus**

A transmission begins when initiated by the host. Reading and writing is accomplished using an 8-bit command, which is sent by the host prior to the exchanged 8-bit data. The byte from the host begins shifting in on the SI pin under the control of the serial clock SK provided from the host. The first 7 bits specify the register address (0x01 to 0x7F) to be written or read by the host. The register address is automatically decoded after receiving the seventh address bit. The command word ends with a R/W bit which, together with the control bit R/W\_POL, specifies the direction of the next data exchange. During register writing, the host continues sending out data during the following 8 SK clocks. For reading, the host stops transmitting and the 8-bit register is clocked out of the DA9063 during the consecutive 8 SK clocks of the frame. Address and data are transmitted MSB first. The polarity

## System PMIC for Mobile and Automotive Applications

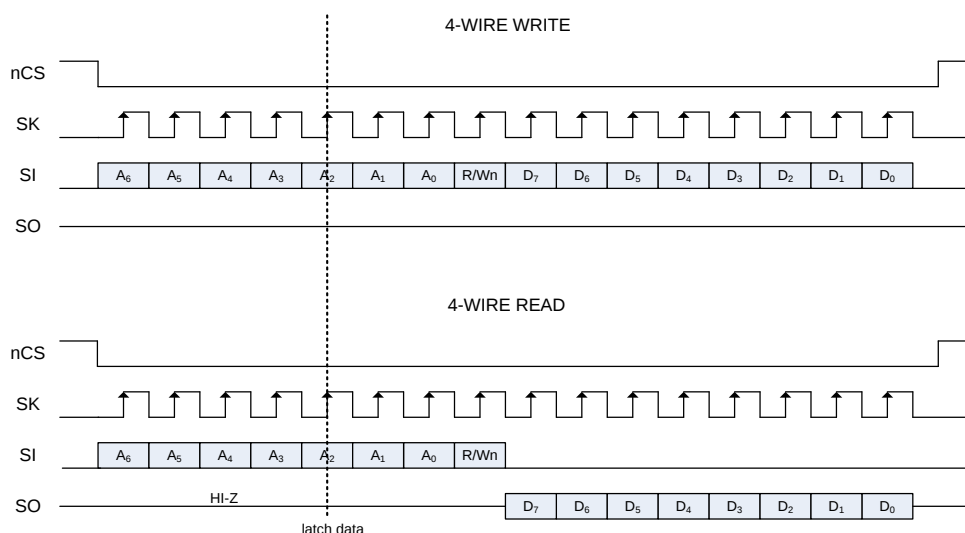
(active state) of nCS is defined by control bit nCS\_POL. nCS resets the interface when inactive and it must be released between successive cycles.

The SO output from DA9063 is normally in a high-impedance state and active only during the second half of read cycles. A pull-up or pull-down resistor may be needed on the SO line if a floating logic signal can cause unintended current consumption inside other circuits.

**Table 43: 4-WIRE Clock Configurations**

| CPOL Clock Polarity | CPHA Clock Phase | Output Data is Updated at SK Edge | Input Data is Registered at SK Edge |
|---------------------|------------------|-----------------------------------|-------------------------------------|
| 0 (idle low)        | 0                | falling                           | rising                              |
| 0 (idle low)        | 1                | rising                            | falling                             |
| 1 (idle high)       | 0                | rising                            | falling                             |
| 1 (idle high)       | 1                | falling                           | rising                              |

The DA9063 4-WIRE interface offers two further configuration bits. Clock polarity (CPOL) and clock phase (CPHA). CPOL determines whether SK idles high (CPOL = 1) or low (CPOL = 0). CPHA determines on which SK edge, data is shifted in and out. With CPOL = 0 and CPHA = 0, the DA9063 latches data on the SK rising edge. If CPHA = 1, the data is latched on the SK falling edge. The CPOL and CPHA states allow four different combinations of clock polarity and phase; each setting is incompatible with the other three. The host and DA9063 must be set to the same CPOL and CPHA states to communicate with each other.



**Figure 20: 4-WIRE Host Write and Read Timing (Ncs\_POL = 0, CPOL = 0, CPHA = 0)**

## System PMIC for Mobile and Automotive Applications

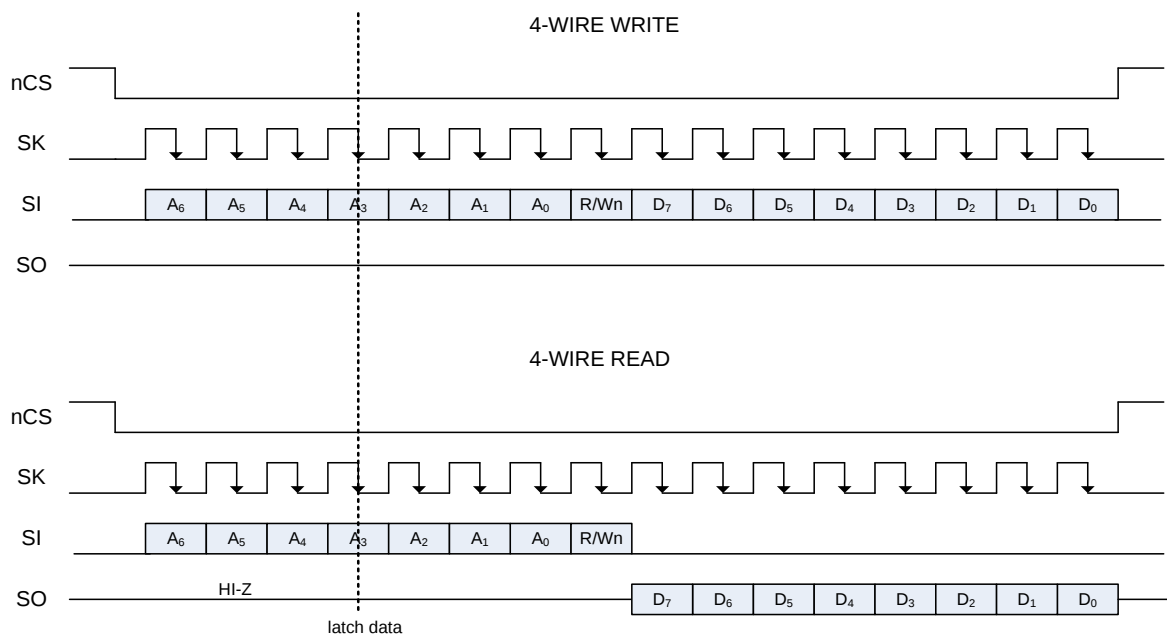


Figure 21: 4-WIRE Host Write and Read Timing (Ncs\_POL = 0, CPOL = 0, CPHA = 1)

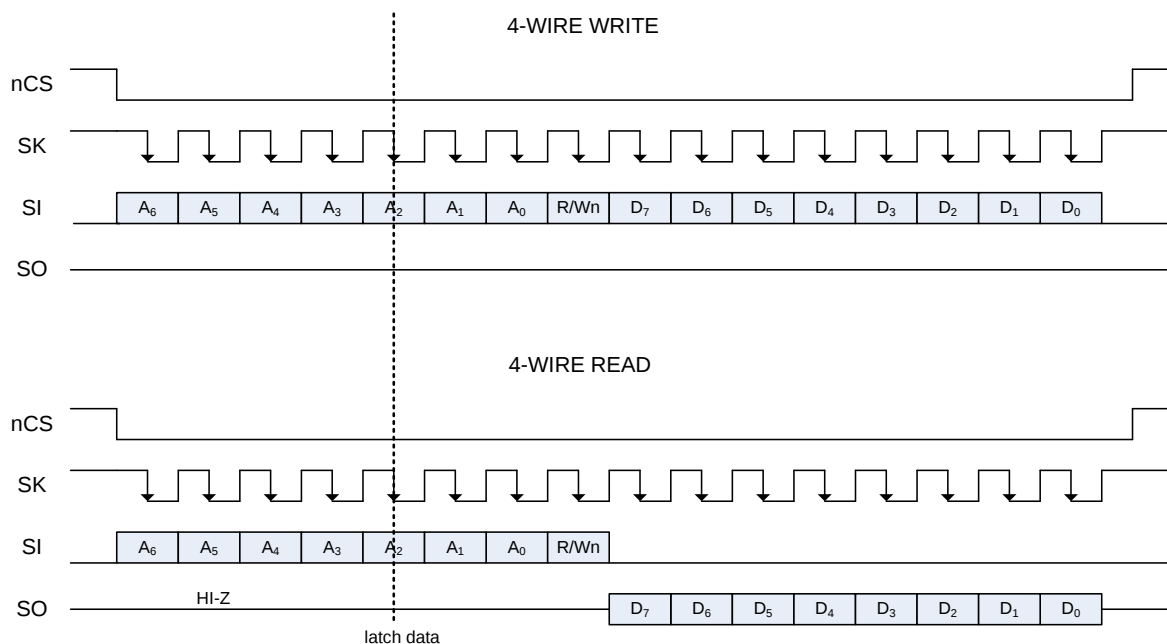


Figure 22: 4-WIRE Host Write and Read Timing (Ncs\_POL = 0, CPOL = 1, CPHA = 0)

## System PMIC for Mobile and Automotive Applications

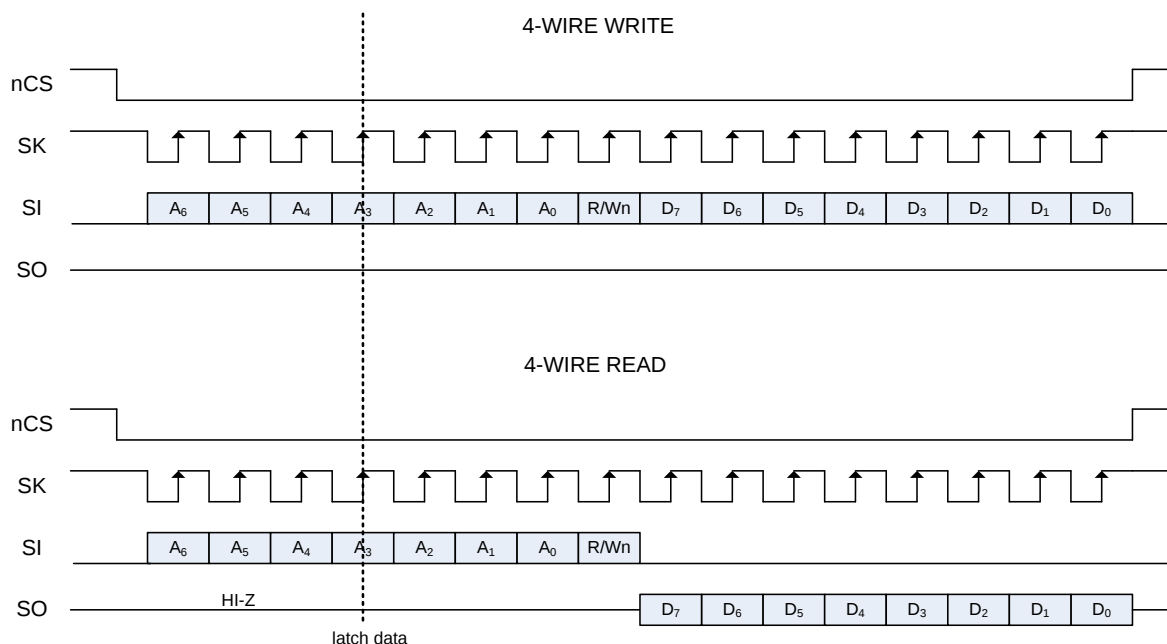


Figure 23: 4-WIRE Host Write and Read Timing (Ncs\_POL = 0, CPOL = 1, CPHA = 1)

Table 44: 4-WIRE Interface Summary

| Parameter      |                                 | Description                                 |
|----------------|---------------------------------|---------------------------------------------|
| Signal Lines   | nCS                             | Chip select                                 |
|                | SI Serial input data            | Master out, Slave in                        |
|                | SO Serial output data           | Master in, Slave out                        |
|                | SK                              | Transmission clock                          |
| Interface      | Push-pull with tri-state        |                                             |
| Supply voltage | Selected from VDD_IO1 / VDD_IO2 | 1.6 to 3.3 V                                |
| Data rate      | Effective read/write data       | Up to 7 Mbps                                |
| Transmission   | Half-duplex                     | MSB first                                   |
|                | 16-bit cycles                   | 7-bit address, 1-bit read/write, 8-bit data |
| Configuration  | CPOL                            | clock polarity                              |
|                | CPHA                            | clock phase                                 |
|                | nCS_POL                         | nCS active-low / -high                      |

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### 6.8.1.2 2-WIRE Communication

With control IF\_TYPE = 1, the DA9063 power manager interface is configured for 2-WIRE serial data exchange. It has a configurable device address IF\_BASE\_ADDR (default read address: 0xB1, write address 0xB0). For details of configurable addresses, see control IF\_BASE\_ADDR in Section A.4.2.

In 2-WIRE mode, SK is the clock (CLK) and SI is data (DATA). The 2-WIRE interface is open-drain, supporting multiple devices on a single line. The bus lines must be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). The attached devices only drive the bus lines low by connecting them to ground. As a result, two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode, the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and does not have any relation to the DA9063 internal clock signals. The DA9063 follows the host clock speed within the described limitations and does not initiate any clock arbitration or slow down. Control TWOWIRE\_TO enables an automatic interface RESET that is triggered when the clock signal ceases to toggle for >35 ms (compatible with SMBus T<sub>TIMEOUT</sub>).

The interface supports operation compatible with Standard, Fast, Fast-Plus and High Speed modes of the I<sup>2</sup>C-bus specification Rev 03 (UM10204\_3). Bus clear, in the case of the DATA signal being stuck low, is achieved after receiving 9 clock pulses. Operation in High Speed mode at 3.4 MHz requires a minimum interface supply voltage of 1.8 V and a mode change in order to enable spike suppression and slope control characteristics compatible with the I<sup>2</sup>C-bus specification. The high speed mode can be enabled on a transfer-by-transfer basis by sending the master code (0000 1XXX) at the beginning of the transfer. The DA9063 does not make use of clock stretching and delivers read data without additional delay up to 3.4 MHz.

Alternatively, the interface can be configured to continuously use High Speed mode via PM\_IF\_HSM, so that the master code is not required at the beginning of every transfer. This reduces communication overhead on the bus, but limits the attachable slaves to the bus to compatible devices.

Communication on the 2-WIRE bus always takes place between two devices, one acting as the master and the other as the slave. The DA9063 only operates as a slave. Opposite to the 4-WIRE mode, the 2-WIRE interface has direct access to two pages of the DA9063 register map (up to 256 addresses). The register at address zero on each page is used as a page control register (with the 2-WIRE bus ignoring the LSB of control REG\_PAGE). Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting control REVERT. Unless REVERT was asserted after modifying the active page, a read-back of the page control register is recommended to ensure that future data exchange is accessing the intended registers.

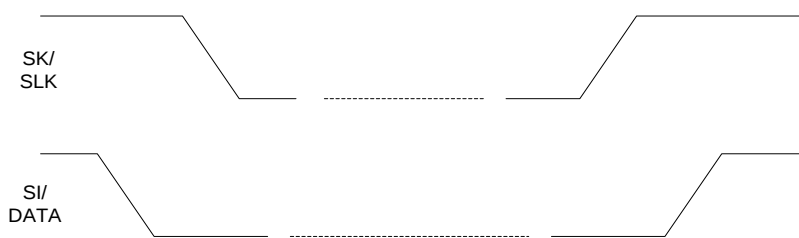
In 2-WIRE operation, the DA9063 offers an alternative method to access register pages 2 and 3. These pages can be accessed directly by incrementing the device address by one (default read address 0xB3; write address 0xB2). This removes the need to write to the page register before access to pages 2 and 3, thus reducing the traffic on the 2-WIRE bus.

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### 6.8.1.3 Details of the 2-WIRE Control Bus Protocol

All data is transmitted across the 2-WIRE bus in groups of 8 bits. To send a bit, the SI line is driven at the intended state while the SK is LOW (a low on SI indicates a zero bit). Once the SI has settled, the SK line is brought high and then low. This pulse on SK clocks the SI bit into the receiver's shift register, see [Figure 24](#).

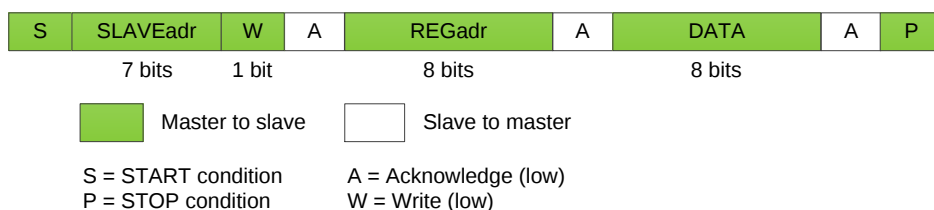
A two byte serial protocol is used containing one byte for address and one byte data. Data and address transfer is MSB transmitted first for both read and write operations. Transmission begins with the START condition from the master while the bus is idle. It is initiated by a high-to-low transition on the SI line while the SK is in the high state (a STOP condition is indicated by a low-to-high transition on the SI line while the SK is in the high state).



**Figure 24: Timing of 2-WIRE START and STOP Condition**

The 2-WIRE bus is monitored by the DA9063 for a valid slave address when the interface is enabled. It responds immediately when it receives its own slave address. This 'Acknowledge' is done by pulling the SI line low during the following clock cycle (see the white blocks marked A in [Figure 25](#) to [Figure 29](#)).

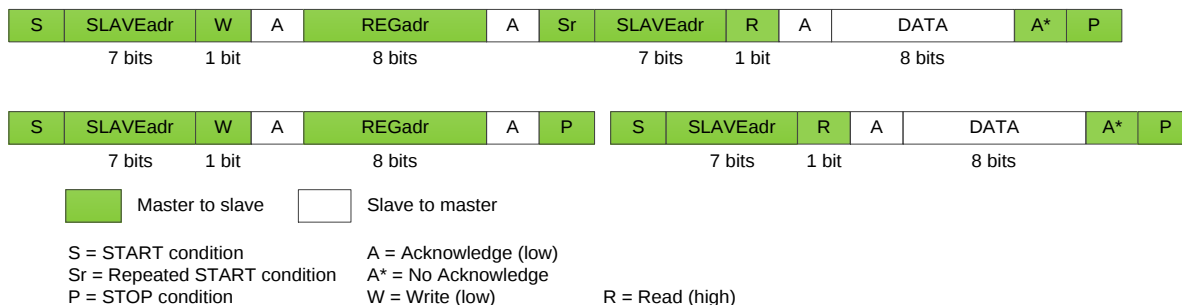
The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (all bytes responded by DA9063 with Acknowledge), as illustrated in [Figure 25](#).



**Figure 25: 2-WIRE Byte Write (SI/DATA Line)**

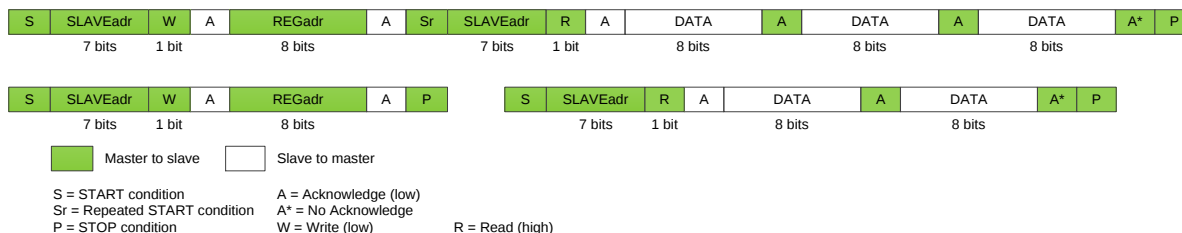
When the host reads data from a register, it first has to write access the DA9063 with the target register address and then read access the DA9063 with a Repeated START or alternatively a second START condition. After receiving the data, the host sends Not Acknowledge and terminates the transmission with a STOP condition ([Figure 26](#)).

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**Figure 26: Examples of 2-WIRE Byte Read (SI/DATA Line)**

Consecutive (page) read mode is initiated from the master by sending an Acknowledge instead of Not Acknowledge after receipt of the data word. The 2-WIRE control block then increments the address pointer to the next 2-WIRE address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a Not Acknowledge directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent 2-WIRE address is read then the DA9063 returns code zero (Figure 27).

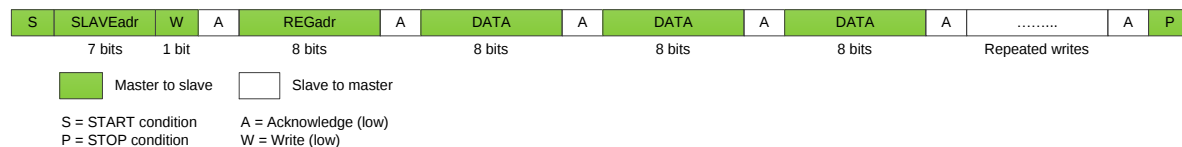


**Figure 27: Examples of 2-WIRE Page Read (SI/DATA Line)**

The slave address after the Repeated START condition must be the same as the previous slave address.

For enhanced data transfer efficiency, the DA9063 supports two write modes: Page Write mode and Repeated Write mode.

Page Write mode is used where the host has multiple bytes of data to be written to consecutive register addresses. It is selected by setting the WRITE MODE control to 0. For Page Write mode the master sends a device address followed by a register address then multiple data bytes. The 2-WIRE interface automatically increments the register address pointer after each data byte is received. The slave acknowledges each received byte of data until the master sends the STOP condition (Figure 28).



**Figure 28: 2-WIRE Page Write (SI/DATA Line)**

Repeated Write mode is used where the host has multiple bytes of data to be sent to non-consecutive registers. It is selected by setting the WRITE MODE control to 1. For Repeated Write mode the master sends a device address followed by multiple address-data pairs. The slave acknowledges each received byte until the master sends the STOP condition (Figure 29).

## System PMIC for Mobile and Automotive Applications

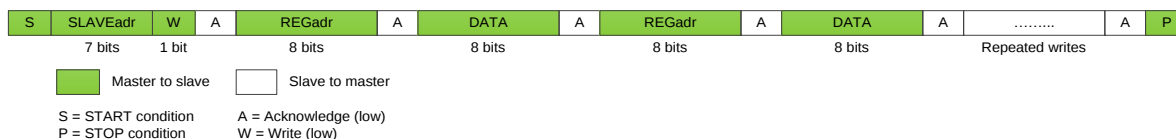


Figure 29: 2-WIRE Repeated Write (SI/DATA Line)

### 6.8.2 High Speed 2-WIRE Interface

The high speed HS 2-WIRE interface is the alternate serial control bus. It consists of DATA (data line) and CLK (clock line) and can be used as an independent control interface for data transactions between the DA9063 and a second host processor. The DA9063 high speed 2-WIRE interface has a configurable 8-bit write address (default 0xB4) and a configurable read address (default 0xB5). For details of configurable addresses see control IF\_BASE\_ADDR in Section A.4.2. The interface is enabled if HS2 DATA was selected via configuration control GPIO14\_PIN. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). GPIO14\_TYPE defines the supply rail of the interface (used for input logic levels and the internal pull-up resistors). The controls GPIO15\_PIN and GPIO15\_WEN are disabled when enabling the interface via GPIO14\_PIN.

When the interface receives a read or write command that includes a matching slave address, the DA9063 can trigger the assertion of nIRQ and an optional wake-up event (enabled via GPIO14\_WEN). If the nIRQ assertion from interface access is enabled (E\_GPI14), it should be masked as long as the HS 2-WIRE is in use. This nIRQ cannot be cleared via the HS 2-WIRE interface because every interface access triggers a re-assertion.

Except for the interface device addresses and the optional wake-up, the characteristics of the HS 2-WIRE interface are identical to the power manager 2-WIRE interface, see Section 6.8.1. High speed mode at 3.4 MHz can be enabled either via master code or continuously via PM\_IF\_HSM, but it does not support slope control for minimum tFDA specification.

### 6.9 Voltage Regulators

Three types of low drop-out regulators (LDOs) are integrated on the DA9063: for sensitive analog rails (for example, RF transceiver supply), the low noise regulators offer high PSRR across a wide frequency range; the LDOs provide an optimized PSRR and noise performance with lowest quiescent current. Quiescent current has been optimized for the always-on type regulators.

The regulators employ Dialog Semiconductor's Smart Mirror™ dynamic biasing that guarantees PSRR to be maintained across the full current range. Quiescent current consumption is dynamically adjusted to the load, which improves efficiency at light load conditions. Furthermore, Dialog Semiconductor's Smart Mirror™ technology allows the capacitor to be placed close to the load.

#### Note

When placing an LDO capacitor remotely from the DA9063, the voltage drop (= load current \* parasitic PCB impedance) needs to be considered when configuring the LDO output voltage.

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**Table 45: Regulator Control**

| Regulator | Type      | V <sub>OUT</sub> Steps (mV) | Mode   | Output Voltage (V)     | Supplied Max. Current (mA) | Current Limit LDO/ Bypass (mA) | V <sub>OUT</sub> Control          | Notes                                                     |
|-----------|-----------|-----------------------------|--------|------------------------|----------------------------|--------------------------------|-----------------------------------|-----------------------------------------------------------|
| LDO1      | Always-on | 20                          |        | 0.6 to 1.86            | 100                        | 200                            | DVC variable slew rate            | Optional voltage tracking                                 |
| LDO2      | Standard  | 20                          |        | 0.6 to 1.86            | 200                        | 400                            | DVC variable slew rate            |                                                           |
| LDO3      | Standard  | 20                          | Bypass | 0.9 to 3.44            | 200                        | 400/300                        | DVC variable slew rate            |                                                           |
| LDO4      | Standard  | 20                          | Bypass | 0.9 to 3.44            | 200                        | 400/200                        | DVC variable slew rate            |                                                           |
| LDO5      | Standard  | 50                          |        | 0.9 to 3.6             | 100                        | 200                            | V <sub>OUT</sub> programmable     |                                                           |
| LDO6      | Low noise | 50                          |        | 0.9 to 3.6             | 200                        | 400                            | V <sub>OUT</sub> programmable     |                                                           |
| LDO7      | Standard  | 50                          | Bypass | 0.9 to 3.6             | 200                        | 400/300                        | V <sub>OUT</sub> programmable     |                                                           |
| LDO8      | Standard  | 50                          | Bypass | 0.9 to 3.6             | 200                        | 400/400                        | V <sub>OUT</sub> programmable     | Switching vibration motor driver, common supply with LDO7 |
| LDO9      | Low noise | 50                          |        | 0.95 to 3.6            | 200                        | 400                            | V <sub>OUT</sub> programmable     | Common supply with LDO10                                  |
| LDO10     | Low noise | 50                          |        | 0.9 to 3.6             | 300                        | 400                            | V <sub>OUT</sub> programmable     | Common supply with LDO9                                   |
| LDO11     | Standard  | 50                          | Bypass | 0.9 to 3.6             | 300                        | 400/300                        | V <sub>OUT</sub> programmable     |                                                           |
| LDOCORE   | Always-on |                             |        | 2.5<br>±2%<br>accuracy | 4                          |                                | V <sub>OUT</sub> non-programmable | Internal LDO                                              |

### 6.9.1 Regulators Controlled by Software

The regulators can be programmed via the power manager interface. All regulators can be enabled or disabled by a write command to the enable bit LDOxx\_EN. Each LDO has two voltage registers for output voltage A and B. The appropriate values are stored in the registers VLDOxx\_A and VLDOxx\_B. The specific output voltage is selected with the bit VLDOxx\_SEL. Changes to this control result in immediate output voltage changes on non-DVC regulators and ramped voltage transitions on DVC-enabled regulators. The output voltage can also be changed by directly re-programming the voltage control register. The sequencer also uses these registers and may write to them: their contents can therefore be found to differ from previous write commands.

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For security reasons, the re-programming of registers that may cause damage when being incorrectly programmed (for example, voltage settings) can be disabled with control V\_LOCK. This disables write access to registers with an address higher than 0x7F.

### 6.9.2 Regulators Controlled by Hardware

All regulators can be enabled or disabled under hardware control using GPIO1, 2, or 13. The GPIO port used is defined in register LDOxx\_GPI. The output voltages can be switched by the GPIO port between the A and B voltage. The specific GPIO port is defined in register VLDOxx\_GPI. After detecting a rising or falling edge at the GPI, the DA9063 configures the related regulators with the status of GPI1, GPI2, or GPI13 (the event bit E\_GPI1, E\_GPI2, or E\_GPI13 is automatically cleared). A parallel write access to the regulator control registers is delayed and later overrides the hardware configuration. The sequencer does not affect regulators controlled via GPIOs.

### 6.9.3 Power Sequencer Control of LDOs

The power sequencer can control LDO1 to LDO11. The specific time slot of each LDO is defined with bit LDOx\_STEP in register bank starting at address 0x83. The sequencer enables and disables each LDO individually depending on the setting of each LDO's bit LDOx\_CONF and LDOx\_AUTO. To limit the inrush current, it is recommended to enable a maximum of one regulator (including bucks) per time slot.

If the control OTPREAD\_EN is set, the regulator control registers are reloaded from OTP before leaving POWERDOWN mode. During power-up, the sequencer always takes output voltage A (defined in register VLDOxx\_A). Therefore it also clears all VLDOxx\_SEL bits.

When powering down, the sequencer disables all LDOs, but the LDOs can be configured to remain on by setting bit LDOxx\_CONF. In this case the output voltage B is always selected (value programmed in register VLDOxx\_B). The related bit VLDOxx\_SEL is set by the sequencer accordingly.

**Table 46: LDO Power Sequence Voltage**

| LDO Output Voltage During Power-Up Sequencing   |           |                 |                |
|-------------------------------------------------|-----------|-----------------|----------------|
| LDOx_CONF                                       | LDOx_AUTO | LDO             | Output Voltage |
| -                                               | 1         | gets enabled    | A              |
| 1                                               | 0         | gets enabled    | A              |
| 0                                               |           | disabled        | -              |
| LDO Output Voltage During Power-Down Sequencing |           |                 |                |
| LDOx_CONF                                       | LDOx_AUTO | LDO             | Output Voltage |
| 1                                               | -         | remains enabled | B              |
| 0                                               |           | gets disabled   | -              |

The bit DEF\_SUPPLY defines the sequencer action for time slot 0. If Bit DEF\_SUPPLY is set, all LDOs configured to time slot 0 are enabled or disabled during power-up according to [Table 46](#). If bit DEF\_SUPPLY is not set, the LDOs configured to time slot 0 are disabled.

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### Note

When control bit LDOxx\_SL\_B is asserted, the LDO enters a forced sleep mode with the lowest quiescent current, but with a reduced maximum output current. The maximum current is reduced because a smaller output driver is used (a partial pass device). Asserting LDOxx\_SL\_A results in the same forced sleep mode for an LDO when using the type A voltage register. Before wake-up from POWERDOWN mode (processing time slots from domain SYSTEM), the sequencer can configure all regulators with default voltage values from OTP: this allows any previously altered VLDOxx\_A and LDOxx\_SL\_A settings to be reset.

Entering RESET mode automatically disables all regulators except LDO1. LDO1 stays enabled when entering RESET mode and can be used as an always-on supply (staying on even when  $V_{SYS}$  drops below VDD\_FAULT). However, LDO1 is disabled during NO-POWER, RTC and DELIVERY modes.

### 6.9.4 Dynamic Voltage Control

LDO1 to 4 include DVC:

- The output voltage can be programmed in 20 mV steps.
- If the feedback signal GP\_FB1 is configured to be READY (by asserting PM\_FB1\_PIN), this port is asserted while slewing and asserts E\_DVC\_RDY after all voltage and buck regulators have completed slewing.

DVC voltage transitions are handled by the following registers:

- Output voltage setting registers VLDO1\_A/VLDO1\_B to VLDO4\_A/VLDO4\_B.  
When writing into a selected voltage control register the output voltage is immediately ramped to the new value. When writing into the non-selected voltage register the ramping is delayed until this register is selected by toggling VLDOxx\_SEL.
- The voltage selection registers VLDOx\_SEL activate a pre-configured transition to the alternate output voltage. These controls have been grouped together in registers DVC\_1 and DVC\_2 to better enable synchronized ramping of supply voltages.
- The DVC slew rate for all DVC-enabled regulators can be configured as 10 mV per (0.5, 1.0, 2.0, or 4.0)  $\mu$ s via control SLEW\_RATE. Under light load conditions (< 10 mA), the slew rate is less than the programmed value when the output is close to the start and end of the slope. This is especially the case for the fastest slew rate settings. The negative slew rate is load dependent and might be lower than the one mentioned above.

### 6.9.5 Voltage Tracking Mode LDO1

LDO1 is able to follow the output voltage of buck converters BUCKCORE1, BUCKCORE2, or BUCKPRO. The specific buck converter is selected and enabled with the bits LDO1\_TRACK. The initial voltage delta between LDO1 and the DC-DC converter is captured and any voltage transition of the buck converter is mirrored to LDO1. Re-programming the LDO1 voltage register has no effect. Although LDO1 shares the ramping speed with the buck converter, the real LDO1 output voltage is also influenced by the load current. When the tracking mode is terminated via bit LDO1\_TRACK or the selected buck converter enters shutdown, LDO1 returns to its default output voltage (that is, to the value set in register VLDO1\_B or VLDO1\_A).

When the buck converter ramping exceeds the maximum or minimum voltage capability of LDO1, further steps below 0.6 V or above 1.86 V result in the temporary saturation of the LDO1 output voltage. The tracked buck converter should not ramp to below 0.6 V while LDO1 tracking is enabled.

The minimum delta voltage between the output of LDO1 and BUCKCORE is achieved by connecting the output of LDO1 to port CORE\_SWS\_GPIO4 and enabling the internal rail switch for the output of BUCKCORE1 (or dual-phase BUCKCORE) through the assertion of control CORE\_SW\_INT. In this case, the settings of the CORE\_SW rail controller are used to configure the internal switch with the

## System PMIC for Mobile and Automotive Applications

result that this channel of the rail switch controller can no longer drive external switches (GPIO3 may be used as a standard GPIO). The configured LDO1 output voltage should be equal to or slightly lower than  $V_{BUCK}$  when closing the switch. DVC transitions on BUCKCORE1 (or BUCKCORE) during this mode require LDO1\_TRACK to be programmed to 10.

### 6.9.6 Pull-Down Resistor

All LDOs have a pull-down resistor at the output when they are disabled. The pull-down resistor can be disabled with bit LDOxx\_PD\_DIS, and is required when LDOs are used in parallel with another supply. Otherwise the output is pulled to GND.

If an over-voltage occurs (LDO1 to 4:  $V_{OUT} > 109\%$  of nominal  $V_{OUT}$ , LDO5 to 11:  $V_{OUT} > 106\%$  of nominal  $V_{OUT}$ ), the voltage regulators enable an internal load to discharge the output back to its configured voltage. This can be disabled via LDOxx\_PD\_DIS.

### 6.9.7 Bypass Mode and Current Limit

All LDOs feature a current limiting function. For LDOs with a bypass mode (LDO3, 4, 7, 8, and 11), an over-current is indicated with an interrupt. When at least one of these LDOs reaches the current limit for more than 10 ms, an interrupt is raised to the host (during POWERDOWN mode a wake-up sequence is initiated) and the event bit E\_LDO\_LIM is set. The interrupt IRQ can be suppressed via the mask bit M\_LDO\_LIM.

If the current limit condition persists for more than 200 ms (indicating a probable short circuit condition), the related LDO is disabled and its LDOx\_EN bit is de-asserted. The LDO remains disabled until a new enable occurs (via hardware or software activation). The automatic shutdown of the LDO can be disabled via bit LDO\_SD. The host processor can distinguish if the IRQ is related to a temporary over-current or to a permanent shutdown by polling the related bit LDOx\_ILIM or checking LDO3\_EN, LDO4\_EN, LDO7\_EN, LDO8\_EN, and LDO11\_EN.

If the current limit is hit for more than 10 ms but less than 200 ms, the IRQ is generated but the related LDO is not disabled. If the current limit is hit for more than 200 ms and the involved LDO is shut down, the LDO<x>\_EN bit is de-asserted. If the over-current spike has stopped before the host is able to read the xx\_LIM bits, the LDO that has been in current limit cannot be evaluated.

Changing from LDO to bypass mode and back triggers a change of the output voltage with some over/undershoot during the transition phase.

The LDO accuracy specification is not applicable if the LDO has been configured for bypass mode.

For LDOs operated in bypass mode it is recommended to configure the voltage in the VLDO<x>\_A register to the expected output voltage of the LDO. When using the LDO above the normal operating range, it is recommended to set the VLDO<x>\_A to 0x40 for LDO 3 and 4 and to 0x20 for LDO 7, 8, and 11.

### 6.9.8 LDO Supply from Buck Converter

LDO1 to LDO11 can optionally be supplied from a buck output ( $V_{DD} < 2.8\text{ V}$ ). In this mode some specification parameters change:

- at  $V_{DD} = 1.8\text{ V}$ , the dropout voltage at  $I_{max}$  increases by 70 %
- for a supply voltage less than 1.8 V, the LDO dropout voltage is valid only for 1/3 of the standard  $I_{max}$  and the current capability decreases with the provided supply voltage.

LDO5 and LDO11 may be supplied from a rail higher than  $V_{SYS}/CHG\_WAKE$  (for example, the output of a 5 V boost) as long as  $V_{DD} < 5.5\text{ V}$ .

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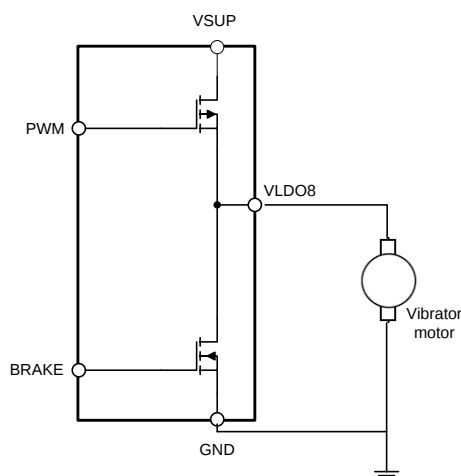
### 6.9.9 LDO Sleep Mode for Reduced $I_{OUT}$

If the required output current is  $< 10\%$  of  $I_{MAX}$ , the quiescent power can be reduced by setting an LDO into sleep mode. In this mode, the output driver current capability is reduced to  $10\%$  of  $I_{MAX}$ . Sleep mode can be set independently for the output voltage A and B by setting bit LDOxx\_SL\_A or bit LDOxx\_SL\_B. During LDO sleep mode, the over-current limit of the LDOs with a bypass function (LDO3, 4, 7, 8, and 11) is reduced to  $50\%$ . As a benefit of Dialog Semiconductor's Smart Mirror™ technology, sleep mode is typically not required because the quiescent current taken by the regulator is automatically minimized when operating at low current demands.

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### 6.9.10 Vibration Motor Driver

LDO8 provides a third mode dedicated to drive vibration motors selected via bit LDO8\_MODE. In this mode, the voltage regulation circuitry is disabled and no external stabilization capacitor is needed. In comparison to LDO mode, the PWM control is more efficient and allows an instant on and off for the vibrator signal.



**Figure 30: Vibration Motor Driver**

The vibrator motor driver is a half-bridge PWM-controlled motor driver, with an automatic battery supply correction of the PWM duty cycle (Figure 30). The PWM base frequency can be selected by PWM\_CLK to be either 1.0 MHz or 2.0 MHz (resulting in a PWM repetition rate of 15.6 kHz or 31.25 kHz). The vibration motor speed is determined by the effective output voltage which is set via control VIB\_SET (6 bits giving 64 programmable speeds). Setting the output voltage to 0 turns on a braking NMOS transistor to stop the vibration motor immediately.

The motor can also be stopped and started by a level on port nVIB\_BRAKE, if enabled via bit PM\_FB3\_PIN.

The PWM duty cycle is corrected automatically before it is enabled and after each breaking period. It is also automatically corrected every 10 s when it is running for longer periods. These corrections are done via autonomous  $V_{SYS}$  measurement via the internal GPADC (overrides control setting of AUTO\_VSYS\_EN). The duty cycle,  $D$ , is given by  $D = VIB\_SET / V_{SYS}$ .

#### Note

The half-bridge driver transistors have an internal current limit of approximately 400 mA

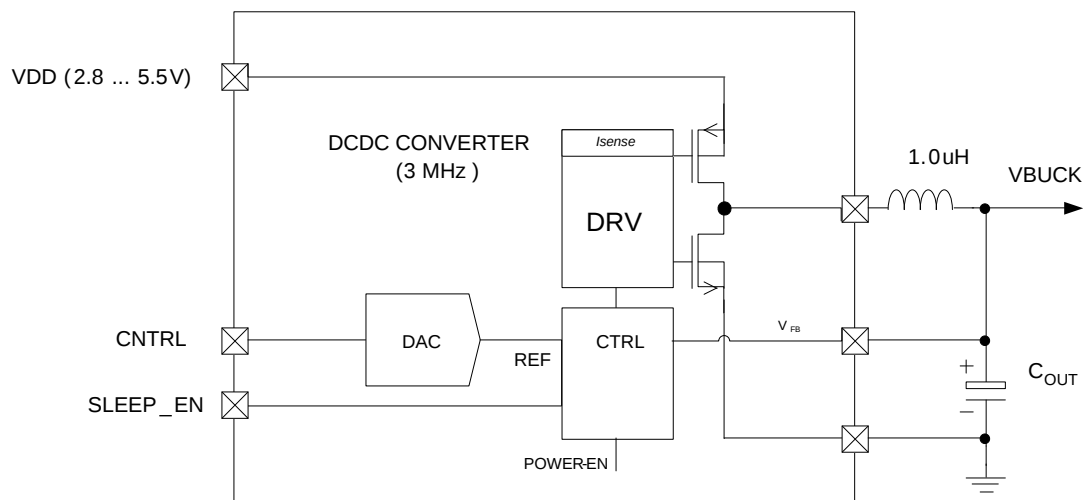
### 6.9.11 Core Regulator LDOCORE

The LDOCORE is a 2.5 V supply dedicated for the internal logic of DA9063. It is used for running the state machine, GPIO pins with comparators, bias, reference, GPADC, OTP, and power manager registers. It is supplied from internal rail  $V_{DDREF}$ , powered from either CHG\_WAKE or  $V_{SYS}$ . When LDOCORE is supplied in RESET mode, its output voltage is temporarily reduced to 2.2 V. In general, LDOCORE is an always-on supply (remaining enabled during RESET mode), but for lowest dissipation power LDOCORE can also be disabled when progressing towards RTC or DELIVERY mode.

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### 6.10 DC/DC Buck Converters

DA9063 includes six DC/DC buck converters with DVC.



**Figure 31: DC-DC Buck Converter**

The converters are high efficiency synchronous step-down regulators, operating at a high frequency (3 MHz), supplying individual output voltages with  $\pm 3\%$  accuracy. The default output voltage is loaded from OTP and can be set in 10 mV steps. To limit in-rush current from  $V_{SYS}$ , the buck converters perform a soft-start for up to 3 ms, when enabled via control `SOFT_START`. During this 3 ms period, the output current of the buck is limited. The use of the `SOFT_START` feature slows the start-up of the bucks. In the case where the load current exceeds the current limit during the first 3 ms, the output may fail to reach the programmed voltage until the end of the 3 ms period. The start-up sequence may have to be adjusted to take into account the `SOFT_START` behavior.

The DVC controller allows the following features:

- The buck converter output voltage is programmable over the power manager bus in 10 mV steps.
- If the feedback port `GP_FB1` is configured as `READY`, this port is asserted while slewing and asserts `E_DVC_RDY` after all voltage and buck regulators have stopped slewing.
- Output voltages below 0.7 V are only supported in Pulse Frequency Modulation (PFM) mode. During a voltage reduction below 0.7 V, the slew rate control ends at 0.7 V and the buck mode is automatically changed to PFM mode.

The DVC control is handled by the following registers:

- Output voltage setting register `VBxxxx_A/VBxxxx_B`.  
When writing to the voltage control register that is in use by an enabled buck, the output immediately ramps to the new setting. When writing to the voltage control register that is not in use, the ramping is delayed until this register is selected by toggling `VBxxxx_SEL`.
- The voltage register selection `VBxxxx_SEL`.  
This activates a pre-configured transition to the alternate output voltage. These controls are grouped into registers `DVC_1` and `DVC_2` to better enable synchronized ramping of supply voltages.
- The DVC slew rate is programmable as at 10 mV per (4, 2, 1, or 0.5)  $\mu\text{s}$  via control `SLEW_RATE`. During PFM mode, the negative slew rate is load-dependent and might be lower than the programmed rate.

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The supply current during PWM (synchronous) operation is in the order of 3.5 mA (quiescent current and charge/discharge current) and drops to <1  $\mu$ A in shutdown. Switching frequency is chosen to be high enough (3 MHz) to allow the use of a small 1.0  $\mu$ H inductor.

The operating mode of the buck converter is selected via the buck control register bits B<x>\_MODE. The buck converter can be forced to operate in either PWM or PFM mode. Additionally, the buck converter has an automatic mode where it switches between PWM and PFM modes depending on the load current.

The switching converters can be enabled/disabled/configured via the power manager and HS 2-WIRE interface. Writing to Bxxxx\_EN/VBxxxx\_SEL unconditionally configures the regulator to the selected mode (enabled/disabled). Reading Bxxxx\_EN/VBxxxx\_SEL provides the actual state, which may differ from a previous write (in the case where the regulator state is changed from GPIO or power sequencer control). All bucks can be controlled with an ID from the power sequencer. If enabled in DEF\_SUPPLY, supplies can be configured to default settings when the sequencer passes slot 0.

To limit the inrush current, it is recommended to select individual regulators (including LDOs) only with xxxx\_DEF settings.

When powering up, the power sequencer clears VBxxxx\_SEL for a buck when it has an ID pointing to the time slot being processed. This forces the regulator to ramp the output voltage to the value programmed inside the related register VBxxxx\_A.

When powering down (for example, to POWERDOWN mode), sequencer-controlled supplies are usually disabled but can be configured to remain on by setting Bxxxx\_CONF. In the latter case, the sequencer sets VBxxxx\_SEL so that the regulator output voltage is ramped to the value programmed inside the related register VBxxxx\_B. Disabled bucks can switch off their pull-down resistor, see Section 6.9.5. Before wake-up from POWERDOWN mode (processing time slots from domain SYSTEM), the sequencer can configure the bucks with default voltage values from OTP and reset any changed VBxxxx\_A settings.

All buck converters provide an optional hardware enable/disable via GPIO1, 2, and 13. A regulator that has to be enabled/disabled from a GPI port selects this feature via its control Bxxxx\_GPI. A change of the output voltage from the state of a GPI is enabled via control VBxxxx\_GPI. After detecting a rising or falling edge at the GPI, the DA9063 configures the enabled regulators with the status of GPI1, GPI2, or GPI13 (the event bit E\_GPI1, E\_GPI2 or E\_GPI13 is automatically cleared). A parallel write access to the regulator control registers is delayed and later overrides the HW configuration. The sequencer does not change regulator settings enabled for GPI control. Powering down to RESET mode automatically disables all buck converters. When the output of a buck converter is combined with a parallel low power LDO, its pull-down resistor needs to be disabled via Bxxxx\_PD\_DIS. Otherwise its output is discharged to GND when being disabled.

To allow DVC transitions under load, the buck current limit should be configured at least 40% higher than the required maximum continuous output current. See Table 47 as a guide to determining this limit.

**Table 47: Selection of Buck Current Limit from Coil Parameters**

| Min. ISAT (mA) | Frequency (MHz) | Buck Current Limit (mA) | Max. Output Current (mA) |
|----------------|-----------------|-------------------------|--------------------------|
| 3800           | 3               | 3400                    | 2400                     |
| 3100           | 3               | 2800                    | 2000                     |
| 2400           | 3               | 2100                    | 1500                     |
| 1700           | 3               | 1700                    | 1200                     |

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To ensure correct regulation, the buck converters require the supply voltage to be 0.7 V higher than the output voltage. As this is not always possible at higher output voltage settings, the converters BUCKMEM, BUCKIO, and BUCKPERI provide a follower mode where the electrical characteristics of the DC-DC converter no longer apply, but instead the PMOS output driver is fully-on and the output voltage simply follows the dropping input voltage. There will be a voltage drop between the buck VDD supply and the output which results from the on-resistance of the buck PMOS driver and the coil, with the voltage drop magnitude being depending on load current. Bucks running in follower mode will temporarily stop switching and by that process will generate PWM mode 3 MHz sub-harmonics.

### 6.10.1 Active Discharge

When switching off a buck converter the output rail can be actively discharged. This feature is enabled by setting BUCK\_ACTV\_DISCHRG. The discharge is implemented by ramping down the output voltage using DVC.

### 6.10.2 BUCKCORE1, BUCKCORE2, and BUCKPRO

BUCKCORE1, BUCKCORE2, and BUCKPRO include a full-current (previously overdrive) mode, individually enabled via control BCORE1\_OD, BCORE2\_OD, and BPRO\_OD.

In full-current mode:

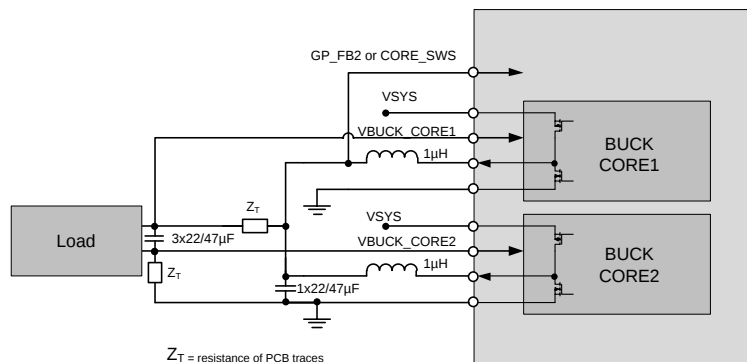
- The maximum current capability is 2500 mA
- The selected current limits are automatically doubled
- The quiescent current increases due to the increased switching losses

For full-current mode, the application requires two 47  $\mu$ F output capacitors and an appropriate inductor that can sustain higher currents without heating up or suffering from inductance degradation.

BUCKCORE1 and 2 can also be merged as a dual-phase BUCKCORE with up to 5000 mA maximum output current. If enabled in OTP via BCORE\_MERGE, the register controls of BUCKCORE2 (except BCORE2\_PD\_DIS) are automatically disabled and the output from both coils must be routed together. The feedback signal for both phases is taken from the sense node switch matrix of BUCKCORE1 (the VBUCKCORE2 pin may be left floating if the internal pull-down resistor is enabled by setting BCORE2\_PD\_DIS = 0). With BCORE1\_FB programmed in OTP to 0b000, a differential remote sensing at the point-of-load can be enabled, using VBUCKCORE2 as a GND sense port. In this mode, the BUCKCORE output capacitor voltage has to be routed to port CORE\_SWS or GP\_FB\_2 (selected via control MERGE\_SENSE). Depending on the settings of BCORE1\_OD, the dual-phase buck provides a maximum 2500 mA or 5000 mA, requiring two or four 47  $\mu$ F output capacitors, respectively.

BUCKCORE2 always runs on the inverted clock (anti-phase) of BUCKCORE1. The switching node output of both phases must be connected symmetrically on the PCB (with matched routing inductances and resistances).

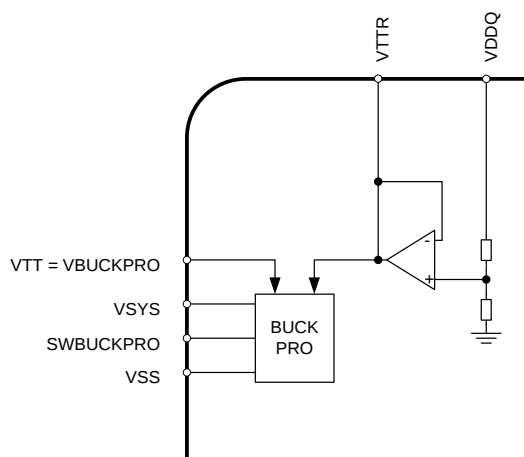
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**Figure 32: BUCKCORE1 and BUCKCORE2 in Dual-Phase Remote Sense Mode**

### 6.10.3 BUCKPRO in DDR Memory Bus Termination Mode

If enabled via BPRO\_VTT\_EN, BUCKPRO offers an alternative mode to provide VTT bus termination for DDR memory. In this mode, its output voltage tracks 50 % of the VDDQ sense port voltage (Figure 33). In this mode, BUCKPRO must be set to sync mode either by the host or by OTP configuration. If enabled via BPRO\_VTTR\_EN, a second VTTR output provides the same voltage for a DDR VTTR reference rail, buffered with  $\pm 10$  mA source/sink capability (requires 0.1  $\mu$ F stabilization capacitor). With BPRO\_VTTR\_EN being asserted in combination with BPRO\_VTT\_EN released, the DA9063 provides a VTTR reference buffer with BUCKPRO running in a normal output voltage control mode. If memory termination is not required (BPRO\_VTTR\_EN = 0), port VDDQ provides the state of event E GPI2 and port VTTR provides the state of the 1.2 V comparator.



### Figure 33: BUCKPRO Memory Bus Termination Mode

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### 6.10.4 BUCKMEM and BUCKIO in Merged Mode

The converter BUCKMEM can be merged with BUCKIO via control BUCK\_MERGE to form a single DC-DC converter with a maximum output current of 3000 mA (Figure 34). The routing of the switcher output pins to the common inductor must be symmetrical. The VBUCKIO feedback pin may be left floating in merged mode if its internal pull-down resistor is enabled by setting BIO\_PD\_DIS = 0. The inductor (1.0  $\mu$ H) and the output capacitor have to be selected according to the increased output current configuration controls of BUCKIO are disabled by asserting the bit BUCK\_MERGE; the selected current limits of BUCKMEM are automatically doubled.

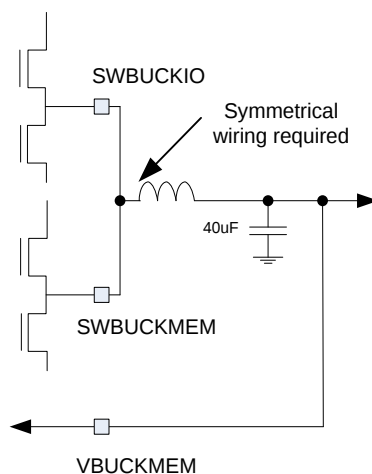


Figure 34: BUCKMEM Merged With BUCKIO

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### 6.11 Buck Rail Switches

BUCKCORE and BUCKPERI offer a gate driver for an external NMOS that allows an output rail shutdown and re-enable independently from the state of the buck (Figure 35). If a switch is open, the associated pin is discharged to VSS by a pull-down resistor. All switch outputs require 100 nF decoupling. All switches provide a soft-start in the form of a slew-rate limit which can be programmed via control SWITCH\_SR. The input surge current is therefore linearly proportional to the capacitance connected to the output of the switch.

When the switch is closed, the buck can be configured by control Bxxx\_FB to select the switch output signal as a voltage sense node (instead of the buck output voltage) to compensate for losses in the switch. Otherwise, Bxxx\_FB should be programmed as 0b001 (setting 0b000 is invalid).

Where a buck does not require a rail switch, it can be routed to the output of another buck. In this case, the feedback control should be programmed to 0b001. The feedback of the buck using both switches may be programmed to be taken from the output of CORE\_SW (CORE\_SWS) or the output of PERI\_SW (PERI\_SWS), or even from a mix of both (averaged). When a switch is opened, its signal is automatically disconnected from the feedback path. When all switches selected for the feedback signal mix are open, the buck automatically switches the feedback back to its output.

Before any of the rail switches can be closed, a charge pump must be enabled via control CP\_EN. Depending on the setting of CP\_EN\_MODE, it may be automatically disabled when all buck rail switches are opened. During charge pump automatic mode, closing the first switch is delayed until the charge pump has stabilized its output voltage (< 700  $\mu$ s).

The state of each switch is controlled via its control xxx\_SW\_EN. These bits can be modified by a register write or via GPI1, 2, or 13 if enabled by register SWITCH\_CONT. Alternatively, they can be controlled from the power sequencer by programming controls xxx\_SW\_STEP into the intended time slot (which closes the switches on power-up and opens the switches on power-down). By asserting xxx\_SW\_CONF, the sequencer can be forced to leave the switch closed when powering down.

If a buck rail switch is not required, its ports can instead be used as a GPIO (selected via GPIOxx\_TYPE).

Additional rail switches are available by using LDOs 3, 4, 7, 8, and 11 in bypass mode.

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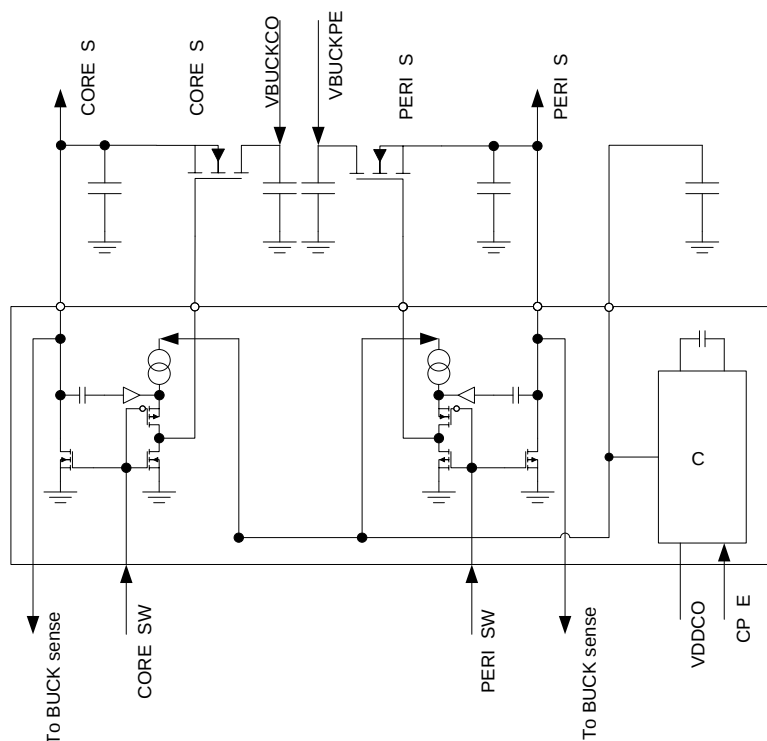


Figure 35: Buck Rail Switches

### 6.12 Backup Battery Charger/RTC Supply Rail Generator

The backup battery charger provides a constant charge current with a programmable top-up charging voltage for charging of Lithium-Manganese coin cell batteries and super capacitors. Charging current is programmable via `BCHG_ISET` from 100 to 1000  $\mu\text{A}$  (in 100  $\mu\text{A}$  steps) and from 1 mA to 6 mA (in 1 mA steps). End-of-charge termination voltage is programmable in 100 mV/200 mV steps from 1.1 V to 3.1 V. The backup battery charger is enabled by setting `BCHG_VSET` and `BCHG_ISET` to a non-zero value. When enabled, the charger aims to maintain the backup battery at its target voltage. The backup battery charger can be temporarily disabled in POWERDOWN mode via control bit `BBAT_DIS` and it switches off automatically during a POR.

The backup battery charger includes reverse current protection and can also be used as an ultra-low quiescent always-on supply for low voltage/power rails (may stay on during RESET mode).

The backup battery rail follower provides the internal supply voltage `VDDRTC` for the 32 kHz oscillator and RTC digital whenever being powered from `VDDREF` ( $V_{DDREF} > 2.4\text{ V}$ ) or from a backup battery ( $V_{BBAT} > 2.0\text{ V}$ ), depending on the following conditions:

- If only the backup battery is applied (for example, in case of a deep discharged or removed main battery) the switch automatically connects the RTC block to the backup battery.
- If both the system rail `VDDREF` and the backup battery are present, the RTC block is powered by the higher of these two voltage sources. This implementation allows for maximum utilization of the energy left in the main battery, thus extending the life of the lower capacity backup battery. A seamless transition is achieved by the `VDDRTC` follower by generating a replica of the backup battery voltage from `VDDREF` (min. 1.45 V). To limit the oscillation while switching between `VBBAT` and the internal replica voltage, the backup battery switch has a built-in hysteresis of 75 mV.

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### 6.13 General Purpose ADC

#### 6.13.1 ADC Overview

The Analog to Digital Converter (ADC) uses a sample and hold successive approximation switched capacitor architecture. It is supplied from VDDCORE (2.5 V). Configured via control ADC\_MODE, it can be used either in high-speed mode with measurement sequences repeated every 1 ms or in economy mode with sequences repeated every 10 ms.

#### 6.13.2 ADC Input MUX

The DA9063 provides an ADC with 10-bit resolution and track and hold circuitry combined with an analog input multiplexer (Figure 36). The analog input multiplexer allows conversion of up to nine different inputs. The track and hold circuit ensures stable input voltages at the input of the ADC during the conversion.

The ADC is used to measure the following inputs:

- Channel 0: VSYS\_RES – measurement of the system VDD (2.5 to 5.5 V)
- Channel 1: ADCIN1\_RES – high impedance input (0 to 2.5 V)
- Channel 2: ADCIN2\_RES – high impedance input (0 to 2.5 V)
- Channel 3: ADCIN3\_RES – high impedance input (0 to 2.5 V)
- Channel 4: T<sub>J</sub> – measurement of internal temperature sensor
- Channel 5: V<sub>BAT</sub> – measurement of the backup battery voltage (0 to 5.0 V)
- Channel 8: MON\_A8\_RES – group 1 internal regulators voltage (0 to 5.0 V)
- Channel 9: MON\_A9\_RES – group 2 internal regulators voltage (0 to 5.0 V)
- Channel 10: MON\_A10\_RES – group 3 internal regulators voltage (0 to 5.0 V)

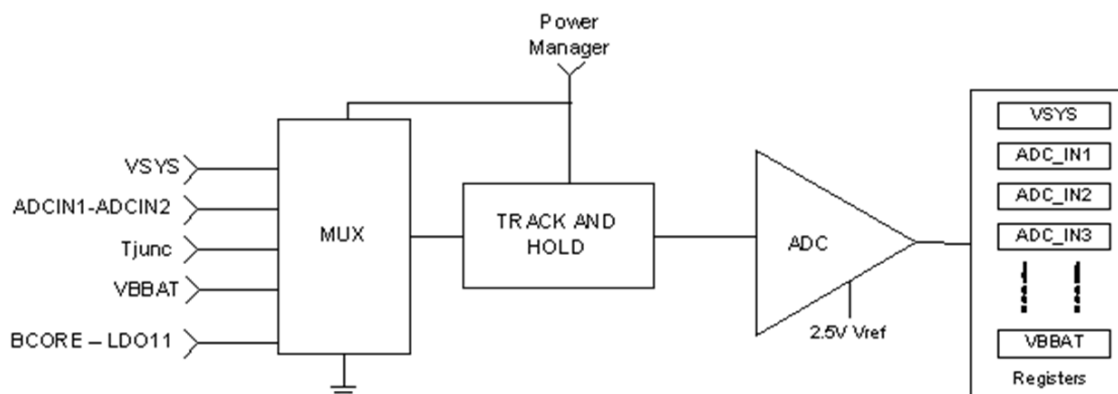


Figure 36: ADC Block Diagram

The MUX selects from and isolates the nine inputs, and presents the channel to be measured to the ADC input. When selected, an input amplifier on the V<sub>sys</sub> channel subtracts the VDDCORE reference voltage and scales the signal to the correct value for the ADC.

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### 6.13.3 Manual Conversion Mode

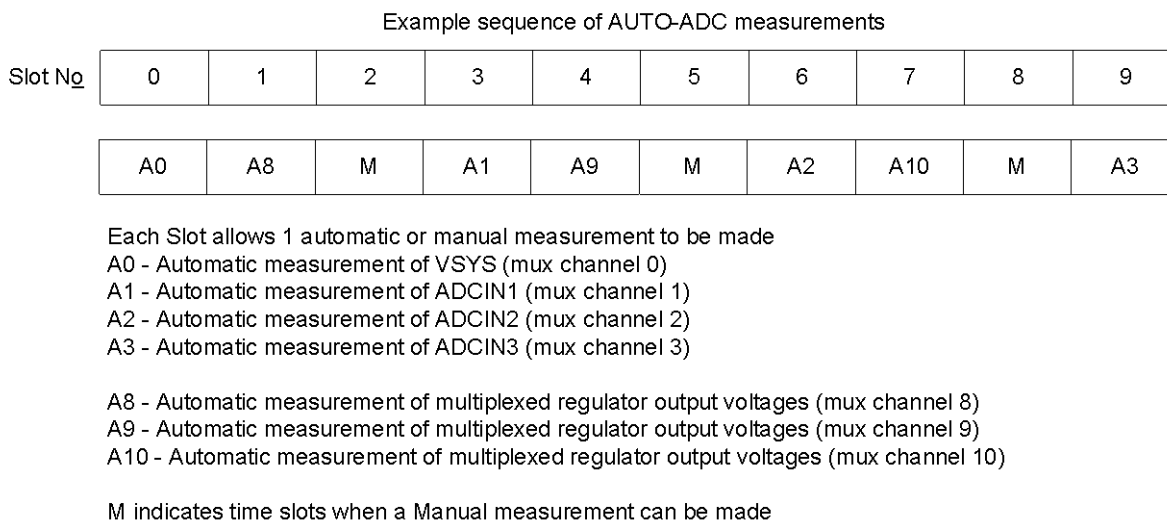
Manual measurements by the ADC are initiated by an ADC\_MAN bit register write. The ADC powers up, one conversion is done on the channel specified by ADC\_MUX and the 10-bit result is stored in the ADC\_RES\_H and ADC\_RES\_L registers. After the conversion is completed, the ADC powers down again, ADC\_MAN bit is reset and an IRQ event flag is set (E\_ADC\_RDY). The generation of this IRQ can be masked by the IRQ mask M\_ADC\_RDY.

### 6.13.4 Automatic Measurements Scheduler

The automatic measurement scheduler allows monitoring of the system voltage  $V_{SYS}$ , the auxiliary channels ADCIN1 to 3 and the output voltage supervision of embedded regulators. The results are automatically compared with upper and lower thresholds set by power manager registers to give an nIRQ event if a measurement is outside these levels. All measurements are handled by the scheduler system detailed below.

The scheduler performs a sequence of 10 slots continually repeated according to the configured mode. A slot requires 100  $\mu$ s. The pattern of measurements over the 10 slots depends upon the enabled automatic measurements. Additional manual measurement opportunities are available in slots where automatic measurements have been disabled by control bits in ADC\_CONT. Automatic measurements only store the eight MSBs of the ADC measurement.

Figure 37 shows (with typical configurations) how the different measurements are scheduled.



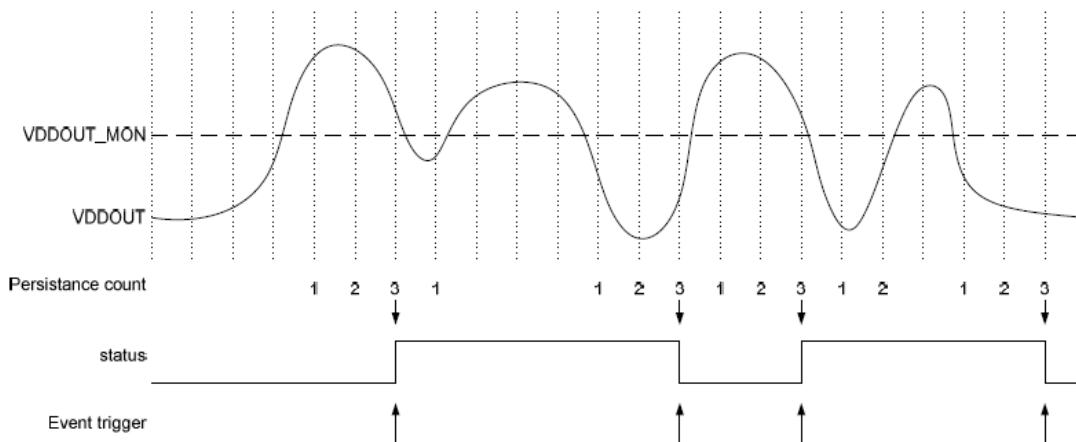
**Figure 37: ADC Sequence**

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### 6.13.4.1 A0: $V_{SYS}$ Voltage nIRQ Measurement Mode

$V_{SYS}$  is measured, stored in  $VSYS\_RES$  and compared with the  $VSYS\_MON$  threshold. If the result of the comparison is different to its previous state (being either lower or higher) for three consecutive readings, an  $E\_VDD\_MON$  event is generated. Glitches of a duration less than three consecutive measurements do not update the state; events are triggered at rising and falling edges of the state signal. This multiple reading debounces the  $V_{SYS}$  voltage before issuing an nIRQ. After the nIRQ assertion, the automatic measurement of channel  $V_{SYS}$  is paused for reading. The host must clear the associated event flag to re-enable the supervision of  $V_{SYS}$ . The event-causing value is kept in the result register.

If selected via  $GPIO12\_PIN$ , the debounced comparator state can be indicated via the GPO12 port, representing a power good signal that can be used, for example, to trigger boot activities on external ICs. If no action is taken to restore the  $V_{SYS}$  voltage (that is, discharging of the battery continues), the host may consider switching off optional 'always-on' blocks (for example, backup battery) to save energy later on.  $V_{SYS}$  measurements are enabled via control  $AUTO\_VSYS\_EN$ .



**Figure 38:  $V_{SYS}$  Monitor Persistence Behavior**

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### 6.13.4.2 A1, A2, A3: Automatic Measurement and High/Low Threshold Warning nIRQ Mode

The automatic measurement result of channel ADC\_IN1 is stored in the ADCIN1\_RES register. If a reading of A1 is less than AUTO1\_LOW or greater than AUTO1\_HIGH, then the event flag E\_GPIO is set. If nIRQ is asserted, the automatic measurement of channel ADC\_IN1 is paused until the host has cleared the associated event flag (the event-causing value is kept in the result register). The assertion of nIRQ can be masked by IRQ mask M\_GPIO, which also disables the pausing of automatic measurements. If debouncing is selected via ADCIN1\_DEB the event is only asserted if two consecutive measurements override the same threshold. The automatic measurement is enabled by register AUTO\_AD1\_EN. In addition, it is possible to use ADCIN\_1 with a 1  $\mu$ A to 40  $\mu$ A current source that allows automatic measurement of a resistor value (programmed via ADCIN1\_CUR). The current source is enabled by AD1\_ISRC\_EN. During automatic measurements the enabled current source is dynamically switched off at the end of the conversion and switched on one slot prior to the next ADCIN\_1 measurement (to enable minimum current consumption, and allow any external capacitance voltage to settle); otherwise its status is static.

A similar functionality is available at ADC\_IN2 and ADC\_IN3. ADC\_IN2 provides notification to the processor via a fixed voltage comparator (also available when ADC is powered down) but the ADCIN2 current source is static (no dynamic switch-off at the end of automatic conversion). The input selection switch of ADC\_IN2 provides an enhanced isolation (80 dB typ.) between the externally-connected circuit and the internal ADC block (for example, allowing the DC supervision of noise sensitive audio lines).

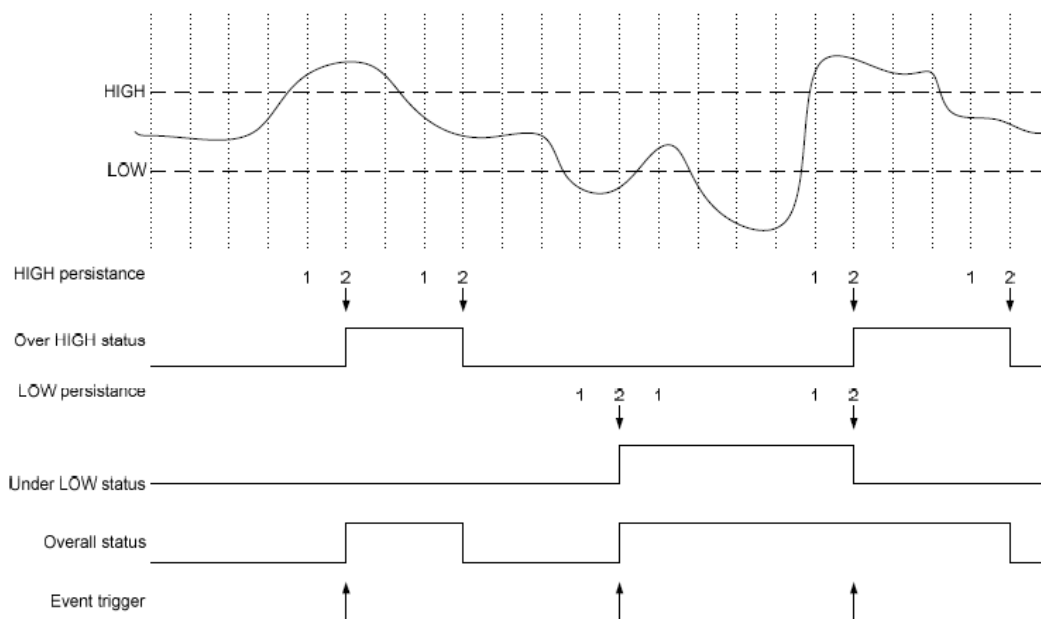


Figure 39: A1, A2, A3 Persistence Behavior

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### 6.13.4.3 A8, A9, A10: Automatic Regulator Monitor with Under- Or Over-Voltage Shutdown

DA9063 provides the capability to monitor the output voltage of internal regulators. In case of a catastrophic failure, the related regulator is disabled. This feature is enabled using control MON\_MODE. Each internal regulator is assigned to a GPADC input channel and can be individually enabled for monitoring via controls BCORE1\_MON\_EN to LDO11\_MON\_EN. For example, if ADC channel A8 is connected to an enabled regulator and it is also enabled for monitoring, the ADC automatically measures the regulator output voltage every 1 ms (10 ms in ADC economy mode). Simultaneously, two relative thresholds are calculated from the regulator nominal output voltage (supporting DVC). If the regulator is out of range, the voltage measurement is stored inside MON\_A8\_RES, the regulator ID is recorded inside the index MON\_A8\_IDX and the event flag E\_REG\_UVOV is set. To secure a stable output voltage, the monitoring is delayed after regulators are switched on and when changing their voltage level to a new target (that is, during DVC slewing, after writing into the active regulator voltage register, or when the active voltage control register is changing between Vxxx\_A and Vxxx\_B). This delay is programmable using control UVOV\_DELAY.

If debouncing is selected via MON\_DEB, an event is only created if two consecutive measurements exceed the same threshold. The feature is also available for channels A9 and A10.

**Table 48: Assignment of Regulators for Voltage Monitoring**

| ADC Channel | Regulator                                                  | Enable                                                                                      |
|-------------|------------------------------------------------------------|---------------------------------------------------------------------------------------------|
| A8          | BUCKCORE1<br>BUCKCORE2<br>BUCKPRO<br>LDO3<br>LDO4<br>LDO11 | BCORE1_MON_EN<br>BCORE2_MON_EN<br>BPRO_MON_EN<br>LDO3_MON_EN<br>LDO4_MON_EN<br>LDO11_MON_EN |
| A9          | BUCKIO<br>BUCKMEM<br>BUCKPERI<br>LDO1<br>LDO2<br>LDO5      | BIO_MON_EN<br>BMEM_MON_EN<br>BPERI_MON_EN<br>LDO1_MON_EN<br>LDO2_MON_EN<br>LDO5_MON_EN      |
| A10         | LDO6<br>LDO7<br>LDO8<br>LDO9<br>LDO10                      | LDO6_MON_EN<br>LDO7_MON_EN<br>LDO8_MON_EN<br>LDO9_MON_EN<br>LDO10_MON_EN                    |

If more than one regulator is assigned to A8, A9, or A10, the regulator measurements are sequentially multiplexed on this channel (elongates the measurement period of 1 ms or 10 ms by each additional assigned regulator). In the case of an E\_REG\_UVOV event, the regulator monitoring continues and shuts down rails facing catastrophic failure (voltage and IDX controls contain information for determining the cause of the most recently detected under- or over-voltage). When clearing E\_REG\_UVOV via a host write, the related regulator index controls are reset. In the unlikely case in which several regulators from a sequenced ADC channel have triggered an under- or over-voltage condition before the host was able to read the related controls, all monitored supplies may be checked for their actual state (enabled or shutdown) to detect if further supplies have also been shut down in addition to the one captured by the index control.

The assertion of nIRQ can be masked by IRQ mask M\_REG\_UVOV. With a masked nIRQ from regulator supervision, the setting of MON\_RES determines whether an out-of-range detection disables the related regulator or triggers the assertion of port nRESET. In the latter case, nRESET is asserted for 1 ms and continues to be asserted until the regulator returns to being in range.

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(regulators that are not enabled but are selected for monitoring do not trigger the assertion of nRESET). With a masked nIRQ, GP\_FB2 can be configured to flag PWR\_OK, indicating that all monitored regulator voltages are in-range. Selecting disabled regulators for monitoring suppresses the assertion of PWR\_OK.

### Note

Voltage monitoring function cannot be used for any LDO in bypass mode.

The regulator monitor unit provides alternative modes selected via MON\_MODE. In measurement-only mode, the event flag E\_REG\_UVOV is set for every automatic measurement result being available on either A8, A9, or A10 (with a maximum of one regulator per channel being enabled for measurements). When enabled, an auto-measurement on A8, A9, or A10 allows the host to get its actual output voltage from registers MON\_A8\_RES to MON\_A10\_RES. When multiple ADC channels are enabled for automatic regulator voltage measurements, the burst measurement mode may reduce the control interface traffic and number of nIRQ assertions. When the ADC time slot of A10 has finished, the event flag E\_REG\_UVOV is set (independent of A10 being enabled for auto-measurements). The host can then read the measurement results stored inside MON\_A8\_RES - MON\_A10\_RES as a block. During measurement modes, there are no threshold comparisons or regulator shutdowns. If the nIRQ line was asserted, automatic measurements on channels A8 (A9 and A10) are paused until the host has cleared the associated event flag (the event-causing value is kept in the result registers). During measurement modes, E\_REG\_UVOV is cleared by writing the read value into register EVENT\_B. To sequentially measure other regulators on ADC input channels A8, A9, and A10, the host has to set the monitor enable for the next measurement slot to the required regulator before clearing the event. The assertion of nIRQ can be masked by IRQ mask M\_REG\_UVOV, which also disables the pausing of automatic measurements. For further information about voltage monitoring, please see DA9063 Voltage Monitoring [2].

### Note

Voltage monitoring function cannot be used for any LDO in bypass mode.

### 6.13.4.4 A4 and A5: Manual Measurement T<sub>J</sub> and V<sub>BBAT</sub>

The 10-bit result of manual measurements is stored in the registers ADC\_RES\_L and ADC\_RES\_H. Channel 4 (T<sub>J</sub>) is used to measure the output of the internal temperature sensor (generated from a proportional to absolute temperature (PTAT) current using a bandgap reference circuit). The ADC measurement result and the T\_OFFSET value can be used by the host to calculate the internal junction temperature, defined by the following formula:

$$T_J [^{\circ}\text{C}] = -0.398 * (\text{ADC} - T\_OFFSET) + 330$$

Channel 5 can be used to measure the voltage of the backup battery.

Manual measurements on A8 to A10 are possible, but require disabling the automatic measurements on these channels and also ensuring that only one regulator is connected to each of these ADC channels.

### NOTE

The T\_OFFSET value is stored in the T\_OFFSET register at address 0x104 during manufacture.

### 6.13.5 Fixed Threshold Comparator

A comparator with a threshold of 1.2 V is connected to the input of ADC channel 2. The comparator is asserted when the input voltage exceeds or drops below 1.2 V for at least 10 ms (debouncing). After being enabled via COMP1V2\_EN, the status flag COMP1V2 indicates the actual state and a maskable interrupt request E\_COMP1V2 is generated at the falling and rising edge state transitions.

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The comparator may be disabled via COMP1V2\_EN when auto-measurements with high resolution are executed on ADCIN2.

### 6.14 Real Time Clock

The RTC circuit maintains the real time clock and alarm functions. The variable RTC supply voltage, VDDRTC, is derived from V<sub>BBAT</sub>. Generally, the RTC block is powered from V<sub>DDREF</sub>, but with RTC\_EN asserted, the DA9063 enters a special low-power RTC mode under the following conditions:

- Unconditionally, when the V<sub>BBAT</sub> (the backup battery supply) is the only available voltage source in the system (no external charger or main battery). DA9063 enters RTC mode automatically since all the other supply domains are down ( $V_{DDREF} < VPOR\_LOWER$ ).
- If the RTC\_MODE\_PD control bit is set (from OTP or host) and the power sequencer reaches slot 0 during a power transition from ACTIVE to POWERDOWN mode. The above condition disables LDOCORE and powers down all blocks (that are unrelated to the RTC circuit operation).
- Similar to the above case, the device goes in to RTC mode if RTC\_MODE\_SD control bit is set (from OTP or host) and the main PM control logic reaches RESET mode in the presence of a V<sub>SYS</sub> fault.

The following conditions (edge sensitive) that re-enable the DA9063's full control logic (terminating RTC mode):

- V<sub>DDREF</sub> rising to > 2.6 V (unconditionally)  
There is no dedicated event bit. A start-up with POR asserted but no asserted E\_WAKE, E\_nONKEY, E\_TICK, or E\_ALARM event bit indicates main battery insertion. Depending on the V<sub>SYS</sub> rise timing and final level, an E\_VDD\_WARN or E\_VDD\_MON wake-up event may be triggered which, if not masked via M\_VDD\_WARN and M\_VDD\_MON in OTP, will cause an application power-up, even when AUTO\_BOOT is cleared in OTP.
- External charger insertion via CHG\_WAKE in the presence of a valid V<sub>DDREF</sub> supply ( $V_{DDREF} > 2.6$  V)
- Assertion of nONKEY in the presence of a valid V<sub>DDREF</sub> supply ( $V_{DDREF} > 2.6$  V)
- Alarm/tick event when there is a valid V<sub>DDREF</sub> supply ( $V_{DDREF} > 2.6$  V; alarm event is otherwise stored in case this condition later becomes true)

The above assertions from nONKEY or CHG\_WAKE must remain until LDOCORE is able to leave the POR state, otherwise the DA9063 relapses back into RTC mode.

#### 6.14.1 32 kHz Oscillator

The clock oscillator circuit is used to drive the RTC. It works with an external piezoelectric oscillator crystal at 32.768 kHz and is enabled via control CRYSTAL. If enabled, the DA9063 biases the crystal when leaving DELIVERY or NO-POWER mode, which starts up the oscillator. By asserting RTC\_EN, the crystal remains biased (the RTC continues to run).

#### Note

When the 32 kHz oscillator is disabled, an external oscillator signal may be applied to port XOUT (the signal is forwarded phase-inverted).

In order to achieve the desired crystal frequency, an external capacitor (10 pF to 20 pF, depending on the parasitic capacitance of the board) should be connected to ground from each of the crystal pins. The start-up time of the oscillator is typically 0.5 s to 1 s. The XTAL pins should be grounded when the crystal is not mounted and when not being driven by an external oscillator signal. The 32 kHz clock signal is available at the OUT\_32K port and the buffer can be enabled/disabled from

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the host via control EN\_32KOUT. The 32 kHz signal can also be made available at GP\_FB3 (enabled via control PM\_FB3\_PIN).

### 6.14.1.1 First Power-Up Sequencing after Enable of 32 kHz Oscillator (ID EN32K\_STEP)

When the oscillator is enabled (when asserting control CRYSTAL, or when leaving DELIVERY or NO-POWER mode with CRYSTAL already asserted), OUT\_CLOCK determines whether the clock provision at OUT\_32K (GP\_FB3) is gated by a timer. This enables the clock output only when the oscillator signal has become stable. The control RTC\_CLOCK provides a similar gating function prior to the clock signal being fed into the internal RTC counter. The stabilization timer (configured via STABILIZATION\_TIME) can either be started immediately or be configured to wait until the clock's duty cycle is within the range 30-70% (selected via DELAY\_MODE). When powering up before the stabilization timer has expired, ID EN32K\_STEP forces the sequencer to wait for timer expiry, which allows a correlation of the 32 kHz signal being provided to outputs with other power up actions following the enable of the 32 kHz oscillator. When reaching ID EN32K\_STEP with OUT\_CLOCK being released, the gating of the 32 kHz signal is terminated immediately. ID EN32K\_STEP is not processed by the sequencer powering-down, nor during consecutive sequencing powering-up.

### 6.14.1.2 Other Power-Up and -Down Sequencing (ID PD\_DIS\_STEP)

If the power sequence does not contain the sequencer ID EN32K\_STEP, the control OUT\_32K\_PAUSE from ID PD\_DIS\_STEP can be used to control the dedicated clock output port OUT\_32K in relation to other sequencer actions when powering up and down. The same is true for any sequencing following the first signal provision to port OUT\_32K in case the power sequence contains ID EN32K\_STEP.

Clearing control crystal enables the provision of the 32 kHz signal from an external clock source connected to the XOUT pin, see [Table 49](#). The provision of external clock signals is not timing controlled and the sequencer ID EN\_32K immediately progresses in this case. The crystal input pins can withstand leakage currents corresponding to connected resistances at least as low as 10 MΩ, connected between the pin and any signal level between  $V_{DDREF}$  and GND.

**Table 49: 32 kHz Oscillator Modes**

| Power Mode | Conditions                                                    | $V_{DDREF}$ | $V_{BBAT}$ | VDDCORE                     | RTC_EN | CRYSTAL | RTC clock | OUT_32K |
|------------|---------------------------------------------------------------|-------------|------------|-----------------------------|--------|---------|-----------|---------|
| NO-POWER   | No operation, supplies < ~2V                                  | 0           | 0          | 0                           | x      | x       | -         | -       |
| DELIVERY   | No operation, though powered                                  | 0           | 1          | 0                           | 0      | x       | -         | -       |
|            |                                                               | 1           | x          | 0<br><a href="#">Note 1</a> | 0      | x       | -         | -       |
| RTC        | Only RTC and Alarm operating from external clock              | 1           | x          | 0<br><a href="#">Note 1</a> | 1      | 0       | EXT       | -       |
|            |                                                               | x           | 1          |                             |        |         |           |         |
|            | Only RTC and Alarm operating from internal crystal oscillator | 1           | x          | 0<br><a href="#">Note 1</a> | 1      | 1       | OSC       | -       |
|            |                                                               | x           | 1          |                             |        |         |           |         |

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| Power Mode | Conditions                                                                  | V <sub>DDREF</sub> | V <sub>BBAT</sub> | V <sub>DDCORE</sub> | RTC_EN | CRYSTAL | RTC clock | OUT_32K       |
|------------|-----------------------------------------------------------------------------|--------------------|-------------------|---------------------|--------|---------|-----------|---------------|
| ACTIVE     | Half-current operation, RTC and alarm off using external clock              | 1                  | x                 | 1<br>Note 2         | 0      | 0       | -         | EXT           |
|            | Half-current operation, RTC and alarm on using external clock               | 1                  | x                 | 1<br>Note 3         | 1      | 0       | EXT       | EXT           |
|            | Half-current operation, RTC and alarm off using internal crystal oscillator | 1                  | x                 | 1<br>Note 2         | 0      | 1       | -         | OSC<br>Note 4 |
|            | Half-current operation, RTC and alarm on using internal crystal oscillator  | 1                  | x                 | 1<br>Note 3         | 1      | 1       | OSC       | OSC           |

**Note 1** Requires nOFF or nSHUTDOWN to be asserted during V<sub>DDREF</sub> rising, or a power-down transition from ACTIVE mode with RTC\_MODE\_PD or RTC\_MODE\_SD being enabled

**Note 2** Triggered from nONKEY press, assertion of CHG\_WAKE or V<sub>DDREF</sub> rising towards > 2.6 V

**Note 3** Triggered from nONKEY press, assertion of CHG\_WAKE, alarm/tick event or V<sub>DDREF</sub> rising towards > 2.6 V

**Note 4** RTC\_EN = 0 causes an initially unstable clock signal when entering half-current mode

The timekeeping error from the frequency variance of crystal oscillators (typ. ±20 ppm) can be trimmed individually during the application end test via the OTP-programmable register TRIM\_CLDR by ± 242 ppm with a resolution of 1.9 ppm (1/[32768 \* 16]). More advanced solutions can dynamically correct even the temperature related oscillator frequency drift (> 100 ppm) using a periodic temperature measurement located close to the crystal. The timekeeping correction is applied only to the RTC calendar counter. Because of potential clock jitter issues, the 32 kHz clock signal at the OUT\_32K pin provides the original frequency of the crystal.

### 6.14.2 RTC Counter and Alarm

The RTC counter counts the number of 32 kHz clock periods, providing a sec, min, hrs, day, month, and year output. Year 0 corresponds to 2000. It is able to count up to 63 years. The value of the RTC calendar is read-/write-able via the power manager communication. A read of COUNT\_S (seconds) latches the current RTC calendar count into the registers COUNT\_S through to COUNT\_Y (coherent for approx. 0.5 s), so to obtain an updated calendar value requires a read of COUNT\_S. Registers are only valid when RTC\_READ status bit is asserted (assertion may take several milliseconds from leaving POR).

There is an alarm register containing sec, min, hrs, day, month, and year. When the RTC counter register value corresponds to the value set in the alarm, an IRQ event is triggered and a wake-up is triggered if the DA9063 is in POWERDOWN mode. The trigger also sets a bit in an event register to notify that an alarm has occurred. The alarm can alternatively be asserted from a periodic 'tick' signal that, depending on control TICK\_TYPE, is either asserted every second or minute.

#### Note

After modifying TICK\_TYPE or TICK\_WAKE, a write to register ALARM\_Y is required to activate the new settings.

The power manager controls, ALARM\_ON and TICK\_ON, enable/disable the alarm and tick.

The power manager register bit MONITOR is set to 0 each time the RTC is powered up. Software should set this bit to 1 when setting the time and date which allows software to detect a subsequent

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loss of the clock. Values written into the RTC calendar and alarm registers must be valid for the associated units of calendar time, for example less than 60 for second and minute registers, see register description for further details.

The RTC registers SECOND\_A to SECOND\_D define a 32-bit seconds counter (approx. 136 years) that can only be reset after powering up from NO-POWER mode. A read of SECOND\_A (seconds counter LSBs) latches the full 32-bit counter into the registers SECOND\_A to SECOND\_D (coherent for approx. 0.5 s), so that receiving an updated counter value requires a read of SECOND\_A. After MONITOR has been set, any host write to CRYSTAL and RTC\_EN is prohibited to ensure that the SECOND\_A to SECOND\_D counters are never stopped.

### 6.15 Adjustable Frequency Internal Oscillator

An internal oscillator provides a nominal 6.0 MHz clock that is divided down to 3.0 MHz for the buck converters. It is divided down to control the digital core, timers, PWM units, charge pump and ADC. The frequency of the internal oscillator is adjusted during the initial start-up sequence of the DA9063 to within 5 % of the nominal 6.0 MHz. It can be adjusted further within  $\pm 10\%$  via register control OSC\_FRQ. The tolerance of this frequency affects most absolute timer values and PWM repetition rates (for example, LED and vibrator mode drivers) of the DA9063.

### 6.16 Reference Voltage Generation: VREF, VLNREF

The DA9063 includes a temperature-independent voltage reference circuit which is derived from an internal band-gap reference and OTP-trimmed buffer amplifier. The output voltage on VREF is trimmed to 1.2 V and the reference is decoupled by an external capacitor on the VREF pin. A lower voltage instance of VREF is provided at VLNREF (0.9 V) and used for the LDOs. These pins must not be loaded. The IREF pin provides the internally used accurate current bias and requires an external 200 k $\Omega$  precision resistor.

### 6.17 Thermal Supervision

The application must ensure that the DA9063 junction temperature does not exceed 125 °C. To protect the DA9063 from damage due to excessive power dissipation, the internal temperature is continuously monitored. Whenever the junction temperature is higher than TEMP\_WARN = 125 °C, an E\_TEMP event is asserted and an IRQ is generated for the host. If this occurs during POWERDOWN mode, a wake-up is triggered.

The host may then check the exact junction temperature by a manual measurement on GPADC channel 4. An 8-bit OTP register (T\_OFFSET) can be used to store its offset at a known temperature (for example 50 °C) to improve the absolute accuracy, which should then be  $\pm 7$  °C of the measured silicon die junction temperature. This T\_OFFSET can be used by the host to calculate the absolute die temperature.

The absolute die junction temperature can be calculated by the host using the result from the ADC channel 4 measurement result and the T\_OFFSET trim values.

When the junction temperature exceeds 125 °C, it is recommended to shut down optional functions of the application allowing the DA9063 to cool. When the junction temperature increases further, exceeding TEMP\_CRIT = 140 °C, the fault flag TEMP\_CRIT is asserted in the FAULT\_LOG register and the DA9063 immediately shuts down to RESET mode. The fault condition remains as long as the junction temperature is higher than TEMP\_WARN. The TEMP\_CRIT flag can be evaluated by the application after the next power up. Whenever the junction temperature exceeds TEMP\_POR = 150 °C, a POR to the digital core is immediately asserted and this stops all functions of the DA9063 except for the RTC. This is necessary to prevent the possibility of permanent device damage.

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### 6.18 Main System Rail Voltage Supervision

Two comparators supervise the system supply  $V_{SYS}$ . One is monitoring the under-voltage level ( $V_{DD\_FAULT\_LOWER}$ ) and the other is indicating a good system supply ( $V_{DD\_FAULT\_UPPER}$ ). The  $V_{DD\_FAULT\_LOWER}$  threshold is OTP configurable and can be set via the  $V_{DD\_FAULT\_ADJ}$  register from 2.5 V to 3.25 V in 50 mV steps. The  $V_{DD\_FAULT\_UPPER}$  threshold is also OTP configurable and can be set via the  $V_{DD\_HYST\_ADJ}$  register from 100 mV to 450 mV higher than the  $V_{DD\_FAULT\_LOWER}$  threshold.  $V_{SYS}$  dropping below the  $V_{DD\_FAULT\_UPPER}$  threshold asserts the event  $E\_VDD\_WARN$ . If the event is not masked, this issues an interrupt, which can be used by the host processor as an indication to decrease its activity.

If  $V_{SYS}$  drops below  $V_{DD\_FAULT\_LOWER}$  for more than 100 ms, the supply error flag  $V_{DD\_FAULT}$  (in register  $FAULT\_LOG$ ) is asserted and a shutdown sequence to RESET mode is triggered, see Section 6.2.3. The  $nRESET$  output is asserted at the beginning of the shutdown sequence. The status can also be reported using a dedicated  $nV_{DD\_FAULT}$  signal, see Section 6.1.11.

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### 7 Register Map

This section provides an overview of the registers. A description of each register is provided in 11.

| Hex                                         | Register   | 7               | 6           | 5          | 4           | 3         | 2              | 1            | 0           |
|---------------------------------------------|------------|-----------------|-------------|------------|-------------|-----------|----------------|--------------|-------------|
| PAGE 0                                      |            |                 |             |            |             |           |                |              |             |
| 00                                          | PAGE_CON   | Revert          | WRITE_MODE  | Reserved   |             |           | REG_PAGE       |              |             |
| System Control and Event Registers (SYSMON) |            |                 |             |            |             |           |                |              |             |
| 01                                          | STATUS_A   | Reserved        |             |            |             | COMP1V2   | DVC_BUSY       | WAKE         | nONKEY      |
| 02                                          | STATUS_B   | GPI7            | GPI6        | GPI5       | GPI4        | GPI3      | GPI2           | GPI1         | GPI0        |
| 03                                          | STATUS_C   | GPI15           | GPI14       | GPI13      | GPI12       | GPI11     | GPI10          | GPI9         | GPI8        |
| 04                                          | STATUS_D   | LDO11_LIM       | LDO8_LIM    | LDO7_LIM   | LDO4_LIM    | LDO3_LIM  | Reserved       |              |             |
| 05                                          | FAULT_LOG  | WAIT_SHUT       | nSHUTDOWN   | KEY_RESET  | TEMP_CRIT   | VDD_START | VDD_FAULT      | POR          | TWD_ERROR   |
| 06                                          | EVENT_A    | EVENTS_D        | EVENTS_C    | EVENTS_B   | E_SEQ_RDY   | E_ADC_RDY | E_TICK         | E_ALARM      | E_nONKEY    |
| 07                                          | EVENT_B    | E_VDD_WARN      | E_VDD_MON   | E_DVC_RDY  | E_REG_UVOV  | E_LDO_LIM | E_COMP_1V2     | E_TEMP       | E_WAKE      |
| 08                                          | EVENT_C    | E_GPI7          | E_GPI6      | E_GPI5     | E_GPI4      | E_GPI3    | E_GPI2         | E_GPI1       | E_GPI0      |
| 09                                          | EVENT_D    | E_GPI15         | E_GPI14     | E_GPI13    | E_GPI12     | E_GPI11   | E_GPI10        | E_GPI9       | E_GPI8      |
| 0A                                          | IRQ_MASK_A | Reserved        |             |            | M_SEQ_RDY   | M_ADC_RDY | M_TICK         | M_ALARM      | M_nONKEY    |
| 0B                                          | IRQ_MASK_B | M_VDD_WARN      | M_VDD_MON   | M_DVC_RDY  | M_REG_UVOV  | M_LDO_LIM | M_COMP_1V2     | M_TEMP       | M_WAKE      |
| 0C                                          | IRQ_MASK_C | M_GPI7          | M_GPI6      | M_GPI5     | M_GPI4      | M_GPI3    | M_GPI2         | M_GPI1       | M_GPI0      |
| 0D                                          | IRQ_MASK_D | M_GPI15         | M_GPI14     | M_GPI13    | M_GPI12     | M_GPI11   | M_GPI10        | M_GPI9       | M_GPI8      |
| 0E                                          | CONTROL_A  | CP_EN           | M_POWER1_EN | M_POWER_EN | M_SYSTEM_EN | STANDBY   | POWER1_EN      | POWER_EN     | SYSTEM_EN   |
| 0F                                          | CONTROL_B  | BUCK_SLOWS_TART | Reserved    |            | nONKEY_LOCK | nRES_MODE | RESET_BLINKING | WATCHDOG_DIS | CHG_SEL     |
| 10                                          | CONTROL_C  | DEF_SUPPLY      | SLEW_RATE   |            | OTPREAD_EN  | AUTO_BOOT | DEBOUNCING     |              |             |
| 11                                          | CONTROL_D  | BLINK_DUR       |             | BLINK_FRQ  |             |           | TWDSCALE       |              |             |
| 12                                          | CONTROL_E  | V_LOCK          | PM_FB3_PIN  | PM_FB2_PIN | PM_FB1_PIN  | ECO_MODE  | RTC_EN         | RTC_MODE_SD  | RTC_MODE_PD |

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| Hex                               | Register      | 7            | 6            | 5           | 4           | 3           | 2           | 1            | 0          |
|-----------------------------------|---------------|--------------|--------------|-------------|-------------|-------------|-------------|--------------|------------|
| 13                                | CONTROL_F     | Reserved     |              |             |             |             | WAKE_UP     | SHUTDOWN     | WATCHDOG   |
| 14                                | PD_DIS        | PMCONT_DIS   | OUT32K_PAUSE | BBAT_DIS    | Reserved    | HS2IF_DIS   | PMIF_DIS    | GPADC_PAUSE  | GPI_DIS    |
| GPIO Control Registers (GPIO)     |               |              |              |             |             |             |             |              |            |
| 15                                | GPIO0-1       | GPIO1_WEN    | GPIO1_TYPE   | GPIO1_P IN  |             | GPIO0_WEN   | GPIO0_TYPE  | GPIO0_P IN   |            |
| 16                                | GPIO2-3       | GPIO3_WEN    | GPIO3_TYPE   | GPIO3_P IN  |             | GPIO2_WEN   | GPIO2_TYPE  | GPIO2_P IN   |            |
| 17                                | GPIO4-5       | GPIO5_WEN    | GPIO5_TYPE   | GPIO5_P IN  |             | GPIO4_WEN   | GPIO4_TYPE  | GPIO4_P IN   |            |
| 18                                | GPIO6-7       | GPIO7_WEN    | GPIO7_TYPE   | GPIO7_P IN  |             | GPIO6_WEN   | GPIO6_TYPE  | GPIO6_P IN   |            |
| 19                                | GPIO8-9       | GPIO9_WEN    | GPIO9_TYPE   | GPIO9_P IN  |             | GPIO8_WEN   | GPIO8_TYPE  | GPIO8_P IN   |            |
| 1A                                | GPIO10-11     | GPIO11_WEN   | GPIO11_TYPE  | GPIO11_P IN |             | GPIO10_WEN  | GPIO10_TYPE | GPIO10_P IN  |            |
| 1B                                | GPIO12-13     | GPIO13_WEN   | GPIO13_TYPE  | GPIO13_P IN |             | GPIO12_WEN  | GPIO12_TYPE | GPIO12_P IN  |            |
| 1C                                | GPIO14-15     | GPIO15_WEN   | GPIO15_TYPE  | GPIO15_P IN |             | GPIO14_WEN  | GPIO14_TYPE | GPIO14_P IN  |            |
| 1D                                | GPIO_MODE0-7  | GPIO7_MODE   | GPIO6_MODE   | GPIO5_MODE  | GPIO4_MODE  | GPIO3_MODE  | GPIO2_MODE  | GPIO1_MODE   | GPIO0_MODE |
| 1E                                | GPIO_MODE8-15 | GPIO15_MODE  | GPIO14_MODE  | GPIO13_MODE | GPIO12_MODE | GPIO11_MODE | GPIO10_MODE | GPIO9_MODE   | GPIO8_MODE |
| 1F                                | SWITCH_CONT   | CP_EN_MODE   | CORE_SW_INT  | SWITCH_SR   |             |             |             | CORE_SW_GP I |            |
| Regulator Control Registers (REG) |               |              |              |             |             |             |             |              |            |
| 20                                | BCORE2_CONT   | Reserved     | VBCORE2_GPI  |             | Reserved    | BCORE2_CONF | BCORE2_GPI  |              | BCORE2_EN  |
| 21                                | BCORE1_CONT   | CORE_SW_CONF | VBCORE1_GPI  |             | CORE_SW_EN  | BCORE1_CONF | BCORE1_GPI  |              | BCORE1_EN  |
| 22                                | BPRO_CONT     | Reserved     | VBPRO_GPI    |             | Reserved    | BPRO_CONF   | BPRO_GPI    |              | BPRO_EN    |
| 23                                | BMEM_CONT     | Reserved     | VBMEM_GPI    |             | Reserved    | BMEM_CONF   | BMEM_GPI    |              | BMEM_EN    |
| 24                                | BIO_CONT      | Reserved     | VBIO_GPI     |             | Reserved    | BIO_CONF    | BIO_GPI     |              | BIO_EN     |
| 25                                | BPERI_CONT    | PERI_SW_CONF | BPERI_GP I   |             | PERI_SW_EN  | BPERI_CONF  | PERI_SW_GPI |              | BPERI_EN   |
| 26                                | LDO1_CONT     | LDO1_CONF    | VLDO1_GPI    |             | Reserved    | LDO1_PD_DIS | LDO1_GPI    |              | LDO1_EN    |
| 27                                | LDO2_CONT     | LDO2_CONF    | VLDO2_GPI    |             | Reserved    | LDO2_PD_DIS | LDO2_GPI    |              | LDO2_EN    |

## System PMIC for Mobile and Automotive Applications

| Hex                              | Register   | 7           | 6           | 5           | 4           | 3            | 2           | 1           | 0            |
|----------------------------------|------------|-------------|-------------|-------------|-------------|--------------|-------------|-------------|--------------|
| 28                               | LDO3_CONT  | LDO3_CONF   | VLDO3_GPI   |             | Reserved    | LDO3_PD_DIS  | LDO3_GPI    |             | LDO3_EN      |
| 29                               | LDO4_CONT  | LDO4_CONF   | VLDO4_GPI   |             | Reserved    | LDO4_PD_DIS  | LDO4_GPI    |             | LDO4_EN      |
| 2A                               | LDO5_CONT  | LDO5_CONF   | VLDO5_GPI   |             | VLDO5_SEL   | LDO5_PD_DIS  | LDO5_GPI    |             | LDO5_EN      |
| 2B                               | LDO6_CONT  | LDO6_CONF   | VLDO6_GPI   |             | VLDO6_SEL   | LDO6_PD_DIS  | LDO6_GPI    |             | LDO6_EN      |
| 2C                               | LDO7_CONT  | LDO7_CONF   | VLDO7_GPI   |             | VLDO7_SEL   | LDO7_PD_DIS  | LDO7_GPI    |             | LDO7_EN      |
| 2D                               | LDO8_CONT  | LDO8_CONF   | VLDO8_GPI   |             | VLDO8_SEL   | LDO8_PD_DIS  | LDO8_GPI    |             | LDO8_EN      |
| 2E                               | LDO9_CONT  | LDO9_CONF   | VLDO9_GPI   |             | VLDO9_SEL   | LDO9_PD_DIS  | LDO9_GPI    |             | LDO9_EN      |
| 2F                               | LDO10_CONT | LDO10_CONF  | VLDO10_GPI  |             | VLDO10_SEL  | LDO10_PD_DIS | LDO10_GPI   |             | LDO10_EN     |
| 30                               | LDO11_CONT | LDO11_CONF  | VLDO11_GPI  |             | VLDO11_SEL  | LDO11_PD_DIS | LDO11_GPI   |             | LDO11_EN     |
| 31                               | VIB        | Reserved    |             | VIB_SET     |             |              |             |             |              |
| 32                               | DVC_1      | VLDO3_SEL   | VLDO2_SEL   | VLDO1_SEL   | VBPERI_SEL  | VBMEM_SEL    | VBPRO_SEL   | VBCORE2_SEL | VBCORE1_SEL  |
| 33                               | DVC_2      | VLDO4_SEL   | Reserved    |             |             |              |             |             | VBIO_SEL     |
| GP-ADC Control Registers (GPADC) |            |             |             |             |             |              |             |             |              |
| 34                               | ADC_MAN    | Reserved    | Reserved    | ADC_MODE    | ADC_MAN     | ADC_M UX     |             |             |              |
| 35                               | ADC_CONT   | COMP1V2_EN  | AD3_ISRC_EN | AD2_ISRC_EN | AD1_ISRC_EN | AUTO_AD3_EN  | AUTO_AD2_EN | AUTO_AD1_EN | AUTO_VSYS_EN |
| 36                               | VSYS_MON   | VSYS_MON    |             |             |             |              |             |             |              |
| 37                               | ADC_RES_L  | ADC_RES_LSB |             | Reserved    |             |              |             |             |              |
| 38                               | ADC_RES_H  | ADC_RES_H   |             |             |             |              |             |             |              |
| 39                               | VSYS_RES   | VSYS_RES    |             |             |             |              |             |             |              |
| 3A                               | ADCIN1_RES | ADCIN1_RES  |             |             |             |              |             |             |              |
| 3B                               | ADCIN2_RES | ADCIN2_RES  |             |             |             |              |             |             |              |
| 3C                               | ADCIN3_RES | ADCIN3_RES  |             |             |             |              |             |             |              |
| 3D                               | MON_A8_RES | MON_A8_RES  |             |             |             |              |             |             |              |
| 3E                               | MON_A9_RES | MON_A9_RES  |             |             |             |              |             |             |              |

## System PMIC for Mobile and Automotive Applications

| Hex                                         | Register    | 7           | 6        | 5          | 4          | 3           | 2 | 1 | 0 |
|---------------------------------------------|-------------|-------------|----------|------------|------------|-------------|---|---|---|
| 3F                                          | MON_A10_RES | MON_A10_RES |          |            |            |             |   |   |   |
| RTC Calendar and Alarm Registers (RTC)      |             |             |          |            |            |             |   |   |   |
| 40                                          | COUNT_S     | RTC_READ    | Reserved | COUNT_SEC  |            |             |   |   |   |
| 41                                          | COUNT_MI    | Reserved    |          | COUNT_MIN  |            |             |   |   |   |
| 42                                          | COUNT_H     | Reserved    |          |            | COUNT_HOUR |             |   |   |   |
| 43                                          | COUNT_D     | Reserved    |          |            | COUNT_DAY  |             |   |   |   |
| 44                                          | COUNT_MO    | Reserved    |          |            |            | COUNT_MONTH |   |   |   |
| 45                                          | COUNT_Y     | Reserved    | MONITOR  | COUNT_YEAR |            |             |   |   |   |
| 46                                          | ALARM_S     | ALARM_TYPE  |          | ALARM_SEC  |            |             |   |   |   |
| 47                                          | ALARM_MI    | Reserved    |          | ALARM_MIN  |            |             |   |   |   |
| 48                                          | ALARM_H     | Reserved    |          |            | ALARM_HOUR |             |   |   |   |
| 49                                          | ALARM_D     | Reserved    |          |            | ALARM_DAY  |             |   |   |   |
| 4A                                          | ALARM_MO    | Reserved    |          | TICK_WAKE  | TICK_TYPE  | ALARM_MONTH |   |   |   |
| 4B                                          | ALARM_Y     | TICK_ON     | ALARM_ON | ALARM_YEAR |            |             |   |   |   |
| System Control and Event Registers (SYSMON) |             |             |          |            |            |             |   |   |   |
| 4C                                          | SECOND_A    | SECONDS_A   |          |            |            |             |   |   |   |
| 4D                                          | SECOND_B    | SECONDS_B   |          |            |            |             |   |   |   |
| 4E                                          | SECOND_C    | SECONDS_C   |          |            |            |             |   |   |   |
| 4F                                          | SECOND_D    | SECONDS_D   |          |            |            |             |   |   |   |

## System PMIC for Mobile and Automotive Applications

| Hex                               | Register  | 7              | 6          | 5        | 4 | 3              | 2        | 1 | 0 |
|-----------------------------------|-----------|----------------|------------|----------|---|----------------|----------|---|---|
| PAGE 1                            |           |                |            |          |   |                |          |   |   |
| 80                                | PAGE_CON  | Revert         | WRITE_MODE | Reserved |   |                | REG_PAGE |   |   |
| Sequencer Control Registers (SEQ) |           |                |            |          |   |                |          |   |   |
| 81                                | SEQ       | NXT_SEQ_START  |            |          |   | SEQ_POINTER    |          |   |   |
| 82                                | SEQ_TIMER | SEQ_DUMM       |            |          |   | SEQ_TIME       |          |   |   |
| 83                                | ID_2_1    | LDO2_STEP      |            |          |   | LDO1_STEP      |          |   |   |
| 84                                | ID_4_3    | LDO4_STEP      |            |          |   | LDO3_STEP      |          |   |   |
| 85                                | ID_6_5    | LDO6_STEP      |            |          |   | LDO5_STEP      |          |   |   |
| 86                                | ID_8_7    | LDO8_STEP      |            |          |   | LDO7_STEP      |          |   |   |
| 87                                | ID_10_9   | LDO10_STEP     |            |          |   | LDO9_STEP      |          |   |   |
| 88                                | ID_12_11  | PD_DIS_STEP    |            |          |   | LDO11_STEP     |          |   |   |
| 89                                | ID_14_13  | BUCKCORE2_STEP |            |          |   | BUCKCORE1_STEP |          |   |   |
| 8A                                | ID_16_15  | BUCKIO_STEP    |            |          |   | BUCKPRO_STEP   |          |   |   |
| 8B                                | ID_18_17  | BUCKPERI_STEP  |            |          |   | BUCKMEM_STEP   |          |   |   |
| 8C                                | ID_20_19  | PERI_SW_STEP   |            |          |   | CORE_SW_STEP   |          |   |   |
| 8D                                | ID_22_21  | GP_FALL1_STEP  |            |          |   | GP_RISE1_STEP  |          |   |   |
| 8E                                | ID_24_23  | GP_FALL2_STEP  |            |          |   | GP_RISE2_STEP  |          |   |   |
| 8F                                | ID_26_25  | GP_FALL3_STEP  |            |          |   | GP_RISE3_STEP  |          |   |   |
| 90                                | ID_28_27  | GP_FALL4_STEP  |            |          |   | GP_RISE4_STEP  |          |   |   |
| 91                                | ID_30_29  | GP_FALL5_STEP  |            |          |   | GP_RISE5_STEP  |          |   |   |
| 92                                | ID_32_31  | EN32K_STEP     |            |          |   | WAIT_STEP      |          |   |   |
| 93                                | RESERVED  | Reserved       |            |          |   | Reserved       |          |   |   |
| 94                                | RESERVED  | Reserved       |            |          |   | Reserved       |          |   |   |
| 95                                | SEQ_A     | POWER_END      |            |          |   | SYSTEM_END     |          |   |   |

## System PMIC for Mobile and Automotive Applications

| Hex                               | Register    | 7           | 6         | 5            | 4           | 3            | 2                  | 1 | 0 |
|-----------------------------------|-------------|-------------|-----------|--------------|-------------|--------------|--------------------|---|---|
| 96                                | SEQ_B       | PART_DOWN   |           |              |             | MAX_COUNT    |                    |   |   |
| 97                                | WAIT        | WAIT_DIR    |           | TIME_OUT     | WAIT_MODE   | WAIT_TIME    |                    |   |   |
| 98                                | EN_32K      | OUT_32K_EN  | RTC_CLOCK | OUT_CLOCK    | DELAY_MODE  | CRYSTAL      | STABILIZATION_TIME |   |   |
| 99                                | RESET       | RESET_EVENT |           | RESET_TIMER  |             |              |                    |   |   |
| Regulator Setting Registers (REG) |             |             |           |              |             |              |                    |   |   |
| 9A                                | BUCK_ILIM_A | BMEM_ILIM   |           |              |             | BIO_ILIM     |                    |   |   |
| 9B                                | BUCK_ILIM_B | BPERI_ILIM  |           |              |             | BPRO_ILIM    |                    |   |   |
| 9C                                | BUCK_ILIM_C | BCORE2_ILIM |           |              |             | BCORE1_ILIM  |                    |   |   |
| 9D                                | BCORE2_CONF | BCORE2_MODE |           | BCORE2_PD_DS | Reserved    |              | BCORE2_FB          |   |   |
| 9E                                | BCORE1_CONF | BCORE1_MODE |           | BCORE1_PD_DS | Reserved    |              | BCORE1_FB          |   |   |
| 9F                                | BPRO_CONF   | BPRO_MODE   |           | BPRO_PD_DIS  | BPRO_VTT_EN | BPRO_VTTR_EN | BPRO_FB            |   |   |
| A0                                | BIO_CONF    | BIO_MODE    |           | BIO_PD_DIS   | Reserved    |              | BIO_FB             |   |   |
| A1                                | BMEM_CONF   | BMEM_MODE   |           | BMEM_PD_DIS  | Reserved    |              | BMEM_FB            |   |   |
| A2                                | BPERI_CONF  | BPERI_MODE  |           | BPERI_PD_DIS | Reserved    |              | BPERI_FB           |   |   |
| A3                                | VBCORE2_A   | BCORE2_SL_A | VBCORE2_A |              |             |              |                    |   |   |
| A4                                | VBCORE1_A   | BCORE1_SL_A | VBCORE1_A |              |             |              |                    |   |   |
| A5                                | VBPRO_A     | BCPRO_SL_A  | VBPRO_A   |              |             |              |                    |   |   |
| A6                                | VBMEM_A     | BMEM_SL_A   | VBMEM_A   |              |             |              |                    |   |   |
| A7                                | VBIO_A      | BIO_SL_A    | VBIO_A    |              |             |              |                    |   |   |
| A8                                | VBPERI_A    | BPERI_SL_A  | VBPERI_A  |              |             |              |                    |   |   |
| A9                                | VLDO1_A     | LDO1_SL_A   | Reserved  | VLDO1_A      |             |              |                    |   |   |
| AA                                | VLDO2_A     | LDO2_SL_A   | Reserved  | VLDO2_A      |             |              |                    |   |   |
| AB                                | VLDO3_A     | LDO3_SL_A   | VLDO3_A   |              |             |              |                    |   |   |

## System PMIC for Mobile and Automotive Applications

| Hex | Register  | 7           | 6         | 5        | 4 | 3 | 2 | 1 | 0 |
|-----|-----------|-------------|-----------|----------|---|---|---|---|---|
| AC  | VLDO4_A   | LDO4_SL_A   | VLDO4_A   |          |   |   |   |   |   |
| AD  | VLDO5_A   | LDO5_SL_A   | Reserved  | VLDO5_A  |   |   |   |   |   |
| AE  | VLDO6_A   | LDO6_SL_A   | Reserved  | VLDO6_A  |   |   |   |   |   |
| AF  | VLDO7_A   | LDO7_SL_A   | Reserved  | VLDO7_A  |   |   |   |   |   |
| B0  | VLDO8_A   | LDO8_SL_A   | Reserved  | VLDO8_A  |   |   |   |   |   |
| B1  | VLDO9_A   | LDO9_SL_A   | Reserved  | VLDO9_A  |   |   |   |   |   |
| B2  | VLDO10_A  | LDO10_SL_A  | Reserved  | VLDO10_A |   |   |   |   |   |
| B3  | VLDO11_A  | LDO11_SL_A  | Reserved  | VLDO11_A |   |   |   |   |   |
| B4  | VBCORE2_B | BCORE2_SL_B | VBCORE2_B |          |   |   |   |   |   |
| B5  | VBCORE1_B | BCORE1_SL_B | VBCORE1_B |          |   |   |   |   |   |
| B6  | VBPRO_B   | BCPRO_SL_B  | VBPRO_B   |          |   |   |   |   |   |
| B7  | VBMEM_B   | BMEM_SL_B   | VBMEM_B   |          |   |   |   |   |   |
| B8  | VBIO_B    | BIO_SL_B    | VBIO_B    |          |   |   |   |   |   |
| B9  | VBPERI_B  | BPERI_SL_B  | VBPERI_B  |          |   |   |   |   |   |
| BA  | VLDO1_B   | LDO1_SL_B   | Reserved  | VLDO1_B  |   |   |   |   |   |
| BB  | VLDO2_B   | LDO2_SL_B   | Reserved  | VLDO2_B  |   |   |   |   |   |
| BC  | VLDO3_B   | LDO3_SL_B   | VLDO3_B   |          |   |   |   |   |   |
| BD  | VLDO4_B   | LDO4_SL_B   | VLDO4_B   |          |   |   |   |   |   |
| BE  | VLDO5_B   | LDO5_SL_B   | Reserved  | VLDO5_B  |   |   |   |   |   |
| BF  | VLDO6_B   | LDO6_SL_B   | Reserved  | VLDO6_B  |   |   |   |   |   |
| C0  | VLDO7_B   | LDO7_SL_B   | Reserved  | VLDO7_B  |   |   |   |   |   |
| C1  | VLDO8_B   | LDO8_SL_B   | Reserved  | VLDO8_B  |   |   |   |   |   |
| C2  | VLDO9_B   | LDO9_SL_B   | Reserved  | VLDO9_B  |   |   |   |   |   |
| C3  | VLDO10_B  | LDO10_SL_B  | Reserved  | VLDO10_B |   |   |   |   |   |

## System PMIC for Mobile and Automotive Applications

| Hex                                            | Register   | 7          | 6          | 5          | 4          | 3          | 2 | 1          | 0 |
|------------------------------------------------|------------|------------|------------|------------|------------|------------|---|------------|---|
| C4                                             | VLDO11_B   | LDO11_SL_B | Reserved   | VLDO11_B   |            |            |   |            |   |
| Backup Battery Charger Control Register (BBAT) |            |            |            |            |            |            |   |            |   |
| C5                                             | BBAT_CONT  | BCHG_ISET  |            |            |            | BCHG_VSET  |   |            |   |
| GPIO PWM (LED)                                 |            |            |            |            |            |            |   |            |   |
| C6                                             | GPO11_LED  | GPO11_DIM  | GPO11_PWM  |            |            |            |   |            |   |
| C7                                             | GPO14_LED  | GPO14_DIM  | GPO14_PWM  |            |            |            |   |            |   |
| C8                                             | GPO15_LED  | GPO15_DIM  | GPO15_PWM  |            |            |            |   |            |   |
| GP-ADC Threshold Registers (GPADC)             |            |            |            |            |            |            |   |            |   |
| C9                                             | ADC_CONT   | ADCIN3_DEB | ADCIN2_DEB | ADCIN1_DEB | ADCIN3_CUR | ADCIN2_CUR |   | ADCIN1_CUR |   |
| CA                                             | AUTO1_HIGH | AUTO1_HIGH |            |            |            |            |   |            |   |
| CB                                             | AUTO1_LOW  | AUTO1_LOW  |            |            |            |            |   |            |   |
| CC                                             | AUTO2_HIGH | AUTO2_HIGH |            |            |            |            |   |            |   |
| CD                                             | AUTO2_LOW  | AUTO2_LOW  |            |            |            |            |   |            |   |
| CE                                             | AUTO3_HIGH | AUTO3_HIGH |            |            |            |            |   |            |   |
| CF                                             | AUTO3_LOW  | AUTO3_LOW  |            |            |            |            |   |            |   |

## System PMIC for Mobile and Automotive Applications

| Hex                                       | Register  | 7                 | 6                     | 5                     | 4                | 3                  | 2                    | 1           | 0           |
|-------------------------------------------|-----------|-------------------|-----------------------|-----------------------|------------------|--------------------|----------------------|-------------|-------------|
| PAGE 2                                    |           |                   |                       |                       |                  |                    |                      |             |             |
| 100                                       | PAGE_CON  | REVERT            | WRITE_MODE            | Reserved              |                  |                    | REG_PAGE             |             |             |
| OTP                                       |           |                   |                       |                       |                  |                    |                      |             |             |
| 101                                       | OTP_CONT  | GP_WRITE_D<br>S   | OTP_CONF_LO<br>C<br>K | OTP_APPS_LO<br>C<br>K | OTP_GP_LOCK      | PC_DONE            | OTP_APPS_RD          | OTP_GP_RD   | OTP_TIM     |
| 102                                       | OTP_ADDR  | OTP_ADDR          |                       |                       |                  |                    |                      |             |             |
| 103                                       | OTP_DATA  | OTP_DATA          |                       |                       |                  |                    |                      |             |             |
| Customer Trim and Configuration Registers |           |                   |                       |                       |                  |                    |                      |             |             |
| 104                                       | T_OFFSET  | T_OFFSET          |                       |                       |                  |                    |                      |             |             |
| 105                                       | INTERFACE | IF_BASE_ADDR      |                       |                       |                  | R/W_POL            | CPHA                 | CPOL        | nCS_POL     |
| 106                                       | CONFIG_A  | IF_TYPE           | PM_IF_HSM             | PM_IF_FMP             | PM_IF_V          | IRQ_TYPE           | PM_O_TYPE            | PM_O_V      | PM_I_V      |
| 107                                       | CONFIG_B  | CHG_CLK_MO<br>DE  | VDD_HYST_ADJ          |                       |                  | VDD_FAULT_ADJ      |                      |             |             |
| 108                                       | CONFIG_C  | BPERI_CLK_IN<br>V | BIO_CLK_INV           | BMEM_CLK_INV          | BPRO_CLK_IN<br>V | BCORE1_CLK_IN<br>V | BUCK_ACTV_DI<br>SCHG | LDO1_TRACK  |             |
| 109                                       | CONFIG_D  | GP_FB3_TYPE       | GP_FB2_TYPE           | FORCE_RESET           | HS_IF_HSM        | HS_IF_FMP          | SYSTEM_EN_RD         | nIRQ_MODE   | GPI_V       |
| 10A                                       | CONFIG_E  | PERI_SW_AUT<br>O  | CORE_SW_AUT<br>O      | BPERI_AUTO            | BIO_AUTO         | BMEM_AUTO          | BPRO_AUTO            | BCORE2_AUTO | BCORE1_AUTO |
| 10B                                       | CONFIG_F  | LDO11_BYP         | LDO8_BYP              | LDO7_BYP              | LDO4_BYP         | LDO3_BYP           | LDO11_AUTO           | LDO10_AUTO  | LDO9_AUTO   |
| 10C                                       | CONFIG_G  | LDO8_AUTO         | LDO7_AUTO             | LDO6_AUTO             | LDO5_AUTO        | LDO4_AUTO          | LDO3_AUTO            | LDO2_AUTO   | LDO1_AUTO   |
| 10D                                       | CONFIG_H  | BUCK_MERGE        | BCORE1_OD             | BCORE2_OD             | BPRO_OD          | BCORE_MERGE        | MERGE_SENSE          | LDO8_MODE   | PWM_CLK     |
| 10E                                       | CONFIG_I  | LDO_SD            | INT_SD_MODE           | HOST_SD_MOD<br>E      | KEY_SD_MOD<br>E  | GPI14_15_SD        | nONKEY_SD            | nONKEY_PIN  |             |
| 10F                                       | CONFIG_J  | IF_RESET          | TWOWIRE_TO            | RESET_DURATION        |                  | SHUT_DELAY         |                      | KEY_DELAY   |             |
| 110                                       | CONFIG_K  | GPI7_PUPD         | GPI6_PUPD             | GPI5_PUPD             | GPI4_PUPD        | GPI3_PUPD          | GPI02_PUPD           | GPI01_PUPD  | GPI00_PUPD  |
| 111                                       | CONFIG_L  | GPI015_PUPD       | GPI014_PUPD           | GPI013_PUPD           | GPI012_PUPD      | GPI011_PUPD        | GPI010_PUPD          | GPI09_PUPD  | GPI08_PUPD  |

## System PMIC for Mobile and Automotive Applications

| Hex                            | Register  | 7                | 6           | 5            | 4                | 3           | 2            | 1                  | 0                  |
|--------------------------------|-----------|------------------|-------------|--------------|------------------|-------------|--------------|--------------------|--------------------|
| 112                            | CONFIG_M  | OSC_FREQ         |             | Reserved     |                  |             |              |                    |                    |
| 113                            | CONFIG_N  | Reserved         |             |              |                  |             |              |                    |                    |
| 114                            | MON_REG_1 | UVOV_DELAY       |             | MON_MODE     |                  | MON_DEB     | MON_RES      | MON_THRES          |                    |
| 115                            | MON_REG_2 | LDO8_MON_EN<br>N | LDO7_MON_EN | LDO6_MON_EN  | LDO5_MON_EN<br>N | LDO4_MON_EN | LDO3_MON_EN  | LDO2_MON_EN        | LDO1_MON_EN        |
| 116                            | MON_REG_3 | Reserved         |             |              |                  |             | LDO11_MON_EN | LDO10_MON_EN       | LDO9_MON_EN        |
| 117                            | MON_REG_4 | Reserved         |             | BPERI_MON_EN | BMEM_MON_EN<br>N | BIO_MON_EN  | BPRO_MON_EN  | BCORE2_MON_EN<br>N | BCORE1_MON_EN<br>N |
| 118                            | RESERVED  | Reserved         |             |              |                  |             |              |                    |                    |
| 119                            | RESERVED  | Reserved         |             |              |                  |             |              |                    |                    |
| 11A                            | RESERVED  | Reserved         |             |              |                  |             |              |                    |                    |
| 11B                            | RESERVED  | Reserved         |             |              |                  |             |              |                    |                    |
| 11C                            | RESERVED  | Reserved         |             |              |                  |             |              |                    |                    |
| 11D                            | RESERVED  | Reserved         |             |              |                  |             |              |                    |                    |
| 11E                            | MON_REG_5 | Reserved         | MONA9_IDX   |              |                  | Reserved    | MONA8_IDX    |                    |                    |
| 11F                            | MON_REG_6 | Reserved         |             |              |                  |             | MONA10_IDX   |                    |                    |
| 120                            | TRIM_CLDR | TRIM_CLDR        |             |              |                  |             |              |                    |                    |
| General Purpose Registers (GP) |           |                  |             |              |                  |             |              |                    |                    |
| 121                            | GP_ID_0   | GP_0             |             |              |                  |             |              |                    |                    |
| 122                            | GP_ID_1   | GP_1             |             |              |                  |             |              |                    |                    |
| 123                            | GP_ID_2   | GP_2             |             |              |                  |             |              |                    |                    |
| 124                            | GP_ID_3   | GP_3             |             |              |                  |             |              |                    |                    |
| 125                            | GP_ID_4   | GP_4             |             |              |                  |             |              |                    |                    |
| 126                            | GP_ID_5   | GP_5             |             |              |                  |             |              |                    |                    |
| 127                            | GP_ID_6   | GP_6             |             |              |                  |             |              |                    |                    |

## System PMIC for Mobile and Automotive Applications

| Hex                      | Register | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|----------|----------|---|---|---|---|---|---|---|
| 128                      | GP_ID_7  | GP_7     |   |   |   |   |   |   |   |
| 129                      | GP_ID_8  | GP_8     |   |   |   |   |   |   |   |
| 12A                      | GP_ID_9  | GP_9     |   |   |   |   |   |   |   |
| 12B                      | GP_ID_10 | GP_10    |   |   |   |   |   |   |   |
| 12C                      | GP_ID_11 | GP_11    |   |   |   |   |   |   |   |
| 12D                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 12E                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 12F                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 130                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 131                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 132                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 133                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 134                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| Internal Debug Registers |          |          |   |   |   |   |   |   |   |
| 135                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 136                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 137                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 138                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 139                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 13A                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 13B                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 13C                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 13D                      | RESERVED | Reserved |   |   |   |   |   |   |   |
| 13E                      | RESERVED | Reserved |   |   |   |   |   |   |   |

## System PMIC for Mobile and Automotive Applications

| Hex                           | Register    | 7          | 6          | 5        | 4      | 3   | 2        | 1          | 0          |
|-------------------------------|-------------|------------|------------|----------|--------|-----|----------|------------|------------|
| 13F                           | MISC_SUPP   | Reserved   |            |          |        |     |          | CRYSTAL_OK | OTP_CLK_ON |
| PAGE 3                        |             |            |            |          |        |     |          |            |            |
| 180                           | PAGE_CON    | REVERT     | WRITE_MODE | Reserved |        |     | REG_PAGE |            |            |
| Chip Identification Registers |             |            |            |          |        |     |          |            |            |
| 181                           | DEVICE_ID   | DEVICE_ID  |            |          |        |     |          |            |            |
| 182                           | VARIANT_ID  | MRC        |            |          |        | VRC |          |            |            |
| 183                           | CUSTOMER_ID | CUST_ID    |            |          |        |     |          |            |            |
| 184                           | CONFIG_ID   | CONFIG_REV |            |          |        |     |          |            |            |
| 1A8                           | PMIC_STATUS | PC_DONE    | Reserved   |          | Status |     |          |            |            |

Most register bits are reset to defaults (zero in most cases) when powering up from RESET mode. An exception is for example FAULT\_LOG that is not loaded from OTP. Register fields shown in BOLD are loaded from OTP.

## System PMIC for Mobile and Automotive Applications

### 8 Definitions

#### 8.1 Power Dissipation and Thermal Design

When designing with the DA9063, consideration must be given to power dissipation as the level of integration of the device can result in high power when all functions are operating with high battery voltages. Exceeding the package power dissipation capabilities results in the internal thermal sensor shutting down the device until it has sufficiently cooled.

The package includes a thermal management paddle to improve heat spreading into the PCB.

##### For Linear Regulators:

Linear regulators operating with a high current and high differential voltage between input and output dissipate the following power:

$$P_{diss} = (V_{in} - V_{out}) \times I_{out}$$

Example: a regulator supplying 150 mA at 2.8 V from a fully-charged lithium battery ( $V_{DD} = 4.1$  V):

$$P_{diss} = (4.1V - 2.8V) \times 0.15A = 195mW$$

##### For Switching Regulators:

$$P_{out} = P_{in} \times Efficiency$$

Therefore,

$$P_{diss} = P_{in} - P_{out}$$

$$P_{diss} = \frac{P_{out}}{Efficiency} - P_{out}$$

$$P_{diss} = P_{out} \times \left( \frac{1}{Efficiency} - 1 \right)$$

$$P_{diss} = I_{out} \times V_{out} \times \left( \frac{1}{Efficiency} - 1 \right)$$

Example: an 85 % efficient buck converter supplying 1.2 V at 400 mA:

$$P_{diss} = 1.2V \times 0.4A \times \left( \frac{1}{0.85} - 1 \right) = 85mW$$

As the DA9063 has multiple regulators, each supply must be separately considered and their powers summed to give the total device dissipation (current drawn from the reference and control circuitry can be considered negligible in these calculations).

## System PMIC for Mobile and Automotive Applications

### 8.2 Regulator Parameter - Dropout Voltage

In the DA9063, a regulator's dropout voltage is defined as the minimum voltage differential between the input and output voltages whilst regulation still takes place. Within the regulator, voltage control takes place across a PMOS pass transistor and, when entering the dropout condition, the transistor is fully turned on and therefore cannot provide any further voltage control. When the transistor is fully turned on, the output voltage tracks the input voltage and regulation ceases. As the DA9063 is a CMOS device and uses a PMOS pass transistor, the dropout voltage is directly related to the on-resistance of the device. In the device, the pass transistors are sized to provide the optimum balance between required performance and silicon area. By employing a 0.25  $\mu\text{m}$  process, Dialog Semiconductor is able to achieve very small pass transistor sizes for superior performance.

$$V_{\text{dropout}} = V_{\text{in}} - V_{\text{out}} = R_{\text{dson}} \times I_{\text{out}}$$

When defining dropout voltage, it is specified in relation to a minimum acceptable change in output voltage. For example, all Dialog Semiconductor regulators have dropout voltage defined as the point at which the output voltage drops 10 mV below the output voltage at the minimum guaranteed operating voltage. The worst case conditions for dropout are high temperature (highest on-resistance for the internal pass device) and maximum current load.

### 8.3 Regulator Parameter - Power Supply Rejection

Power supply rejection (PSRR) is especially important in the supplies to the RF and audio parts of the telephone. In a TDMA system such as GSM, the 217 Hz transmit burst from the power amplifier results in significant current pulses being drawn from the battery. These can peak at up to 2 Amps before reaching a steady state of 1.4 Amps (see below). Due to the battery having a finite internal resistance (typically 0.5  $\Omega$ ), these current peaks induce ripple on the battery voltage of up to 500 mV. Since the supplies to the audio and RF are derived from this supply, it is essential that this ripple is removed otherwise it would show as a 217 Hz tone in the audio and could also affect the transmit signal. Power supply rejection should always be specified under worst case conditions – when the battery is at its minimum operating voltage and when there is minimum headroom available due to dropout.

### 8.4 Regulator Parameter - Line Regulation

Static line regulation is a measurement that indicates a change in the regulator output voltage,  $\Delta V_{\text{reg}}$  (regulator operating with a constant load current), in response to a change in the input voltage,  $\Delta V_{\text{in}}$ . Transient line regulation is a measurement of the peak change,  $\Delta V_{\text{reg}}$ , in regulated voltage seen when the line input voltage changes.

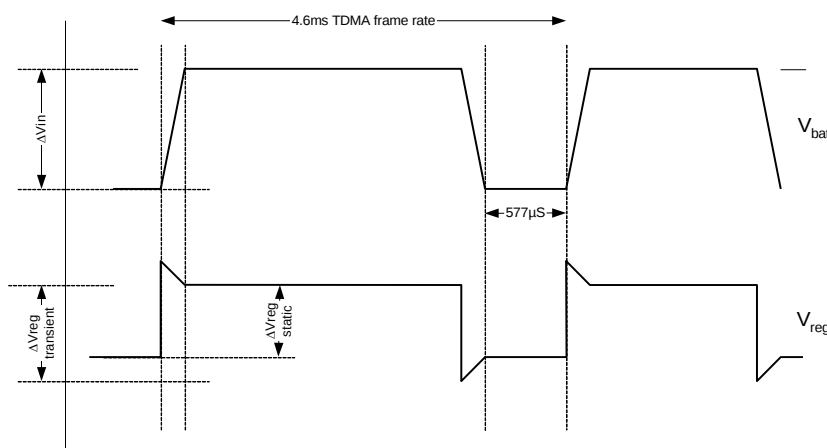
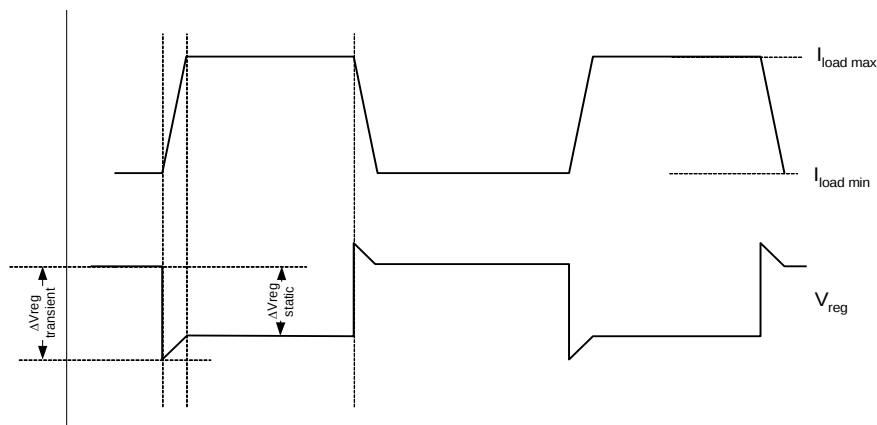


Figure 40: Line Regulation

## System PMIC for Mobile and Automotive Applications

### 8.5 Regulator Parameter - Load Regulation

Static load regulation is a measurement that indicates a change in the regulator output voltage,  $\Delta V_{\text{reg}}$ , in response to a change in the regulator loading,  $\Delta I_{\text{load}}$ , whilst the regulator input voltage remains constant. Transient load regulation is a measurement of the peak change in regulated voltage,  $\Delta V_{\text{reg}}$ , seen when the regulator load changes.



**Figure 41: Load Regulation**

Please contact Dialog Semiconductor for latest application information on the DA9063 and other power management devices.

System PMIC for Mobile and Automotive Applications

9 Package Information

9.1 Package Outlines

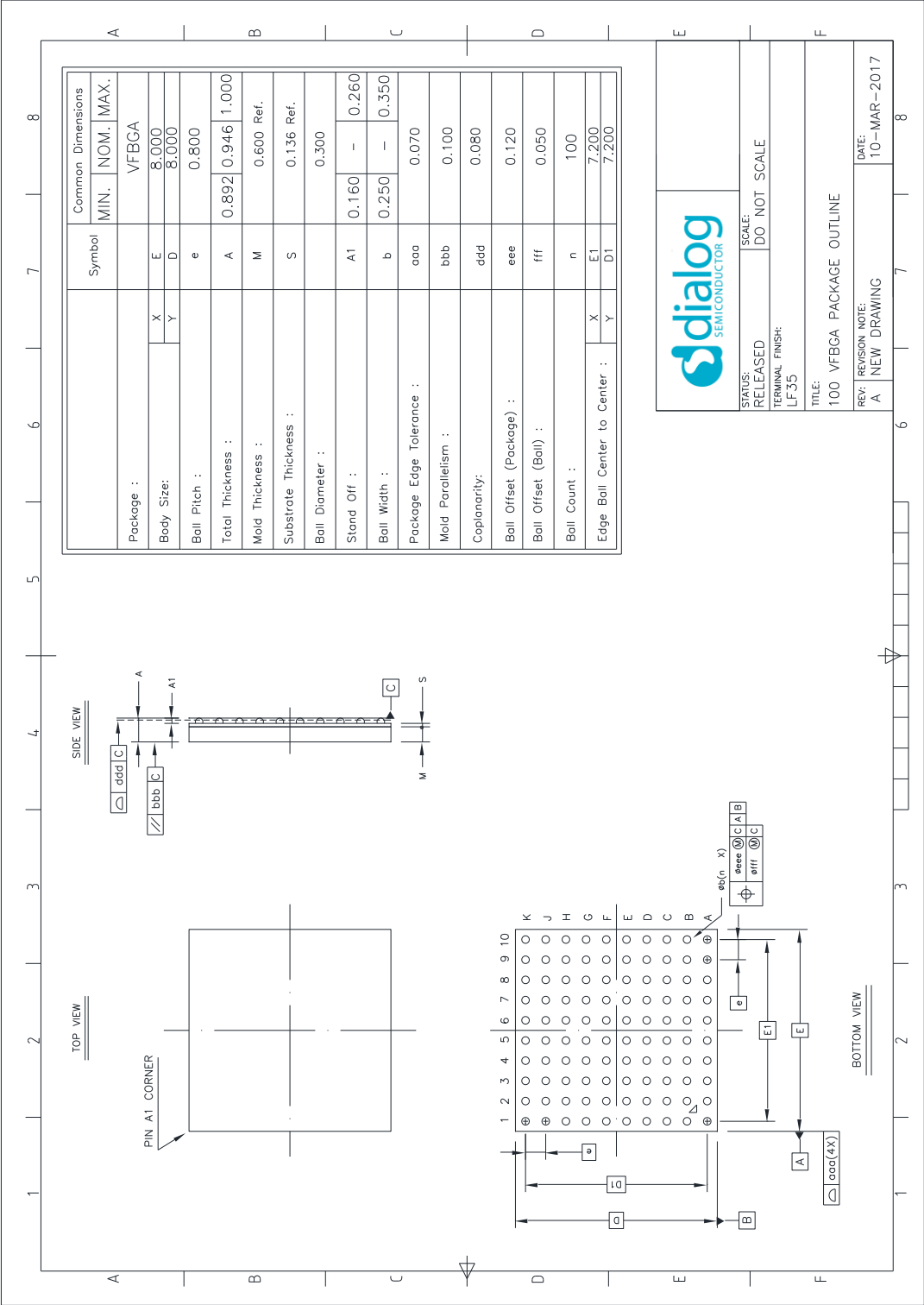


Figure 42: Package Outline Drawing 100 VFBGA 0.3 mm Ball Diameter

System PMIC for Mobile and Automotive Applications

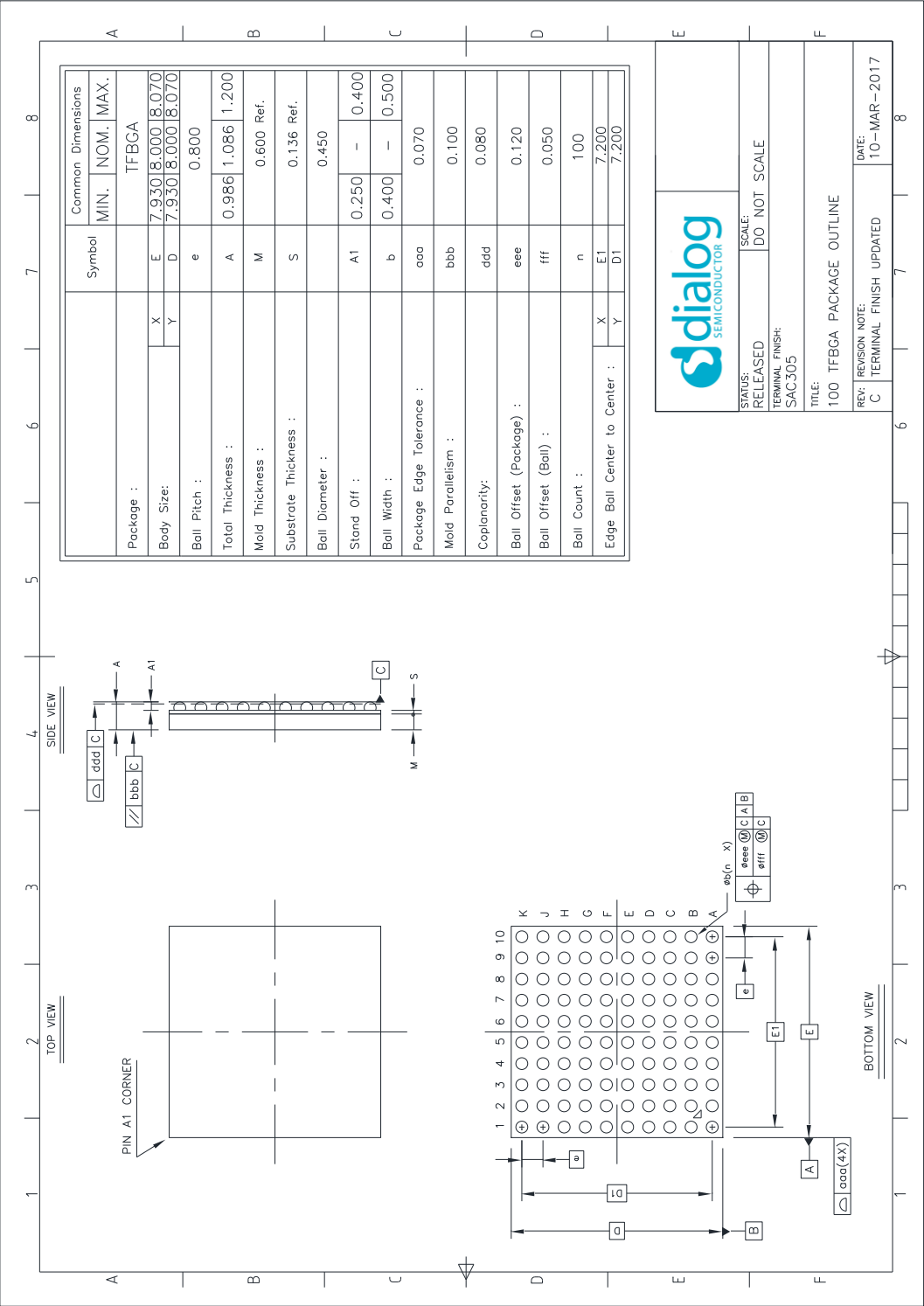


Figure 43: Package Outline Drawing 100 TFBGA 0.45 mm Ball Diameter

## System PMIC for Mobile and Automotive Applications

### 9.2 Package Marking

| Package Marking                                                                      |                                                                                    |  |  |  |  |  |                            |
|--------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|--|--|--|--|--|----------------------------|
| A1 Corner >                                                                          | Marking Content                                                                    |  |  |  |  |  | Format                     |
| 1st                                                                                  |  |  |  |  |  |  | Orientation                |
| 2nd                                                                                  |                                                                                    |  |  |  |  |  | Logo                       |
| 3rd                                                                                  |                                                                                    |  |  |  |  |  | Part No.                   |
| 4th                                                                                  |                                                                                    |  |  |  |  |  | OTP/Silicon Version/Option |
| 5th                                                                                  |                                                                                    |  |  |  |  |  | Date Code                  |
|                                                                                      |                                                                                    |  |  |  |  |  |                            |
| Date Code Format: yy = Year, ww = Week, zzzz = Traceability                          |                                                                                    |  |  |  |  |  |                            |
| xx identifies the OTP Variant, vv may be used to show the silicon version.           |                                                                                    |  |  |  |  |  |                            |
| -A and -AT optionally indicate the Automotive and Automotive high temp test options. |                                                                                    |  |  |  |  |  |                            |

### 9.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in [Table 50](#).

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from <http://www.jedec.org>.

The VFBGA and TFBGA packages are qualified for MSL 3.

**Table 50: MSL Classification**

| MSL Level | Floor Lifetime | Conditions      |
|-----------|----------------|-----------------|
| MSL 4     | 72 hours       | 30 °C / 60 % RH |
| MSL 3     | 168 hours      | 30 °C / 60 % RH |
| MSL 2A    | 4 weeks        | 30 °C / 60 % RH |
| MSL 2     | 1 year         | 30 °C / 60 % RH |
| MSL 1     | Unlimited      | 30 °C / 85 % RH |

## System PMIC for Mobile and Automotive Applications

### 10 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's [website](#) or your local sales representative.

**Table 51: Ordering Information**

| Part Number                                                                                                           | Package                                                             | Shipment Form | Pack Quantity |
|-----------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|---------------|---------------|
| <b>Consumer / Industrial: 0.30 mm ball diameter, 25 °C production testing</b>                                         |                                                                     |               |               |
| DA9063-xxHK1<br><a href="#">Note 2</a>                                                                                | 100 VFBGA, 8.0 mm x 8.0 mm x 1.0 mm,<br>0.8 mm pitch, Pb-free/green | Tray          | 260           |
| DA9063-xxHK2<br><a href="#">Note 2</a>                                                                                | 100 VFBGA, 8.0 mm x 8.0 mm x 1.0 mm,<br>0.8 mm pitch, Pb-free/green | T&R           | 2500          |
| <b>Consumer / Industrial: 0.45 mm ball diameter, 25 °C production testing</b>                                         |                                                                     |               |               |
| DA9063-xxHO1                                                                                                          | 100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm,<br>0.8 mm pitch, Pb-free/green | Tray          | 260           |
| DA9063-xxHO2                                                                                                          | 100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm,<br>0.8 mm pitch, Pb-free/green | T&R           | 2500          |
| <b>Automotive AEC-Q100 Grade 2: 0.30 mm ball diameter, 25 °C production testing <a href="#">Note 1</a></b>            |                                                                     |               |               |
| DA9063-xxHK1-A<br><a href="#">Note 2</a>                                                                              | 100 VFBGA, 8.0 mm x 8.0 mm x 1.0 mm,<br>0.8 mm pitch, Pb-free/green | Tray          | 260           |
| DA9063-xxHK2-A<br><a href="#">Note 2</a>                                                                              | 100 VFBGA, 8.0 mm x 8.0 mm x 1.0 mm,<br>0.8 mm pitch, Pb-free/green | T&R           | 2500          |
| <b>Automotive AEC-Q100 Grade 2: 0.45 mm ball diameter, 25 °C production testing <a href="#">Note 1</a></b>            |                                                                     |               |               |
| DA9063-xxHO1-A                                                                                                        | 100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm,<br>0.8 mm pitch, Pb-free/green | Tray          | 260           |
| DA9063-xxHO2-A                                                                                                        | 100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm,<br>0.8 mm pitch, Pb-free/green | T&R           | 2500          |
| <b>Automotive AEC-Q100 Grade 2: 0.45 mm ball diameter, high temperature production testing <a href="#">Note 1</a></b> |                                                                     |               |               |
| DA9063-xxHO1-AT                                                                                                       | 100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm,<br>0.8 mm pitch, Pb-free/green | Tray          | 260           |
| DA9063-xxHO2-AT                                                                                                       | 100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm,<br>0.8 mm pitch, Pb-free/green | T&R           | 2500          |

**Note 1** Operating temperature is defined in Section 5.2. Automotive qualification temperature is defined by the [Automotive Electronics Council](#) AEC-Q100 specification.

**Note 2** The 0.30 mm ball diameter version is not recommended for new designs.

#### 10.1 Variants Ordering Information

DA9063 supports delivery of variants indicated by xx in the part number above, where xx is replaced with the actual variant number. Please contact your local Dialog Semiconductor office or representative to discuss requirements.

## System PMIC for Mobile and Automotive Applications

### 11 Application Information

The following recommended components are examples selected from requirements of a typical application. The electrical characteristics (for example, supported voltage/current range) have to be cross-checked and component types may need to be adapted from the individual needs of the target circuitry.

#### 11.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account. On the VSYS main supply rail a minimum distributed capacitance of 40  $\mu\text{F}$  (actual capacitance after voltage and temperature derating) is required. For example, a typical design might use:

- 22  $\mu\text{F}$  within 1.5 mm of each BUCKCORE1, BUCKCORE2 and BUCKPRO supply pin.
- 10  $\mu\text{F}$  within 1.5 mm of each BUCKPERI, BUCKIO and BUCKMEM supply pin or 1 x 22  $\mu\text{F}$  if all are attached to a PCB power/split plane.
- 2 x 1  $\mu\text{F}$  shared by all VDD\_LDOx pins if they are all close together, for example, all attached to a power/split plane.
- 1  $\mu\text{F}$  close to the VSYS pin.
- Buck output capacitors should be close to the buck inductors.

The amount of decoupling required will be dependent on the specific application.

**Table 52: Recommended Capacitor Types**

| Application                                                              | Value             | Tol. (%) | Size | Height (mm) | Temp. Char.    | Rated Voltage (V) | Type (Murata/Samsung)                       |
|--------------------------------------------------------------------------|-------------------|----------|------|-------------|----------------|-------------------|---------------------------------------------|
| VLDO1, VLDO5                                                             | 1.0 $\mu\text{F}$ | $\pm 10$ | 0402 | 0.55        | X5R $\pm 15\%$ | 10                | GRM155R61A105KE15                           |
| VDDCORE, VLDO2, VLDO3, VLDO4, VLDO6, VLDO7, VLDO8, VLDO9, VLDO10, VLDO11 | 2.2 $\mu\text{F}$ | $\pm 20$ | 0402 | 0.55        | X5R $\pm 15\%$ | 6.3               | GRM155R60J225ME95                           |
| VBUCKPER, VBUCKIO, VBUCKMEM, VSYS                                        | 22 $\mu\text{F}$  | $\pm 20$ | 0805 | 0.95        | X5R $\pm 15\%$ | 6.3               | GRM219R60J226M***                           |
|                                                                          |                   | $\pm 20$ | 0402 | 0.5         | X5R $\pm 15\%$ | 4.0               | CL05A226MR5NZNC                             |
|                                                                          | 47 $\mu\text{F}$  | $\pm 20$ | 0805 | 0.95        | X5R $\pm 15\%$ | 4.0               | GRM219R60G476M***                           |
|                                                                          |                   | $\pm 20$ | 0603 | 0.8         | X5R $\pm 15\%$ | 4.0               | CL10A476MR8NZN                              |
| VBUCKCORE 1 and 2, VBUCKPRO (using full-current mode)                    | 22 $\mu\text{F}$  | $\pm 20$ | 0603 | 1.0         | X5R $\pm 15\%$ | 6.3               | GRM188R60J226MEA0<br><a href="#">Note 1</a> |
|                                                                          |                   | $\pm 20$ | 0402 | 0.5         | X5R $\pm 15\%$ | 4.0               | CL05A226MR5NZNC                             |
|                                                                          | 47 $\mu\text{F}$  | $\pm 20$ | 0805 | 0.95        | X5R $\pm 15\%$ | 4.0               | GRM219R60G476M***61                         |
|                                                                          |                   | $\pm 20$ | 0603 | 0.8         | X5R $\pm 15\%$ | 4.0               | CL10A476MR8NZN                              |
| VSYS                                                                     | 1.0 $\mu\text{F}$ | $\pm 10$ | 0402 | 0.5         | X5R $\pm 15\%$ | 10                | GRM155R61A105KE15                           |

## System PMIC for Mobile and Automotive Applications

| Application  | Value   | Tol. (%) | Size | Height (mm) | Temp. Char. | Rated Voltage (V) | Type (Murata/Samsung) |
|--------------|---------|----------|------|-------------|-------------|-------------------|-----------------------|
| VBBAT        | 470 nF  | ± 10     | 0402 | 0.5         | X5R ±15 %   | 50                | GRM155R61A474KE11     |
| VREF, VLNREF | 0.22 µF | ± 10     | 0402 | 0.5         | X7R ±15 %   | 16                | GRM155R71C224KA12     |
| VDDCORE      | 2.2 µF  | ± 20     | 0402 | 0.5         | X5R ±15 %   | 6.3               | GRM155R60J225ME95     |
| XIN, XOUT    | 12 pF   | ± 5      | 0402 | 0.5         | C0G         | 50                | GRM1555C1H120JA01D    |
| V_CP         | 47 nF   | ± 10     | 0402 | 0.5         | X7R ±15 %   | 10                | GRM155R71A473KA01     |

**Note 1** For output voltages > 1.4 V Murata GRM219R60J226M is recommended.

**Table 53: Recommended Automotive Capacitor Types**

| Application                                                              | Value   | Tol. (%) | Size | Height (mm) | Temp. Char. | Rated Voltage (V) | Type (Murata/Samsung) |
|--------------------------------------------------------------------------|---------|----------|------|-------------|-------------|-------------------|-----------------------|
| VLDO1, VLDO5                                                             | 1.0 µF  | ± 10     | 0805 | 1.25        | X7R         | 16                | GCM21BR71C105KA58     |
| VDDCORE, VLDO2, VLDO3, VLDO4, VLDO6, VLDO7, VLDO8, VLDO9, VLDO10, VLDO11 | 2.2 µF  | ± 20     | 0402 | 1.25        | X7R         | 10                | GCM21BR71A225MA37     |
| VBUCKPER, VBUCKIO, VBUCKMEM, VSYS                                        | 22 µF   | ± 20     | 1206 | 1.6         | X7R         | 6.3               | GCM31CR70J226ME23     |
|                                                                          | 47 µF   | ± 10     | 1206 | 1.6         | X7R         | 6.3               | GCM32ER70J476KE19     |
| VBUCKCORE 1 and 2, VBUCKPRO (using full-current mode)                    | 22 µF   | ± 20     | 1206 | 1.6         | X7R         | 6.3               | GCM31CR70J226ME23     |
|                                                                          | 47 µF   | ± 10     | 1206 | 1.6         | X7R         | 6.3               | GCM32ER70J476KE19     |
| VSYS                                                                     | 10 µF   | ± 10     | 0805 | 1.25        | X7R         | 10                | GCM21BR71A106ME22     |
|                                                                          | 1.0 µF  | ± 10     | 0805 | 1.25        | X7R         | 16                | GCM21BR71C105KA58     |
| VBBAT                                                                    | 470 nF  | ± 10     | 0402 | 0.5         | X7R         | 10                | GCM155C71A474KE36D    |
| VREF, VLNREF                                                             | 0.22 µF | ± 10     | 0402 | 0.5         | X7R         | 16                | GCM155R71C224ME02     |
| VDDCORE                                                                  | 2.2 µF  | ± 20     | 0402 | 1.25        | X7R         | 10                | GCM21BR71A225MA37     |
| XIN, XOUT                                                                | 12 pF   | ± 5      | 0402 | 0.5         | C0G         | 50                | GRM1555C1H120JA01D    |
| V_CP                                                                     | 47 nF   | ± 10     | 0402 | 0.5         | X7R         | 10                | GRM155R71A473KA01     |

## System PMIC for Mobile and Automotive Applications

### 11.2 Backup Device

The backup battery charger supports Lithium coin cells as well as Supercaps/Goldcaps. The RTC will require approximately 1.5  $\mu$ A between 3.1 V and 2 V for each hour that the RTC should stay alive with the main supply removed. The choice of backup device is dependent on application requirements.

**Table 54: Example Backup Devices**

| Type                                                         | Size (mm)        | Manufacturer      |
|--------------------------------------------------------------|------------------|-------------------|
| Lithium Battery (rechargeable) MS412FE-FL26E, 2.3 mAh, 3.0 V | 4.8 (dia.) x 1.2 | Seiko Instruments |
| Starcap SC SM 2R8, 0.1 F, 2.8 V                              | 4.8 (dia.) x 1.4 | Korchip           |
| Lithium Battery (rechargeable) ML614, 3.4 mAh, 3.0 V         | 6.8 (dia.) x 1.4 | Panasonic         |

### 11.3 Inductor Selection

Inductors should be selected based upon the following parameters:

- Rated maximum current: Usually a coil provides two current limits: ISAT of an Inductor specifies the current required to cause a reduction in the Inductance by a specified amount, typically 30 %, IRMS of an Inductor specifies the current required to affect a temperature rise of a maximum specified amount.
- DC resistance: Critical to converter efficiency at high current and should therefore be minimized.
- ESR at the buck switching frequency: Critical to converter efficiency in PFM mode and should therefore be minimized.
- Inductance: Given by converter electrical characteristics; 1.0  $\mu$ H for all DA9063 switched-mode step-down converters.

**Table 55: Recommended Inductor Types**

| Application                                                               | Value ( $\mu$ H) | Tol. (%) | ISAT (A) | IRMS (A) | DCR (Typ.) (m $\Omega$ ) | Size (mm)   | Type                                 |
|---------------------------------------------------------------------------|------------------|----------|----------|----------|--------------------------|-------------|--------------------------------------|
| BUCKPERI, BUCKMEM, BUCKIO, BUCKCORE1, BUCKCORE2                           | 1.0              | $\pm 30$ | 2.7      | 2.3      | 55                       | 2.0x1.6x1.0 | Toko 1285AS-H-1R0N                   |
|                                                                           |                  | $\pm 20$ | 2.65     | 2.45     | 60                       | 2.0x1.6x1.0 | Tayo Yuden MAKK2016T1R0M (Reference) |
|                                                                           |                  | $\pm 20$ | 3.9      | 3.1      | 50                       | 2.0x1.6x1.0 | TDK TFM201610ALM-1R0MTAA             |
| BUCKPRO, BUCKCORE1 and 2 using full-current mode or merged BUCKMEM/BUCKIO | 1.0              | $\pm 30$ | 3.4      | 3.0      | 60                       | 2.5x2.0x1.0 | Toko 1269AS-H-1R0N                   |
|                                                                           |                  | $\pm 20$ | 3.6      | 3.1      | 45                       | 2.5x2.0x1.2 | Tayo Yuden MAMK2520T1R0M             |
|                                                                           |                  | $\pm 20$ | 3.8      | 3.5      | 45                       | 2.5x2.0x1.2 | Toko 1239AS-H-1R0N (Reference)       |
|                                                                           |                  | $\pm 30$ | 3.9      | 3.1      | 48                       | 3.2x2.5x1.0 | Toko 1276AS-H-1R0N                   |
|                                                                           |                  | $\pm 20$ | 4.5      | 3.6      | 38                       | 2.5x2.0x1.0 | TDK TFM252010ALM-1R0MTAA             |

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| Application         | Value (μH) | Tol. (%) | ISAT (A) | IRMS (A) | DCR (Typ.) (mΩ) | Size (mm)   | Type                                |
|---------------------|------------|----------|----------|----------|-----------------|-------------|-------------------------------------|
|                     |            | ±20      | 4.2      | 3.7      | 35              | 2.5x2.0x1.2 | TDK TFM252012ALMA-1R0MTAA (AECQ200) |
|                     |            | ±20      | 3.35     | 2.5      | 52              | 3.0x3.0x1.2 | Cyntec PST031B-1R0MS                |
|                     |            | ±20      | 8.8      | 12.0     | 8.2             | 4.0x4.0x2.1 | Coilcraft XGL4020-102ME (AEC-Q200)  |
| BUCKPRO, (VTT mode) | 0.24       | ±30      | 1.65     | 2.3      | 49              | 1.6x0.8x1.0 | Taiyo Yuden MBKK1608TR24N           |
|                     | 0.25       | ±20      | 9.7      | 11.45    | 7.64            | 4.0x4.0x1.2 | Coilcraft XFL4012-251ME             |

### 11.4 Resistors

Table 56: Recommended Resistor Types

| Application                 | Value  | Size | Tolerance | P <sub>MAX</sub> | Type                   |
|-----------------------------|--------|------|-----------|------------------|------------------------|
| IREF bias current reference | 200 kΩ | 0402 | ±1%       | 100 mW           | Panasonic ERJ2RKF2003x |

### 11.5 External Pass Transistors

Table 57: Recommended External Pass Transistor Types

| Application        | Package                        | Type                 |
|--------------------|--------------------------------|----------------------|
| BUCK Rail Switches | WLCSP 1.6 mm x1.6 mm x 0.55 mm | Fairchild FDME410NZT |

### 11.6 Crystal

The Real Time Clock module requires an external 32.768 kHz crystal. For correct component selection, the effective load capacitance must be taken into account: this includes both external capacitors on pins XIN and XOUT in series combination, plus the PCB and DA9063 stray capacitances. For example, if two 12 pF external capacitors are used, giving a series combination of 6 pF, and the stray capacitances are 3 pF, then a crystal type that specifies a load capacitance of 9 pF should be chosen. Different stray capacitances may require different external capacitors and/or a different crystal type. Furthermore, the series resistance of the crystal must not exceed 100 kΩ.

Table 58: Example Crystal Type

| Type                               | Size           | Manufacturer  |
|------------------------------------|----------------|---------------|
| CC7V-T1A 32.768 kHz 9.0 pF ±30 ppm | 3.2x1.5x0.9 mm | Micro Crystal |

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## 12 Layout Guidelines

### 12.1 General Recommendations

- Appropriate trace width and quantity of vias should be used for all power supply paths. Too high trace resistances can prevent the system from achieving the best performance, for example, the efficiency and the current ratings of switch-mode converters and charger might be degraded. Furthermore, the PCB may be exposed to thermal hot spots, which can lead to critical overheating due to the positive temperature coefficient of copper. Special care must be taken with the DA9063 pad connections. The traces of the outer row should be connected with the same width as the pads and should become wider as soon as possible. For supply pins in the second row, connection to an inner board layer is recommended (depending on the maximum current two or more vias might be required).
- A common ground plane should be used, which allows proper electrical and thermal performance. Noise sensitive references such as the VREF/VLNREF capacitors and IREF resistor should be referred to a silent ground which is connected at a star point underneath or close to the DA9063 main ground connection.
- Generally, all power tracks with discontinuous/high currents should be kept as short as possible.
- Noise sensitive analog signals such as feedback lines or crystal connections should be kept away from traces carrying pulsed analog or digital signals. This can be achieved by separation (distance) or shielding with quiet signals or ground traces.

### 12.2 LDOs and Switched Mode Supplies

- The placement of the distributed capacitors on the  $V_{SYS}$  rail must ensure that all VDD inputs – and especially to the VSYS pin, the buck converters and LDOs – are connected to a bypass capacitor close to the pads. It is recommended placing at least two 1  $\mu$ F capacitors close to the LDO supply pads and at least one 10  $\mu$ F close to the buck VDD rail. Using a local power plane underneath the chip for  $V_{SYS}$  might be considered.
- Transient current loops in the area of the switched mode converters should be minimized.
- The common references (IREF resistor, VREF/VLNREF capacitors) should be placed close to the DA9063 and cross coupling to any noisy digital or analog trace must be avoided.
- Output capacitors of the LDOs can be placed close to the input pins of the supplied devices (remote from the DA9063).
- Care must be taken with trace routing to ensure that no current is carried on feedback lines of the buck output voltages  $V_{BUCK}$ .
- The inductor placement is less critical since parasitic inductances have negligible effect.

### 12.3 Crystal Oscillator

- The crystal and its load capacitors should be placed as close as possible to the IC with short and symmetric traces.
- The traces must be isolated from noisy signals, especially from clocked digital ones. Ideally the lines should be buried between two ground layers, surrounded by additional ground traces.

### 12.4 Thermal Connection, Land Pad, and Stencil Design

- The DA9063 provides a central ground area of balls, which are soldered to the PCB's central ground pad. This PCB ground pad must be connected with as many vias and as direct as possible to the PCB's main ground plane in order to achieve good thermal performance.
- Solder mask openings for the ball landing pads must be arranged to prohibit solder balls flowing into vias.

For further PCB layout guidance, see PCB Layout Guidelines [3].

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### Appendix A Register Descriptions

This appendix describes the registers summarized in Section 7.

#### A.1 Register Page Control

**Table 59: PAGE\_CON**

| Register Address | Bit | Type | Label      | Description                                                                                                                                               |
|------------------|-----|------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x00<br>PAGE_CON | 7   | RW   | REVERT     | Resets REG_PAGE to 00 after read/write access has finished                                                                                                |
|                  | 6   | RW   | WRITE_MODE | 2-WIRE multiple write mode<br>0: Page Write Mode<br>1: Repeated Write Mode                                                                                |
|                  | 5:3 | RW   | Reserved   |                                                                                                                                                           |
|                  | 2:0 | RW   | REG_PAGE   | 000: Selects Register 0x01 to 0x3F<br>001: Selects Register 0x81 to 0xCF<br>010: Selects Register 0x101 to 0x13F<br>011: Reserved for production and test |

The PAGE\_CON register is located at address 0x00 of each register page (0x00 and 0x80). Each of the control interfaces (4-WIRE and the two 2-WIRE) provides an individual instance of the PAGE\_CON register.

#### A.2 Register Page 0

##### A.2.1 Power Manager Control and Monitoring

The STATUS register reports the current value of the various signals at the time that it is read out. All the status bits have the same polarity as their corresponding signals.

**Table 60: STATUS\_A**

| Register Address | Bit | Type | Label    | Description                                                          |
|------------------|-----|------|----------|----------------------------------------------------------------------|
| 0x01<br>STATUS_A | 7:4 | R    | Reserved |                                                                      |
|                  | 3   | R    | COMP1V2  | Output state of 1.2 V comparator                                     |
|                  | 2   | R    | DVC      | Asserted as long as at least one DVC supply performs voltage ramping |
|                  | 1   | R    | WAKE     | CHG_WAKE level                                                       |
|                  | 0   | R    | nONKEY   | Asserted as long nONKEY is pressed (low level)                       |

**Table 61: STATUS\_B**

| Register Address | Bit | Type | Label | Description                                                             |
|------------------|-----|------|-------|-------------------------------------------------------------------------|
| 0x02<br>STATUS_B | 7   | R    | GPI7  | GPI7 level                                                              |
|                  | 6   | R    | GPI6  | GPI6 level                                                              |
|                  | 5   | R    | GPI5  | GPI5 level                                                              |
|                  | 4   | R    | GPI4  | GPI4 level                                                              |
|                  | 3   | R    | GPI3  | GPI3 level                                                              |
|                  | 2   | R    | GPI2  | GPI2 level or ADCIN3 threshold indicator (1 when overriding high limit) |

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| Register Address | Bit | Type | Label | Description                                                             |
|------------------|-----|------|-------|-------------------------------------------------------------------------|
|                  | 1   | R    | GPI1  | GPI1 level or ADCIN2 threshold indicator (1 when overriding high limit) |
|                  | 0   | R    | GPI0  | GPI0 level or ADCIN1 threshold indicator (1 when overriding high limit) |

Table 62: STATUS\_C

| Register Address | Bit | Type | Label | Description                    |
|------------------|-----|------|-------|--------------------------------|
| 0x03<br>STATUS_C | 7   | R    | GPI15 | GPI15 level                    |
|                  | 6   | R    | GPI14 | GPI14 level                    |
|                  | 5   | R    | GPI13 | GPI13/ EXT_WAKEUP/READY level  |
|                  | 4   | R    | GPI12 | GPI12/nVDD_FAULT/VDD_MON level |
|                  | 3   | R    | GPI11 | GPI11 level                    |
|                  | 2   | R    | GPI10 | GPI10/PWR1_EN level            |
|                  | 1   | R    | GPI9  | GPI9/PWR_EN level              |
|                  | 0   | R    | GPI8  | GPI8/SYS_EN level              |

Table 63: STATUS\_D

| Register Address | Bit | Type | Label     | Description                                        |
|------------------|-----|------|-----------|----------------------------------------------------|
| 0x04<br>STATUS_D | 7   | R/W  | LDO11_LIM | Asserted as long LDO11 hits its over-current limit |
|                  | 6   | R/W  | LDO8_LIM  | Asserted as long LDO8 hits its over-current limit  |
|                  | 5   | R/W  | LDO7_LIM  | Asserted as long LDO7 hits its over-current limit  |
|                  | 4   | R/W  | LDO4_LIM  | Asserted as long LDO4 hits its over-current limit  |
|                  | 3   | R/W  | LDO3_LIM  | Asserted as long LDO3 hits its over-current limit  |
|                  | 2:0 | R/W  | Reserved  |                                                    |

Table 64: FAULT\_LOG

| Register Address  | Bit | Type<br><a href="#">Note 1</a> | Label      | Description                                                                                                |
|-------------------|-----|--------------------------------|------------|------------------------------------------------------------------------------------------------------------|
| 0x05<br>FAULT_LOG | 7   | R                              | WAIT_SHUT  | Power down by time out of ID WAIT                                                                          |
|                   | 6   | R                              | nSHUT_DOWN | Power down by assertion of port nOFF, nSHUTDOWN                                                            |
|                   | 5   | R                              | KEY_RESET  | Power down from a long press of nONKEY or GPIO14/15                                                        |
|                   | 4   | R                              | TEMP_CRIT  | Junction over-temperature detected                                                                         |
|                   | 3   | R                              | VDD_START  | Power down by V <sub>sys</sub> under-voltage detect before or within 16 seconds after entering ACTIVE mode |
|                   | 2   | R                              | VDD_FAULT  | Power down by V <sub>sys</sub> under-voltage detect                                                        |
|                   | 1   | R                              | POR        | DA9063 starts up from NO-POWER or RTC/DELIVERY mode                                                        |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type<br>Note 1 | Label     | Description            |
|------------------|-----|----------------|-----------|------------------------|
|                  | 0   | R              | TWD_ERROR | Watchdog time violated |

**Note 1** Cleared from the host by writing back the read value.

The EVENT registers hold information about events that have occurred in the DA9063. Events are triggered by a change in the status registers that contains the status of monitored signals. When an EVENT bit is set in the event register the nIRQ signal is asserted (unless the nIRQ is to be masked by a bit in the IRQ mask register). The nIRQ is also masked during the power-up sequence and is not released until the event registers have been cleared. The IRQ triggering event register is cleared from the host by writing back its read value. The event registers may be read in page/repeated mode. New events that occur during clearing are delayed before they are passed to the event register, ensuring that the host controller does not miss them.

**Table 65: EVENT\_A**

| Register Address | Bit | Type        | Label     | Description                                                                    |
|------------------|-----|-------------|-----------|--------------------------------------------------------------------------------|
| 0x06<br>EVENT_A  | 7   | R           | EVENTS_D  | Asserted when register EVENT_B to EVENT_D have at least one event bit asserted |
|                  | 6   | R           | EVENTS_C  | Asserted when register EVENT_B to EVENT_C have at least one event bit asserted |
|                  | 5   | R           | EVENTS_B  | Asserted when register EVENT_B has at least one event bit asserted             |
|                  | 4   | R<br>Note 1 | E_SEQ_RDY | Sequencer reached final position caused event                                  |
|                  | 3   | R<br>Note 1 | E_ADC_RDY | ADC manual conversion result ready caused event                                |
|                  | 2   | R<br>Note 1 | E_TICK    | RTC tick caused event                                                          |
|                  | 1   | R<br>Note 1 | E_ALARM   | RTC alarm caused event                                                         |
|                  | 0   | R<br>Note 1 | E_nONKEY  | nONKEY caused event                                                            |

**Note 1** Cleared from the host by writing back the read value.

**Table 66: EVENT\_B**

| Register Address | Bit | Type<br>Note 1 | Label      | Description                                                                                                                                                                |
|------------------|-----|----------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x07<br>EVENT_B  | 7   | R              | E_VDD_WARN | V <sub>sys</sub> dropped below VDD_FAULT_UPPER threshold                                                                                                                   |
|                  | 6   | R              | E_VDD_MON  | V <sub>sys</sub> less or higher than VSYS_MON threshold caused event                                                                                                       |
|                  | 5   | R              | E_DVC_RDY  | Finish of all DVC voltage ramping event                                                                                                                                    |
|                  | 4   | R              | E_REG_UVOV | Event triggered from a monitored regulator voltage being out of selected range or from new regulator voltage measurement being available (depends on settings of MON_MODE) |
|                  | 3   | R              | E_LDO_LIM  | LDO3, 4, 7, 8 or 11 current limit exceeded for more than 10 ms                                                                                                             |
|                  | 2   | R              | E_COMP1V2  | 1.2 V comparator caused event                                                                                                                                              |

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| Register Address | Bit | Type<br>Note 1 | Label  | Description                      |
|------------------|-----|----------------|--------|----------------------------------|
|                  | 1   | R              | E_TEMP | Junction high temp caused event  |
|                  | 0   | R              | E_WAKE | Detected rising edge on CHG_WAKE |

**Note 1** Cleared from the host by writing back the read value.

**Table 67: EVENT\_C**

| Register Address | Bit | Type<br>Note 1 | Label  | Description                                                                                     |
|------------------|-----|----------------|--------|-------------------------------------------------------------------------------------------------|
| 0x08<br>EVENT_C  | 7   | R              | E_GPI7 | GPI event according to active state setting                                                     |
|                  | 6   | R              | E_GPI6 | GPI event according to active state setting                                                     |
|                  | 5   | R              | E_GPI5 | GPI event according to active state setting                                                     |
|                  | 4   | R              | E_GPI4 | GPI event according to active state setting                                                     |
|                  | 3   | R              | E_GPI3 | GPI event according to active state setting                                                     |
|                  | 2   | R              | E_GPI2 | GPI event according to active state setting / ADCIN3 high / low threshold exceeded caused event |
|                  | 1   | R              | E_GPI1 | GPI event according to active state setting / ADCIN2 high / low threshold exceeded caused event |
|                  | 0   | R              | E_GPI0 | GPI event according to active state setting / ADCIN1 high / low threshold exceeded caused event |

**Note 1** Cleared from the host by writing back the read value.

**Table 68: EVENT\_D**

| Register Address | Bit | Type<br>Note 1 | Label   | Description                                                                                       |
|------------------|-----|----------------|---------|---------------------------------------------------------------------------------------------------|
| 0x09<br>EVENT_D  | 7   | R              | E_GPI15 | GPI event according to active state setting                                                       |
|                  | 6   | R              | E_GPI14 | GPI event according to active state setting/Event caused from host addressing HS-2-WIRE interface |
|                  | 5   | R              | E_GPI13 | GPI event according to active state setting                                                       |
|                  | 4   | R              | E_GPI12 | GPI event according to active state setting                                                       |
|                  | 3   | R              | E_GPI11 | GPI event according to active state setting                                                       |
|                  | 2   | R              | E_GPI10 | GPI/PWR1_EN event according to active state setting                                               |
|                  | 1   | R              | E_GPI9  | GPI/PWR_EN event according to active state setting                                                |
|                  | 0   | R              | E_GPI8  | GPI/SYS_EN event according to active state setting                                                |

**Note 1** Cleared from the host by writing back the read value.

The nIRQ line is released only when all events have been cleared from the host processor by writing the read value into all registers with an asserted event bit.

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Table 69: IRQ\_MASK\_A

| Register Address   | Bit | Type | Label     | Description                                         |
|--------------------|-----|------|-----------|-----------------------------------------------------|
| 0x0A<br>IRQ_MASK_A | 7:5 | R/W  | Reserved  |                                                     |
|                    | 4   | R/W  | M_SEQ_RDY | Mask nIRQ from finishing power sequencing           |
|                    | 3   | R/W  | M_ADC_RDY | Mask ADC manual conversion result ready caused nIRQ |
|                    | 2   | R/W  | M_TICK    | Mask RTC tick caused nIRQ                           |
|                    | 1   | R/W  | M_ALARM   | Mask RTC alarm caused nIRQ                          |
|                    | 0   | R/W  | M_nONKEY  | Mask nONKEY caused nIRQ                             |

Table 70: IRQ\_MASK\_B

| Register Address   | Bit | Type | Label      | Description                                                    |
|--------------------|-----|------|------------|----------------------------------------------------------------|
| 0x0B<br>IRQ_MASK_B | 7   | R/W  | M_VDD_WARN | Mask VDDFAULT_UPPER comparator triggered event                 |
|                    | 6   | R/W  | M_VDD_MON  | Mask V <sub>sys</sub> caused nIRQ                              |
|                    | 5   | R/W  | M_DVC_RDY  | Mask DVC voltage ramping triggered event                       |
|                    | 4   | R/W  | M_REG_UVOV | Mask events generated from regulator output voltage monitoring |
|                    | 3   | R/W  | M_LDO_LIM  | Mask LDO current limit exceeded caused nIRQ                    |
|                    | 2   | R/W  | M_COMP1V2  | Mask 1.2 V comparator caused nIRQ                              |
|                    | 1   | R/W  | M_TEMP     | Mask junction over temp caused nIRQ                            |
|                    | 0   | R/W  | M_WAKE     | Mask companion charger caused event                            |

Table 71: IRQ\_MASK\_C

| Register Address   | Bit | Type | Label  | Description                                                        |
|--------------------|-----|------|--------|--------------------------------------------------------------------|
| 0x0C<br>IRQ_MASK_C | 7   | R/W  | M_GPI7 | Mask GPI caused nIRQ                                               |
|                    | 6   | R/W  | M_GPI6 | Mask GPI caused nIRQ                                               |
|                    | 5   | R/W  | M_GPI5 | Mask GPI caused nIRQ                                               |
|                    | 4   | R/W  | M_GPI4 | Mask GPI caused nIRQ                                               |
|                    | 3   | R/W  | M_GPI3 | Mask GPI caused nIRQ                                               |
|                    | 2   | R/W  | M_GPI2 | Mask GPI caused / ADCIN3 high / low threshold exceeded caused nIRQ |
|                    | 1   | R/W  | M_GPI1 | Mask GPI caused / ADCIN2 high / low threshold exceeded caused nIRQ |
|                    | 0   | R/W  | M_GPI0 | Mask GPI caused / ADCIN1 high / low threshold exceeded caused nIRQ |

Table 72: IRQ\_MASK\_D

| Register Address   | Bit | Type | Label   | Description                    |
|--------------------|-----|------|---------|--------------------------------|
| 0x0D<br>IRQ_MASK_D | 7   | R/W  | M_GPI15 | Mask GPI caused nIRQ           |
|                    | 6   | R/W  | M_GPI14 | Mask GPI/HS-2-WIRE caused nIRQ |

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| Register Address | Bit | Type | Label          | Description                  |
|------------------|-----|------|----------------|------------------------------|
|                  | 5   | R/W  | <b>M_GPI13</b> | Mask GPI caused nIRQ         |
|                  | 4   | R/W  | <b>M_GPI12</b> | Mask GPI caused nIRQ         |
|                  | 3   | R/W  | <b>M_GPI11</b> | Mask GPI caused nIRQ         |
|                  | 2   | R/W  | <b>M_GPI10</b> | Mask GPI/PWR1_EN caused nIRQ |
|                  | 1   | R/W  | <b>M_GPI9</b>  | Mask GPI/PWR_EN caused nIRQ  |
|                  | 0   | R/W  | <b>M_GPI8</b>  | Mask GPI/SYS_EN caused nIRQ  |

Table 73: CONTROL\_A

| Register Address | Bit | Type | Label            | Description                                                                                                                                                   |
|------------------|-----|------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xE<br>CONTROL_A | 7   | R/W  | <b>CP_EN</b>     | When asserted charge pump for rail switches is enabled                                                                                                        |
|                  | 6   | R/W  | M_POWER1_EN      | Mask the update of POWER1_EN when writing to CONTROL_A                                                                                                        |
|                  | 5   | R/W  | M_POWER_EN       | Mask the update of POWER_EN when writing to CONTROL_A                                                                                                         |
|                  | 4   | R/W  | M_SYSTEM_EN      | Mask the update of SYSTEM_EN when writing to CONTROL_A                                                                                                        |
|                  | 3   | R/W  | <b>STANDBY</b>   | Clearing SYSTEM_EN/releasing port SYS_EN press will<br>0: completely power down to Slot 0 (Hibernate)<br>1: stop powering down at pointer PART_DOWN (Standby) |
|                  | 2   | R/W  | <b>POWER1_EN</b> | Target status of power domain POWER1: controlled from OTP/PM interface and port PWR1_EN                                                                       |
|                  | 1   | R/W  | <b>POWER_EN</b>  | Target status of power domain POWER: controlled from OTP/PM interface and port PWR_EN                                                                         |
|                  | 0   | R/W  | <b>SYSTEM_EN</b> | Target status of power domain SYSTEM: controlled from OTP/PM interface and port SYS_EN                                                                        |

Table 74: CONTROL\_B

| Register Address | Bit | Type | Label                 | Description                                                                                                                                                                                         |
|------------------|-----|------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xF<br>CONTROL_B | 7   | R/W  | <b>BUCK_SLOWSTART</b> | <b>Enables soft-start for buck converters (recommended for application instant-on with discharged battery and weak external supply)</b><br><a href="#">Note 1</a>                                   |
|                  | 6:5 | R/W  | <b>Reserved</b>       |                                                                                                                                                                                                     |
|                  | 4   | R/W  | <b>nONKEY_LOCK</b>    | 0: Half-current POWERDOWN mode<br><b>1: Wake-up from POWERDOWN mode requires the nONKEY signal being low for longer than selected in KEY_DELAY</b> (automatically cleared during power-up sequence) |

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| Register Address | Bit | Type | Label               | Description                                                                                                                                                                           |
|------------------|-----|------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 3   | R/W  | <b>nRES_MODE</b>    | 0: No assertion of nRESET for power down sequence<br><b>1: Assert nRESET before starting power down sequence (release after leaving POWERDOWN mode in case RESET_EVENT &lt; '11')</b> |
|                  | 2   | R/W  | <b>RES_BLINKING</b> | Enables (time limited) VDD_START triggered GPO11/4/15 flashing in case of no connected external supply                                                                                |
|                  | 1   | R/W  | <b>WATCHDOG_PD</b>  | <b>0: Discontinue Watchdog timer during POWERDOWN mode</b><br>1: Watchdog timer continues during POWERDOWN mode                                                                       |
|                  | 0   | R/W  | <b>CHG_SEL</b>      | <b>Port CHG_WAKE is connected to</b><br>0: Dialog charger WAKE port<br><b>1: Charger SAFE_OUT</b>                                                                                     |

**Note 1** Increases buck start-up time up to 3 ms.

**Table 75: CONTROL\_C**

| Register Address  | Bit | Type | Label             | Description                                                                                                                                                                              |
|-------------------|-----|------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x10<br>CONTROL_C | 7   | R/W  | <b>DEF_SUPPLY</b> | When asserted all supplies (except LDOCORE) are enabled/disabled from OTP default mode when entering sequencer Slot 0.                                                                   |
|                   | 6:5 | R/W  | <b>SLEW_RATE</b>  | DVC slewing (bucks and LDOs) is executed at<br>00: 10 mV every 4.0 $\mu$ s<br>01: 10 mV every 2.0 $\mu$ s<br><b>10: 10 mV every 1.0 <math>\mu</math>s</b><br>11: 10 mV every 0.5 $\mu$ s |
|                   | 4   | R/W  | <b>OTPREAD_EN</b> | 0: OTP read after POWERDOWN mode disabled<br><b>1: Power supplies are configured with OTP values when leaving POWERDOWN mode</b>                                                         |
|                   | 3   | R/W  | <b>AUTO_BOOT</b>  | <b>0: Start-up of power sequencer after progressing from RESET mode requires a valid wake-up event</b><br>1: PMIC automatically starts power sequencer after progressing from RESET mode |
|                   | 2:0 | R/W  | <b>DEBOUNCING</b> | GPI, nONKEY and nSHUTDOWN debounce time<br>000: no debounce time<br>001: 0.1 ms<br>010: 1.0 ms<br><b>011: 10.2 ms</b><br>100: 51.2 ms<br>101: 256 ms<br>110: 512 ms<br>111: 1024 ms      |

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Table 76: CONTROL\_D

| Register Address  | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                            |
|-------------------|-----|------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x11<br>CONTROL_D | 7:6 | R/W  | BLINK_DUR | GPO10/GPO11 flashing on-time<br>00: 10 ms<br><b>01: 20 ms</b><br>10: 40 ms<br>11: 20 ms double stroke (180 ms period)                                                                                                                                                                                                                                                                  |
|                   | 5:3 | R/W  | BLINK_FRQ | GPO11/4/15 flashing frequency<br>000: no blinking (GPO11/14/15 state selected via GPIOxx_MODE)<br>001: every second<br>010: every two seconds<br>011: every four seconds<br>100: every 180 ms (flicker mode)<br><b>101: every two seconds enabled by VDD_START</b><br>110: every four seconds enabled by VDD_START<br>111: every 180 ms enabled by VDD_START<br><a href="#">Note 1</a> |
|                   | 2:0 | R/W  | TWDSCALE  | <b>000: Watchdog disabled</b><br>001: 1x scaling applied to $t_{WD\_MAX}$ period<br>010: 2x<br>011: 4x<br>100: 8x<br>101: 16x<br>110: 32x<br>111: 64x                                                                                                                                                                                                                                  |

**Note 1** Blinking from OTP settings 001 to 100 continues as long as an active charger is connected to port CHG\_WAKE. In the absence of a battery charger a time limited blinking can be enabled via RES\_BLINKING.

Table 77: CONTROL\_E

| Register Address  | Bit | Type | Label      | Description                                                                                                                                                                                                         |
|-------------------|-----|------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x12<br>CONTROL_E | 7   | R/W  | V_LOCK     | <b>0: Allows host writes into registers 0x81 to 0x120</b><br>1: Disables register 0x81 to 0x120 re-programming from host interfaces                                                                                 |
|                   | 6   | R/W  | PM_FB3_PIN | <b>0: 2nd 32 kHz signal output</b><br>1: Feedback pin is used as an input signal to stop and start the vibration motor (active low nVIB_BRAKE)                                                                      |
|                   | 5   | R/W  | PM_FB2_PIN | <b>0: Feedback pin indicates the status of regulators being selected for voltage supervision (PWR_OK)</b><br>1: Feedback pin is used as KEEP_ACT signal for the Watchdog unit                                       |
|                   | 4   | R/W  | PM_FB1_PIN | <b>0: Feedback pin indicates the detection of a wake-up event (EXT_WAKEUP)</b><br>1: Feedback pin is used as an indicator, signaling via low level ongoing power mode transitions (power sequencer and DVC) (READY) |
|                   | 3   | R/W  | ECO_MODE   | When asserted DA9063 is armed for the pulsed mode when entering RESET                                                                                                                                               |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label              | Description                                                                                                                                                                   |
|------------------|-----|------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 2   | R/W  | <b>RTC_EN</b>      | Enables the power supply of the 32 kHz oscillator and RTC (for DA9063 the DELIVERY mode if cleared under certain pre-conditions, locked from the assertion of control MONITOR |
|                  | 1   | R/W  | <b>RTC_MODE_SD</b> | When asserted all supplies (including LDOCORE) and functional blocks except of the RTC are disabled when reaching RESET mode with a VDDFAULT condition                        |
|                  | 0   | R/W  | <b>RTC_MODE_PD</b> | When asserted all supplies (including LDOCORE) and functional blocks except of the RTC are disabled when reaching POWERDOWN mode                                              |

Table 78: CONTROL\_F

| Register Address  | Bit | Type | Label           | Description                                                                                                                  |
|-------------------|-----|------|-----------------|------------------------------------------------------------------------------------------------------------------------------|
| 0x13<br>CONTROL_F | 7:3 | R/W  | Reserved        |                                                                                                                              |
|                   | 2   | R/W  | <b>WAKE_UP</b>  | If set to 1 PMU wakes up from POWERDOWN mode. The bit is cleared back to 0 automatically 16 sec after entering ACTIVE mode   |
|                   | 1   | R/W  | <b>SHUTDOWN</b> | If set to 1 the sequencer powers down to RESET mode. The bit is cleared back to 0 automatically when entering the RESET mode |
|                   | 0   | R/W  | <b>WATCHDOG</b> | If set to 1 watchdog timer is reset. The bit is cleared back to 0 automatically.                                             |

Table 79: PD\_DIS

| Register Address | Bit | Type | Label                | Description                                                                                                                                                                                                          |
|------------------|-----|------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x14<br>PD_DIS   | 7   | R/W  | <b>PMCONT_DIS</b>    | <b>0: SYS_EN, PWR_EN, PWR1_EN enabled during power down</b><br>1: Auto-Disable of SYS_EN, PWR_EN and PWR1_EN during POWERDOWN mode and force the detection hidden transition when re-enabling the control from ports |
|                  | 6   | R/W  | <b>OUT_32K_PAUSE</b> | <b>0: Enables OUT_32K during power down</b><br>1: Auto-Disable OUT_32K output buffer during POWERDOWN mode                                                                                                           |
|                  | 5   | R/W  | <b>BBAT_DIS</b>      | <b>0: Enables Backup battery charger during POWERDOWN mode</b><br>1: Auto-disable backup battery charger during power down                                                                                           |
|                  | 4   | R/W  | <b>CLDR_PAUSE</b>    | 0: Calendar/Clock readout registers are updated during POWERDOWN mode<br><b>1: Update of Calendar/Clock readout registers is paused during POWERDOWN mode</b>                                                        |
|                  | 3   | R/W  | <b>HS2WIRE_DIS</b>   | <b>0: HS-2-WIRE not disabled during power down</b><br>1: Auto-disable of HS-2-WIRE interface during POWERDOWN mode                                                                                                   |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                                           |
|------------------|-----|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 2   | R/W  | PMIF_DIS    | <b>0: Power manager interface not disabled during power down</b><br>1: Auto-disable of power manager interface during POWERDOWN mode                                                                                                                                                                  |
|                  | 1   | R/W  | GPADC_PAUSE | 0: ADC measurements continue during power down as configured<br><b>1: Auto-PAUSE auto measurements on A0, A1, A2 and A3 and manual measurement during POWERDOWN mode; if no autonomous auto-measurements are required (V<sub>sys</sub> from vibration motor driver) switch off the ADC completely</b> |
|                  | 0   | R/W  | GPI_DIS     | <b>0: GPIO extender enabled during power down</b><br>1: Auto-disable of features configured as GPI pins during POWERDOWN mode and force the detection hidden transition when re-enabling the pin                                                                                                      |

**Note 1** When the related ID is configured to be  $1 < PD\_DIS\_STEP \leq MAX\_COUNT$  the value of the above controls define whether functions are switched on when entering POWERDOWN mode from POR or wait until ID PD\_DIS\_STEP is processed.

### A.2.2 GPIO Control

Table 80: GPIO\_0\_1

| Register Address | Bit | Type | Label      | Description                                                                                                                                                                     |
|------------------|-----|------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x15<br>GPIO_0_1 | 7   | R/W  | GPIO1_WEN  | <b>0: Passive to active transition triggers a wake-up</b><br>1: Wake-up suppressed                                                                                              |
|                  | 6   | R/W  | GPIO1_TYPE | <b>0: GPI: active low</b><br>GPO: supplied from VDD_IO1<br><b>1: GPI: active high</b><br>GPO: supplied from VDD_IO2                                                             |
|                  | 5:4 | R/W  | GPIO1_PIN  | PIN assigned to<br><b>00: ADCIN2/1.2 V comparator</b><br>01: GPI (optional regulator HW control)<br>10: GPO mode controlled (Open drain)<br>11: GPO mode controlled (Push-pull) |
|                  | 3   | R/W  | GPIO0_WEN  | 0: Passive to active transition triggers a wake-up<br>1: Wake-up suppressed                                                                                                     |
|                  | 2   | R/W  | GPIO0_TYPE | 0: GPI: active low<br>GPO: supplied from VDD_IO1<br><b>1: GPI: active high</b><br>GPO: supplied from VDD_IO2                                                                    |
|                  | 1:0 | R/W  | GPIO0_PIN  | PIN assigned to<br><b>00: ADCIN1</b><br>01: GPI<br>10: GPO mode controlled (Open drain)<br>11: GPO mode controlled (Push-pull)                                                  |

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Table 81: GPIO\_2\_3

| Register Address | Bit | Type | Label      | Description                                                                                                                                                        |
|------------------|-----|------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x16<br>GPIO_2_3 | 7   | R/W  | GPIO3_WEN  | 0: Passive to active transition triggers a wake-up<br>1: Wake-up suppressed                                                                                        |
|                  | 6   | R/W  | GPIO3_TYPE | 0: GPI: active low<br>GPO: supplied from VDD_IO1<br>1: GPI: active high<br>GPO: supplied from VDD_IO2                                                              |
|                  | 5:4 | R/W  | GPIO3_PIN  | PIN assigned to<br><b>00: CORE_SWG</b><br>01: GPI<br>10: GPO mode controlled (Open drain)<br>11: GPO mode controlled (Push-pull)                                   |
|                  | 3   | R/W  | GPIO2_WEN  | 0: Passive to active transition triggers a wake-up<br>1: Wake-up suppressed                                                                                        |
|                  | 2   | R/W  | GPIO2_TYPE | 0: GPI: active low<br>GPO: supplied from VDD_IO1<br><b>1: GPI: active high</b><br>GPO: supplied from VDD_IO2                                                       |
|                  | 1:0 | R/W  | GPIO2_PIN  | PIN assigned to<br>00: ADCIN3<br><b>01: GPI (optional regulator HW control)</b><br>10: GPO Sequencer controlled (Push-pull)<br>11: GPO mode controlled (Push-pull) |

Table 82: GPIO\_4\_5

| Register Address | Bit | Type | Label      | Description                                                                                                                      |
|------------------|-----|------|------------|----------------------------------------------------------------------------------------------------------------------------------|
| 0x17<br>GPIO_4_5 | 7   | R/W  | GPIO5_WEN  | 0: Passive to active transition triggers a wake-up<br>1: Wake-up suppressed                                                      |
|                  | 6   | R/W  | GPIO5_TYPE | 0: GPI: active low<br>GPO: supplied from VDD_IO1<br>1: GPI: active high<br>GPO: supplied from VDD_IO2                            |
|                  | 5:4 | R/W  | GPIO5_PIN  | PIN assigned to<br><b>00: PERI_SWG</b><br>01: GPI<br>10: GPO mode controlled (Open drain)<br>11: GPO mode controlled (Push-pull) |
|                  | 3   | R/W  | GPIO4_WEN  | 0: Passive to active transition triggers a wake-up<br>1: Wake-up suppressed                                                      |
|                  | 2   | R/W  | GPIO4_TYPE | 0: GPI: active low<br>GPO: supplied from VDD_IO1<br>1: GPI: active high<br>GPO: supplied from VDD_IO2                            |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label     | Description                                                                                                                      |
|------------------|-----|------|-----------|----------------------------------------------------------------------------------------------------------------------------------|
|                  | 1:0 | R/W  | GPIO4_PIN | PIN assigned to<br><b>00: CORE_SWS</b><br>01: GPI<br>10: GPO mode controlled (Open drain)<br>11: GPO mode controlled (Push-pull) |

Table 83: GPIO\_6\_7

| Register Address | Bit | Type | Label      | Description                                                                                                                          |
|------------------|-----|------|------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 0x18<br>GPIO_6_7 | 7   | R/W  | GPIO7_WEN  | 0: Passive to active transition triggers a wake-up<br>1: Wake-up suppressed                                                          |
|                  | 6   | R/W  | GPIO7_TYPE | 0: GPI: active low<br><b>GPO: supplied from VDD_IO1</b><br>1: GPI: active high<br>GPO: supplied from VDD_IO2                         |
|                  | 5:4 | R/W  | GPIO7_PIN  | PIN assigned to<br>00: Reserved<br>01: GPI<br><b>10: GPO Sequencer controlled (Push-pull)</b><br>11: GPO mode controlled (Push-pull) |
|                  | 3   | R/W  | GPIO6_WEN  | 0: Passive to active transition triggers a wake-up<br>1: Wake-up suppressed                                                          |
|                  | 2   | R/W  | GPIO6_TYPE | 0: GPI: active low<br>GPO: supplied from VDD_IO1<br>1: GPI: active high<br>GPO: supplied from VDD_IO2                                |
|                  | 1:0 | R/W  | GPIO6_PIN  | PIN assigned to<br><b>00: PERI_SWS</b><br>01: GPI<br>10: GPO mode controlled (Open drain)<br>11: GPO mode controlled (Push-pull)     |

Table 84: GPIO\_8\_9

| Register Address | Bit | Type | Label      | Description                                                                                                                                                         |
|------------------|-----|------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x19<br>GPIO_8_9 | 7   | R/W  | GPIO9_WEN  | <b>0: Passive to active transition triggers a wake-up</b><br>1: Wake-up suppressed                                                                                  |
|                  | 6   | R/W  | GPIO9_TYPE | <b>0: GPI/PWR_EN: active low</b><br>GPO: supplied from VDD_IO1<br>1: GPI/PWR_EN: active high<br>GPO: supplied from VDD_IO2                                          |
|                  | 5:4 | R/W  | GPIO9_PIN  | PIN and status register bit assigned to<br>00: GPI with PWR_EN<br><b>01: GPI</b><br>10: GPO Sequencer controlled (Push-pull)<br>11: GPO mode controlled (Push-pull) |
|                  | 3   | R/W  | GPIO8_WEN  | <b>0: Passive to active transition triggers a wake-up</b><br>1: Wake-up suppressed                                                                                  |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label             | Description                                                                                                                                                         |
|------------------|-----|------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 2   | R/W  | <b>GPIO8_TYPE</b> | <b>0: GPI/SYS_EN: active low</b><br>GPO: supplied from external/VDD_IO1<br><b>1: GPI/SYS_EN: active high</b><br>GPO: supplied from VDD_IO2                          |
|                  | 1:0 | R/W  | <b>GPIO8_PIN</b>  | PIN and status register bit assigned to<br>00: GPI with SYS_EN<br><b>01: GPI</b><br>10: GPO Sequencer controlled (Push-pull)<br>11: GPO mode controlled (Push-pull) |

Table 85: GPIO\_10\_11

| Register Address   | Bit | Type | Label       | Description                                                                                                                                                              |
|--------------------|-----|------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1A<br>GPIO_10_11 | 7   | R/W  | GPIO11_WEN  | 0: Passive to active transition triggers a wake-up<br>1: Wake-up suppressed                                                                                              |
|                    | 6   | R/W  | GPIO11_TYPE | <b>0: GPI: active low</b><br><b>GPO: supplied from external/VDD_IO1</b><br>1: GPI: active high<br>GPO: supplied from VDD_IO2                                             |
|                    | 5:4 | R/W  | GPIO11_PIN  | PIN assigned to<br>00: GPO (Open drain, with optional blinking)<br>01: GPI<br><b>10: GPO GPO Sequencer controlled (Push-pull)</b><br>11: GPO mode controlled (Push-pull) |
|                    | 3   | R/W  | GPIO10_WEN  | <b>0: Passive to active transition triggers a wake-up</b><br>1: Wake-up suppressed                                                                                       |
|                    | 2   | R/W  | GPIO10_TYPE | <b>0: GPI/PWR1_EN: active low</b><br>GPO: supplied from external/VDD_IO1<br>1: GPI/PWR1_EN: active high<br>GPO: supplied from VDD_IO2                                    |
|                    | 1:0 | R/W  | GPIO10_PIN  | PIN and status register bit assigned to<br>00: GPI with PWR1_EN<br><b>01: GPI</b><br>10: GPO (Open drain)<br>11: GPO mode controlled (Push-pull )                        |

Table 86: GPIO\_12\_13

| Register Address   | Bit | Type | Label              | Description                                                                                                                                |
|--------------------|-----|------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1B<br>GPIO_12_13 | 7   | R/W  | <b>GPIO13_WEN</b>  | 0: Passive to active transition triggers a wake-up<br>1: Wake-up suppressed                                                                |
|                    | 6   | R/W  | <b>GPIO13_TYPE</b> | <b>0: GPI: active low</b><br><b>GPO/GP_FB1: supplied from external/VDD_IO1</b><br>1: GPI: active high<br>GPO/GP_FB1: supplied from VDD_IO2 |

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| Register Address | Bit | Type | Label              | Description                                                                                                                                                                                                                                                                       |
|------------------|-----|------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 5:4 | R/W  | <b>GPIO13_PIN</b>  | PIN and status register bit assigned to<br>00: GPO controlled by state of GP_FB1 (EXT_WAKEUP/READY) (Push-pull)<br>01: GPI (optional regulator HW control)<br>10: GPO controlled by state of GP_FB1 (EXT_WAKEUP/READY) (Open drain)<br><b>11: GPO mode controlled (Push-pull)</b> |
|                  | 3   | R/W  | <b>GPIO12_WEN</b>  | 0: Passive to active transition triggers a wake-up<br>1: Wake-up suppressed                                                                                                                                                                                                       |
|                  | 2   | R/W  | <b>GPIO12_TYPE</b> | <b>0: GPI: active low</b><br><b>GPO/ nVDD_FAULT/V<sub>sys</sub> monitor: supplied from VDD_IO1</b><br>1: GPI: active high<br>GPO/DD_FAULT/V <sub>sys</sub> monitor: supplied from VDD_IO2                                                                                         |
|                  | 1:0 | R/W  | <b>GPIO12_PIN</b>  | PIN assigned to<br><b>00: nVDD_FAULT (Push-pull)</b><br>01: GPI<br>10: GPO controlled by the state of V <sub>sys</sub> monitor (Push-pull)<br>11: GPO mode controlled (Push-pull)                                                                                                 |

Table 87: GPIO\_14\_15

| Register Address   | Bit | Type | Label              | Description                                                                                                                                                                                                        |
|--------------------|-----|------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1C<br>GPIO_14_15 | 7   | R/W  | <b>GPIO15_WEN</b>  | <b>0: Passive to active transition triggers a wake-up</b><br>1: Wake-up suppressed                                                                                                                                 |
|                    | 6   | R/W  | <b>GPIO15_TYPE</b> | <b>0: GPI: active low</b><br><b>GPO: supplied from external/VDD_IO1</b><br>1: GPI: active high<br>GPO: supplied from VDD_IO2                                                                                       |
|                    | 5:4 | R/W  | <b>GPIO15_PIN</b>  | PIN assigned to<br>00: GPO (Open drain, with optional blinking)<br>01: GPI<br><b>10: CLK (configured via GPIO14_PIN)</b><br>11: GPO mode controlled (Open drain)                                                   |
|                    | 3   | R/W  | <b>GPIO14_WEN</b>  | <b>0: Passive to active transition triggers a wake-up</b><br>1: Wake-up suppressed                                                                                                                                 |
|                    | 2   | R/W  | <b>GPIO14_TYPE</b> | <b>0: GPI: active low</b><br><b>GPO: supplied from external/VDD_IO1</b><br>DATA/CLK supplied from VDD_IO1 (Note 1)<br>1: GPI: active high<br>GPO: supplied from VDD_IO2<br>DATA/CLK supplied from VDD_IO2 (Note 1) |
|                    | 1:0 | R/W  | <b>GPIO14_PIN</b>  | PIN assigned to<br>00: GPO(Open drain, with optional blinking)<br>01: GPI<br><b>10: DATA (assigns GPIO15_PIN to CLK)</b><br>11: GPO mode controlled (Push-pull)                                                    |

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**Note 1** When using as HS-2-WIRE IF input logic levels are derived from VDDCORE.

**Table 88: GPIO\_MODE0\_7**

| Register Address     | Bit | Type | Label       | Description                                                                                                                                                                               |
|----------------------|-----|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1D<br>GPIO_MODE0_7 | 7   | R/W  | GPIO7_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level (active low for sequencer control)<br>1: GPI: debouncing on<br>GPO: Sets output to high level (active high for sequencer control) |
|                      | 6   | R/W  | GPIO6_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level (active low for sequencer control)<br>1: GPI: debouncing on<br>GPO: Sets output to high level (active high for sequencer control) |
|                      | 5   | R/W  | GPIO5_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level<br>1: GPI: debouncing on<br>GPO: Sets output to high level                                                                        |
|                      | 4   | R/W  | GPIO4_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level(active low for sequencer control)<br>1: GPI: debouncing on<br>GPO: Sets output to high level (active high for sequencer control)  |
|                      | 3   | R/W  | GPIO3_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level (active low for sequencer control)<br>1: GPI: debouncing on<br>GPO: Sets output to high level (active high for sequencer control) |
|                      | 2   | R/W  | GPIO2_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level<br>1: GPI: debouncing on<br>GPO: Sets output to high level                                                                        |
|                      | 1   | R/W  | GPIO1_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level<br>1: GPI: debouncing on<br>GPO: Sets output to high level                                                                        |
|                      | 0   | R/W  | GPIO0_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level<br>1: GPI: debouncing on<br>GPO: Sets output to high level                                                                        |

**Table 89: GPIO\_MODE8\_15**

| Register Address      | Bit | Type | Label        | Description                                                                                                                                                             |
|-----------------------|-----|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1E<br>GPIO_MODE8_15 | 7   | R/W  | GPIO15_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level (active high for blinking)<br>1: GPI: debouncing on<br>GPO: Sets output to high level (active low for blinking) |

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| Register Address | Bit | Type | Label        | Description                                                                                                                                                                                                                                 |
|------------------|-----|------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 6   | R/W  | GPIO14_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level (active high for blinking)<br>1: GPI:debouncing on<br>GPO: Sets output to high level (active low for blinking)                                                                      |
|                  | 5   | R/W  | GPIO13_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level (active low for GP_FB1)<br>1: GPI: debouncing on<br>GPO: Sets output to high level (active high for GP_FB1)                                                                         |
|                  | 4   | R/W  | GPIO12_ MODE | 0: GPI: debouncing off<br>GPO: Sets output to low level (active low for nVDD_FAULT, V <sub>sys</sub> monitor state)<br>1: GPI: debouncing on<br>GPO: Sets output to high level (active high for nVDD_FAULT, V <sub>sys</sub> monitor state) |
|                  | 3   | R/W  | GPIO11_ MODE | 0: GPI: : debouncing off<br>GPO: Sets output to low level (active high for blinking)<br>1: GPI: : debouncing on<br>GPO: Sets output to high level (active low for blinking)                                                                 |
|                  | 2   | R/W  | GPIO10_ MODE | 0: GPI/PWR1_EN: debouncing off<br>GPO: Sets output to low level<br>1: GPI/PWR1_EN: debouncing on<br>GPO: Sets output to high level                                                                                                          |
|                  | 1   | R/W  | GPIO9_ MODE  | 0: GPI/PWR_EN: debouncing off<br>GPO: Sets output to low level (active low for sequencer control)<br>1: GPI/PWR_EN debouncing on<br>GPO: Sets output to high level (active high for sequencer control)                                      |
|                  | 0   | R/W  | GPIO8_ MODE  | 0: GPI/SYS_EN: debouncing off<br>GPO: Sets output to low level<br>1: GPI/SYS_EN: debouncing on<br>GPO: Sets output to high level                                                                                                            |

Table 90: SWITCH\_CONT

| Register Address    | Bit | Type | Label       | Description                                                                                                                                                                                              |
|---------------------|-----|------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1F<br>SWITCH_CONT | 7   | R/W  | CP_EN_MODE  | Rail switch charge pump is enabled<br><b>0: static</b> (does not shut down, when all switches are open)<br>1: auto, CP enabled before closing the first switch, CP disabled after last switch was opened |
|                     | 6   | R/W  | CORE_SW_INT | Changes the CORE external switch controller into an internal switch between the output of BUCKCORE1 and port CORE_SWS/GPIO4                                                                              |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label       | Description                                                                                                                                                                                                                  |
|------------------|-----|------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 5:4 | R/W  | SWITCH_SR   | Maximum slew rate when closing the rail switch:<br><b>00: 1 mV/μs</b><br>01: 5 mV/μs<br>10: 10 mV/μs<br>11: as fast as possible                                                                                              |
|                  | 3:2 | R/W  | PERI_SW_GPI | GPIO closes PERI_SW on passive to active state transition, opens PERI_SW on active to passive state transition<br><b>00: Not controlled by GPIO</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                  | 1:0 | R/W  | CORE_SW_GPI | GPIO closes CORE_SW on passive to active state transition, opens CORE_SW on active to passive state transition<br><b>00: Not controlled by GPIO</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |

### A.2.3 Regulator Control

Table 91: BCORE2\_CONT

| Register Address                              | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                        |
|-----------------------------------------------|-----|------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x20<br>BCORE2_CONT<br><a href="#">Note 1</a> | 7   | R/W  | Reserved    |                                                                                                                                                                                                                                                                                    |
|                                               | 6:5 | R/W  | VBCORE2_GPI | GPIO select target voltage VBCORE2_A on passive to active transition, selects target voltage VBCORE2_B on active to passive transition (ramping)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                                               | 4   | R/W  | Reserved    |                                                                                                                                                                                                                                                                                    |
|                                               | 3   | R/W  | BCORE2_CONF | Sequencer target state of BCORE2_EN                                                                                                                                                                                                                                                |
|                                               | 2:1 | R/W  | BCORE2_GPI  | GPIO enables BUCKCORE2 on passive to active state transition, disables BUCKCORE2 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                           |
|                                               | 0   | R/W  | BCORE2_EN   | <b>0: BUCKCORE2 disabled</b><br>1: BUCKCORE2 enabled                                                                                                                                                                                                                               |

**Note 1** Disabled in BUCKCORE dual-phase mode.

## System PMIC for Mobile and Automotive Applications

Table 92: BCORE1\_CONT

| Register Address    | Bit | Type | Label        | Description                                                                                                                                                                                                                                                                        |
|---------------------|-----|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x21<br>BCORE1_CONT | 7   | R/W  | CORE_SW_CONF | Sequencer target state of CORE_SW_EN                                                                                                                                                                                                                                               |
|                     | 6:5 | R/W  | VBCORE1_GPI  | GPIO select target voltage VBCORE1_A on passive to active transition, selects target voltage VBCORE1_B on active to passive transition (ramping)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                     | 4   | R/W  | CORE_SW_EN   | <b>0: CORE_SW opened</b><br>1: CORE_SW closed                                                                                                                                                                                                                                      |
|                     | 3   | R/W  | BCORE1_CONF  | Sequencer target state of BCORE1_EN                                                                                                                                                                                                                                                |
|                     | 2:1 | R/W  | BCORE1_GPI   | GPIO enables BUCKCORE1 on passive to active state transition, disables BUCKCORE1 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                           |
|                     | 0   | R/W  | BCORE1_EN    | <b>0: BUCKCORE1 disabled</b><br>1: BUCKCORE1 enabled                                                                                                                                                                                                                               |

Table 93: BPRO\_CONT

| Register Address  | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                    |
|-------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x22<br>BPRO_CONT | 7   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                |
|                   | 6:5 | R/W  | VBPRO_GPI | GPIO select target voltage VBPRO_A on passive to active transition, selects target voltage VBPRO_B on active to passive transition (ramping)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                   | 4   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                |
|                   | 3   | R/W  | BPRO_CONF | Sequencer target state of BPRO_EN                                                                                                                                                                                                                                              |
|                   | 2:1 | R/W  | BPRO_GPI  | GPIO enables BUCKPRO on passive to active state transition, disables BUCKPRO on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                           |
|                   | 0   | R/W  | BPRO_EN   | <b>0: BUCKPRO disabled</b><br>1: BUCKPRO enabled                                                                                                                                                                                                                               |

## System PMIC for Mobile and Automotive Applications

Table 94: BMEM\_CONT

| Register Address  | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                    |
|-------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x23<br>BMEM_CONT | 7   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                |
|                   | 6:5 | R/W  | VBMEM_GPI | GPIO select target voltage VBMEM_A on passive to active transition, selects target voltage VBMEM_B on active to passive transition (ramping)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                   | 4   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                |
|                   | 3   | R/W  | BMEM_CONF | Sequencer target state of BMEM_EN in case of being a default supply)                                                                                                                                                                                                           |
|                   | 2:1 | R/W  | BMEM_GPI  | GPIO enables BUCKMEM on passive to active state transition, disables BUCKMEM on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                           |
|                   | 0   | R/W  | BMEM_EN   | <b>0: BUCKMEM disabled</b><br>1: BUCKMEM enabled                                                                                                                                                                                                                               |

Table 95: BIO\_CONT

| Register Address | Bit | Type | Label    | Description                                                                                                                                                                                                                                                                  |
|------------------|-----|------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x24<br>BIO_CONT | 7   | R/W  | Reserved |                                                                                                                                                                                                                                                                              |
|                  | 6:5 | R/W  | VBIO_GPI | GPIO select target voltage VBIO_A on passive to active transition, selects target voltage VBIO_B on active to passive transition (ramping)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                  | 4   | R/W  | Reserved |                                                                                                                                                                                                                                                                              |
|                  | 3   | R/W  | BIO_CONF | Sequencer target state of BIO_EN                                                                                                                                                                                                                                             |
|                  | 2:1 | R/W  | BIO_GPI  | GPIO enables BUCKIO on passive to active state transition, disables BUCKIO on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                           |
|                  | 0   | R/W  | BIO_EN   | <b>0: BUCKIO disabled</b><br>1: BUCKIO enabled                                                                                                                                                                                                                               |

## System PMIC for Mobile and Automotive Applications

Table 96: BPERI\_CONT

| Register Address   | Bit | Type | Label        | Description                                                                                                                                                                                                                                                                      |
|--------------------|-----|------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x25<br>BPERI_CONT | 7   | R/W  | PERI_SW_CONF | Sequencer target state of PERI_SW_EN                                                                                                                                                                                                                                             |
|                    | 6:5 | R/W  | VBPERI_GPI   | GPIO select target voltage VBPERI_A on passive to active transition, selects target voltage VBPERI_B on active to passive transition (ramping)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                    | 4   | R/W  | PERI_SW_EN   | <b>0: PERI_SW opened</b><br>1: PERI_SW closed                                                                                                                                                                                                                                    |
|                    | 3   | R/W  | BPERI_CONF   | Sequencer target state of BPERI_EN                                                                                                                                                                                                                                               |
|                    | 2:1 | R/W  | BPERI_GPI    | GPIO enables BUCKPERI on passive to active state transition, disables BUCKPERI on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                           |
|                    | 0   | R/W  | BPERI_EN     | <b>0: BUCKPERI disabled</b><br>1: BUCKPERI enabled                                                                                                                                                                                                                               |

Table 97: LDO1\_CONT

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                    |
|-------------------|-----|------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x26<br>LDO1_CONT | 7   | R/W  | LDO1_CONF   | Sequencer target state of LDO1_EN                                                                                                                                                                                                                                              |
|                   | 6:5 | R/W  | VLDO1_GPI   | GPIO select target voltage VLDO1_A on passive to active transition, selects target voltage VLDO1_B on active to passive transition (ramping)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                   | 4   | R/W  | Reserved    |                                                                                                                                                                                                                                                                                |
|                   | 3   | R/W  | LDO1_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                                                                               |
|                   | 2:1 | R/W  | LDO1_GPI    | GPIO enables LDO1 on passive to active state transition, disables LDO1 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                                 |
|                   | 0   | R/W  | LDO1_EN     | <b>0: LDO1 disabled</b><br>1: LDO1 enabled                                                                                                                                                                                                                                     |

## System PMIC for Mobile and Automotive Applications

Table 98: LDO2\_CONT

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                    |
|-------------------|-----|------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x27<br>LDO2_CONT | 7   | R/W  | LDO2_CONF   | Sequencer target state of LDO2_EN                                                                                                                                                                                                                                              |
|                   | 6:5 | R/W  | VLDO2_GPI   | GPIO select target voltage VLDO2_A on passive to active transition, selects target voltage VLDO2_B on active to passive transition (ramping)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                   | 4   | R/W  | Reserved    |                                                                                                                                                                                                                                                                                |
|                   | 3   | R/W  | LDO2_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                                                                               |
|                   | 2:1 | R/W  | LDO2_GPI    | GPIO enables LDO2 on passive to active state transition, disables LDO2 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                                 |
|                   | 0   | R/W  | LDO2_EN     | <b>0: LDO2 disabled</b><br>1: LDO2 enabled                                                                                                                                                                                                                                     |

Table 99: LDO3\_CONT

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                    |
|-------------------|-----|------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x28<br>LDO3_CONT | 7   | R/W  | LDO3_CONF   | Sequencer target state of LDO3_EN                                                                                                                                                                                                                                              |
|                   | 6:5 | R/W  | VLDO3_GPI   | GPIO select target voltage VLDO3_A on passive to active transition, selects target voltage VLDO3_B on active to passive transition (ramping)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                   | 4   | R/W  | Reserved    |                                                                                                                                                                                                                                                                                |
|                   | 3   | R/W  | LDO3_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                                                                               |
|                   | 2:1 | R/W  | LDO3_GPI    | GPIO enables LDO3 on passive to active state transition, disables LDO3 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                                 |
|                   | 0   | R/W  | LDO3_EN     | <b>0: LDO3 disabled</b><br>1: LDO3 enabled                                                                                                                                                                                                                                     |

## System PMIC for Mobile and Automotive Applications

Table 100: LDO4\_CONT

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                    |
|-------------------|-----|------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x29<br>LDO4_CONT | 7   | R/W  | LDO4_CONF   | Sequencer target state of LDO4_EN                                                                                                                                                                                                                                              |
|                   | 6:5 | R/W  | VLDO4_GPI   | GPIO select target voltage VLDO4_A on passive to active transition, selects target voltage VLDO4_B on active to passive transition (ramping)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                   | 4   | R/W  | Reserved    |                                                                                                                                                                                                                                                                                |
|                   | 3   | R/W  | LDO4_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                                                                               |
|                   | 2:1 | R/W  | LDO4_GPI    | GPIO enables LDO4 on passive to active state transition, disables LDO4 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                                 |
|                   | 0   | R/W  | LDO4_EN     | <b>0: LDO4 disabled</b><br>1: LDO4 enabled                                                                                                                                                                                                                                     |

Table 101: LDO5\_CONT

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                                     |
|-------------------|-----|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x2A<br>LDO5_CONT | 7   | R/W  | LDO5_CONF   | Sequencer target state of LDO5_EN                                                                                                                                                                                                                                                               |
|                   | 6:5 | R/W  | VLDO5_GPI   | GPIO select target voltage VLDO5_A on passive to active transition, selects target voltage VLDO5_B on active to passive transition (immediate voltage change)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                   | 4   | R/W  | VLDO5_SEL   | LDO5 voltage is selected from (immediate change):<br><b>0: VLDO5_A</b><br>1: VLDO5_B                                                                                                                                                                                                            |
|                   | 3   | R/W  | LDO5_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                                                                                                |
|                   | 2:1 | R/W  | LDO5_GPI    | GPIO enables LDO5 on passive to active state transition, disables LDO6 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                                                  |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label   | Description                         |
|------------------|-----|------|---------|-------------------------------------|
|                  | 0   | R/W  | LDO5_EN | 0: LDO5 disabled<br>1: LDO5 enabled |

Table 102: LDO6\_CONT

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                                     |
|-------------------|-----|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x2B<br>LDO6_CONT | 7   | R/W  | LDO6_CONF   | Sequencer target state of LDO6_EN                                                                                                                                                                                                                                                               |
|                   | 6:5 | R/W  | VLDO6_GPI   | GPIO select target voltage VLDO6_A on passive to active transition, selects target voltage VLDO6_B on active to passive transition (immediate voltage change)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                   | 4   | R/W  | VLDO6_SEL   | LDO6 voltage is selected from (immediate change):<br><b>0: VLDO6_A</b><br>1: VLDO6_B                                                                                                                                                                                                            |
|                   | 3   | R/W  | LDO6_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                                                                                                |
|                   | 2:1 | R/W  | LDO6_GPI    | GPIO enables LDO6 on passive to active state transition, disables LDO6 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                                                  |
|                   | 0   | R/W  | LDO6_EN     | <b>0: LDO6 disabled</b><br>1: LDO6 enabled                                                                                                                                                                                                                                                      |

Table 103: LDO7\_CONT

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                                     |
|-------------------|-----|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x2C<br>LDO7_CONT | 7   | R/W  | LDO7_CONF   | Sequencer target state of LDO7_EN                                                                                                                                                                                                                                                               |
|                   | 6:5 | R/W  | VLDO7_GPI   | GPIO select target voltage VLDO7_A on passive to active transition, selects target voltage VLDO7_B on active to passive transition (immediate voltage change)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                   | 4   | R/W  | VLDO7_SEL   | LDO7 voltage is selected from (immediate change):<br><b>0: VLDO7_A</b><br>1: VLDO7_B                                                                                                                                                                                                            |
|                   | 3   | R/W  | LDO7_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                                                                                                |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label    | Description                                                                                                                                                                                                                                    |
|------------------|-----|------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 2:1 | R/W  | LDO7_GPI | GPIO enables LDO7 on passive to active state transition, disables LDO7 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                  | 0   | R/W  | LDO7_EN  | <b>0: LDO7 disabled</b><br>1: LDO7 enabled                                                                                                                                                                                                     |

Table 104: LDO8\_CONT

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                                     |
|-------------------|-----|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x2D<br>LDO8_CONT | 7   | R/W  | LDO8_CONF   | Sequencer target state of LDO8_EN                                                                                                                                                                                                                                                               |
|                   | 6:5 | R/W  | VLDO8_GPI   | GPIO select target voltage VLDO8_A on passive to active transition, selects target voltage VLDO8_B on active to passive transition (immediate voltage change)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                   | 4   | R/W  | VLDO8_SEL   | LDO8 voltage is selected from (immediate change):<br><b>0: VLDO8_A</b><br>1: VLDO8_B                                                                                                                                                                                                            |
|                   | 3   | R/W  | LDO8_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                                                                                                |
|                   | 2:1 | R/W  | LDO8_GPI    | GPIO enables LDO8 on passive to active state transition, disables LDO8 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                                                  |
|                   | 0   | R/W  | LDO8_EN     | <b>0: LDO8 disabled</b><br>1: LDO8 enabled                                                                                                                                                                                                                                                      |

Table 105: LDO9\_CONT

| Register Address  | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                     |
|-------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x2E<br>LDO9_CONT | 7   | R/W  | LDO9_CONF | Sequencer target state of LDO9_EN                                                                                                                                                                                                                                                               |
|                   | 6:5 | R/W  | VLDO9_GPI | GPIO select target voltage VLDO9_A on passive to active transition, selects target voltage VLDO9_B on active to passive transition (immediate voltage change)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label       | Description                                                                                                                                                                                                                                                         |
|------------------|-----|------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 4   | R/W  | VLDO9_SEL   | LDO9 voltage is selected from (immediate change):<br><b>0: VLDO9_A</b><br><b>1: VLDO9_B</b>                                                                                                                                                                         |
|                  | 3   | R/W  | LDO9_PD_DIS | <b>0: Enable pull-down resistor</b><br><b>1: No pull-down resistor in disabled mode</b>                                                                                                                                                                             |
|                  | 2:1 | R/W  | LDO9_GPI    | GPIO enables LDO9 on passive to active state transition, disables LDO9 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br><b>01: GPIO1 controlled</b><br><b>10: GPIO2 controlled</b><br><b>11: GPIO13 controlled</b> |
|                  | 0   | R/W  | LDO9_EN     | <b>0: LDO9 disabled</b><br><b>1: LDO9 enabled</b>                                                                                                                                                                                                                   |

Table 106: LDO10\_CONT

| Register Address   | Bit | Type | Label        | Description                                                                                                                                                                                                                                                                                                            |
|--------------------|-----|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x2F<br>LDO10_CONT | 7   | R/W  | LDO10_CONF   | Sequencer target state of LDO10_EN                                                                                                                                                                                                                                                                                     |
|                    | 6:5 | R/W  | VLDO10_GPI   | GPIO select target voltage VLDO10_A on passive to active transition, selects target voltage VLDO10_B on active to passive transition (immediate voltage change)<br><b>00: Not controlled by GPIO (sequencer control)</b><br><b>01: GPIO1 controlled</b><br><b>10: GPIO2 controlled</b><br><b>11: GPIO13 controlled</b> |
|                    | 4   | R/W  | VLDO10_SEL   | LDO10 voltage is selected from (immediate change):<br><b>0: VLDO10_A</b><br><b>1: VLDO10_B</b>                                                                                                                                                                                                                         |
|                    | 3   | R/W  | LDO10_PD_DIS | <b>0: Enable pull-down resistor</b><br><b>1: No pull-down resistor in disabled mode</b>                                                                                                                                                                                                                                |
|                    | 2:1 | R/W  | LDO10_GPI    | GPIO enables LDO10 on passive to active state transition, disables LDO10 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br><b>01: GPIO1 controlled</b><br><b>10: GPIO2 controlled</b><br><b>11: GPIO13 controlled</b>                                                  |
|                    | 0   | R/W  | LDO10_EN     | <b>0: LDO10 disabled</b><br><b>1: LDO10 enabled</b>                                                                                                                                                                                                                                                                    |

## System PMIC for Mobile and Automotive Applications

Table 107: LDO11\_CONT

| Register Address   | Bit | Type | Label        | Description                                                                                                                                                                                                                                                                                       |
|--------------------|-----|------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x30<br>LDO11_CONT | 7   | R/W  | LDO11_CONF   | Sequencer target state of LDO11_EN                                                                                                                                                                                                                                                                |
|                    | 6:5 | R/W  | VLDO11_GPI   | GPIO select target voltage VLDO11_A on passive to active transition, selects target voltage VLDO11_B on active to passive transition (immediate voltage change)<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled |
|                    | 4   | R/W  | VLDO11_SEL   | LDO11 voltage is selected from (immediate change):<br><b>0: VLDO11_A</b><br>1: VLDO11_B                                                                                                                                                                                                           |
|                    | 3   | R/W  | LDO11_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                                                                                                  |
|                    | 2:1 | R/W  | LDO11_GPI    | GPIO enables LDO11 on passive to active state transition, disables LDO11 on active to passive state transition<br><b>00: Not controlled by GPIO (sequencer control)</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO13 controlled                                                  |
|                    | 0   | R/W  | LDO11_EN     | <b>0: LDO11 disabled</b><br>1: LDO11 enabled                                                                                                                                                                                                                                                      |

Table 108: VIB

| Register Address | Bit | Type | Label    | Description                                                                                                                                                                             |
|------------------|-----|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x31<br>VIB      | 7:6 | R/W  | Reserved |                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VIB_SET  | 000000: OFF-BREAK, NMOS on, PMOS off<br>000001: 47.55 mV<br>000010: 95.1 mV<br>...<br>Average output level set in a range of 0 to 3 V in steps of 3 V/63<br>...<br><b>111111: 3.0 V</b> |

Table 109: DVC\_1

| Register Address | Bit | Type | Label     | Description                                                                 |
|------------------|-----|------|-----------|-----------------------------------------------------------------------------|
| 0x32<br>DVC_1    | 7   | R/W  | VLDO3_SEL | LDO3 voltage is selected from (ramping):<br><b>0: VLDO3_A</b><br>1: VLDO3_B |
|                  | 6   | R/W  | VLDO2_SEL | LDO2 voltage is selected from (ramping):<br><b>0: VLDO2_A</b><br>1: VLDO2_B |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label       | Description                                                                          |
|------------------|-----|------|-------------|--------------------------------------------------------------------------------------|
|                  | 5   | R/W  | VLDO1_SEL   | LDO1 voltage is selected from (ramping):<br><b>0: VLDO1_A</b><br>1: VLDO1_B          |
|                  | 4   | R/W  | VBPERI_SEL  | BUCKPERI voltage is selected from (ramping):<br><b>0: VBPERI_A</b><br>1: VBPERI_B    |
|                  | 3   | R/W  | VBMEM_SEL   | BUCKMEM voltage is selected from (ramping):<br><b>0: VBMEM_A</b><br>1: VBMEM_B       |
|                  | 2   | R/W  | VBPRO_SEL   | BUCKPRO voltage is selected from (ramping):<br><b>0: VBPRO_A</b><br>1: VBPRO_B       |
|                  | 1   | R/W  | VBCORE2_SEL | BUCKCORE2 voltage is selected from (ramping):<br><b>0: VBCORE2_A</b><br>1: VBCORE2_B |
|                  | 0   | R/W  | VBCORE1_SEL | BUCKCORE1 voltage is selected from (ramping):<br><b>0: VBCORE1_A</b><br>1: VBCORE1_B |

Table 110: DVC\_2

| Register Address | Bit | Type | Label     | Description                                                                 |
|------------------|-----|------|-----------|-----------------------------------------------------------------------------|
| 0x33<br>DVC_2    | 7   | R/W  | VLDO4_SEL | LDO4 voltage is selected from (ramping):<br><b>0: VLDO4_A</b><br>1: VLDO4_B |
|                  | 6:1 | R/W  | Reserved  |                                                                             |
|                  | 0   | R/W  | VBIO_SEL  | BUCKIO voltage is selected from (ramping):<br><b>0: VBIO_A</b><br>1: VBIO_B |

## System PMIC for Mobile and Automotive Applications

### A.2.4 GPADC

Table 111: ADC\_MAN

| Register Address | Bit | Type | Label    | Description                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x34<br>ADC_MAN  | 7:6 | R/W  | Reserved |                                                                                                                                                                                                                                                                                                                                         |
|                  | 5   | R/W  | ADC_MODE | <b>0: Measurement sequence interval 10 ms (economy mode)</b><br>1: Measurement sequence interval 1 ms                                                                                                                                                                                                                                   |
|                  | 4   | R/W  | ADC_MAN  | Perform manual conversion. Bit is reset to 0 when conversion is complete.                                                                                                                                                                                                                                                               |
|                  | 3:0 | R/W  | ADC_MUX  | Manual measurement selects:<br>0000: VSYS port<br>0001: ADCIN1<br>0010: ADCIN2<br>0011: ADCIN3<br><b>0100: internal T-Sense</b><br>0101: V <sub>BBAT</sub> -voltage<br>0110: reserved<br>0111: reserved<br>1000: Group 1 regulators voltage<br>1001: Group 2 regulators voltage<br>1010: Group 3 regulators voltage<br>> 1010: reserved |

Table 112: ADC\_CONT

| Register Address | Bit | Type | Label        | Description                                                                                                               |
|------------------|-----|------|--------------|---------------------------------------------------------------------------------------------------------------------------|
| 0x35<br>ADC_CONT | 7   | R/W  | COMP1V2_EN   | <b>0: Disable 1.2 V comparator at ADCIN2</b><br>1: Enable 1.2 V comparator                                                |
|                  | 6   | R/W  | AD3_ISRC_EN  | <b>0: Disable ADCIN3 current source</b><br>1: Enable ADCIN3 current source                                                |
|                  | 5   | R/W  | AD2_ISRC_EN  | <b>0: Disable ADCIN2 current source</b><br>1: Enable ADCIN2 current source                                                |
|                  | 4   | R/W  | AD1_ISRC_EN  | <b>0: Disable ADCIN1 current source</b><br>1: Enable ADCIN1 current source                                                |
|                  | 3   | R/W  | AUTO_AD3_EN  | <b>0: ADCIN3 auto-measurements disabled</b><br>1: ADCIN3 auto-measurements enabled                                        |
|                  | 2   | R/W  | AUTO_AD2_EN  | <b>0: ADCIN2 auto-measurements disabled</b><br>1: ADCIN2 auto-measurements enabled                                        |
|                  | 1   | R/W  | AUTO_AD1_EN  | <b>0: ADCIN1 auto-measurements disabled</b><br>1: ADCIN1 auto-measurements enabled                                        |
|                  | 0   | R/W  | AUTO_VSYS_EN | <b>0: VSYS auto-measurements disabled when charger/vibration motor driver is off</b><br>1: VSYS auto-measurements enabled |

Table 113: VSYS\_MON

| Register Address | Bit | Type | Label    | Description                                                                                           |
|------------------|-----|------|----------|-------------------------------------------------------------------------------------------------------|
| 0x36<br>VSYS_MON | 7:0 | R/W  | VSYS_MON | VSYS_MON threshold setting (8-bit).<br>00000000 corresponds to 2.5 V<br>11111111 corresponds to 5.5 V |

## System PMIC for Mobile and Automotive Applications

### A.2.5 ADC Results

**Table 114: ADC\_RES\_L**

| Register Address  | Bit | Type | Label       | Description                              |
|-------------------|-----|------|-------------|------------------------------------------|
| 0x37<br>ADC_RES_L | 7:6 | R    | ADC_RES_LSB | 10-bit manual conversion result (2 LSBs) |
|                   | 5:0 | R    | Reserved    |                                          |

**Table 115: ADC\_RES\_H**

| Register Address  | Bit | Type | Label       | Description                              |
|-------------------|-----|------|-------------|------------------------------------------|
| 0x38<br>ADC_RES_H | 7:0 | R    | ADC_RES_MSB | 10-bit manual conversion result (8 MSBs) |

**Table 116: VSYS\_RES**

| Register Address | Bit | Type | Label    | Description                                                                                             |
|------------------|-----|------|----------|---------------------------------------------------------------------------------------------------------|
| 0x39<br>VSYS_RES | 7:0 | R    | VSYS_RES | 0x00 – 0xFF: Auto VSYS conversion result (A0)<br>0x00 corresponds to 2.5 V<br>0xFF corresponds to 5.5 V |

**Table 117: ADCIN1\_RES**

| Register Address   | Bit | Type | Label      | Description                                    |
|--------------------|-----|------|------------|------------------------------------------------|
| 0x3A<br>ADCIN1_RES | 7:0 | R    | ADCIN1_RES | 0x00 – 0xFF: Auto ADC ADCIN1 conversion result |

**Table 118: ADCIN2\_RES**

| Register Address   | Bit | Type | Label      | Description                                    |
|--------------------|-----|------|------------|------------------------------------------------|
| 0x3B<br>ADCIN2_RES | 7:0 | R    | ADCIN2_RES | 0x00 – 0xFF: Auto ADC ADCIN2 conversion result |

**Table 119: ADCIN3\_RES**

| Register Address   | Bit | Type | Label      | Description                                    |
|--------------------|-----|------|------------|------------------------------------------------|
| 0x3C<br>ADCIN3_RES | 7:0 | R    | ADCIN3_RES | 0x00 – 0xFF: Auto ADC ADCIN3 conversion result |

**Table 120: MON\_A8\_RES**

| Register Address   | Bit | Type | Label      | Description                                                                                                                      |
|--------------------|-----|------|------------|----------------------------------------------------------------------------------------------------------------------------------|
| 0x3D<br>MON_A8_RES | 7:0 | R    | MON_A8_RES | 0x00 – 0xFF: Regulator output voltage monitor 1 (A8) conversion result<br>0x00 corresponds to 0.0 V<br>0xFF corresponds to 5.0 V |

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Table 121: MON\_A9\_RES

| Register Address   | Bit | Type | Label      | Description                                                                                                                      |
|--------------------|-----|------|------------|----------------------------------------------------------------------------------------------------------------------------------|
| 0x3E<br>MON_A9_RES | 7:0 | R    | MON_A9_RES | 0x00 – 0xFF: Regulator output voltage monitor 2 (A9) conversion result<br>0x00 corresponds to 0.0 V<br>0xFF corresponds to 5.0 V |

Table 122: MON\_A10\_RES

| Register Address    | Bit | Type | Label       | Description                                                                                                                       |
|---------------------|-----|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 0x3F<br>MON_A10_RES | 7:0 | R    | MON_A10_RES | 0x00 – 0xFF: Regulator output voltage monitor 3 (A10) conversion result<br>0x00 corresponds to 0.0 V<br>0xFF corresponds to 5.0 V |

### A.2.6 RTC Calendar and Alarm

Table 123: COUNT\_S

| Register Address | Bit | Type | Label     | Description                                                                                                                                                         |
|------------------|-----|------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x40<br>COUNT_S  | 7   | R    | RTC_READ  | Asserted when below registers have been transferred from RTC logic into host readable registers (for example, after leaving POR)                                    |
|                  | 6   | R    | Reserved  |                                                                                                                                                                     |
|                  | 5:0 | R/W  | COUNT_SEC | 0x00 – 0x3B: RTC seconds read-out. A read of this register latches the current RTC calendar count into the registers COUNT_S to COUNT_Y coherent for approx 0.5 s). |

Table 124: COUNT\_MI

| Register Address | Bit | Type | Label     | Description                       |
|------------------|-----|------|-----------|-----------------------------------|
| 0x41<br>COUNT_MI | 7:6 | R    | Reserved  |                                   |
|                  | 5:0 | R/W  | COUNT_MIN | 0x00 – 0x3B: RTC minutes read-out |

Table 125: COUNT\_H

| Register Address | Bit | Type | Label      | Description                     |
|------------------|-----|------|------------|---------------------------------|
| 0x42<br>COUNT_H  | 7:5 | R    | Reserved   |                                 |
|                  | 4:0 | R/W  | COUNT_HOUR | 0x00 – 0x17: RTC hours read-out |

Table 126: COUNT\_D

| Register Address | Bit | Type | Label     | Description                    |
|------------------|-----|------|-----------|--------------------------------|
| 0x43<br>COUNT_D  | 7:5 | R    | Reserved  |                                |
|                  | 4:0 | R/W  | COUNT_DAY | 0x01 – 0x1F: RTC days read-out |

Table 127: COUNT\_MO

| Register Address | Bit | Type | Label    | Description |
|------------------|-----|------|----------|-------------|
| 0x44             | 7:4 | R    | Reserved |             |

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| Register Address | Bit | Type | Label       | Description                      |
|------------------|-----|------|-------------|----------------------------------|
| COUNT_MO         | 3:0 | R/W  | COUNT_MONTH | 0x01 – 0x0C: RTC months read-out |

Table 128: COUNT\_Y

| Register Address | Bit | Type | Label      | Description                                                                                                                                                                               |
|------------------|-----|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x45<br>COUNT_Y  | 7   | R    | Reserved   |                                                                                                                                                                                           |
|                  | 6   | R/W  | MONITOR    | Read-out 0 indicates that the power was lost. Read-out of 1 indicates that the clock is OK. Set to 1 when setting time to arm RTC monitor function. Cannot be cleared via register write. |
|                  | 5:0 | R/W  | COUNT_YEAR | 0x00 – 0x3F: RTC years read-out (0 corresponds to year 2000). A write to this register latches the registers COUNT_S to COUNT_Y into the current RTC calendar counters.                   |

Table 129: ALARM\_S

| Register Address | Bit | Type | Label      | Description                                                                       |
|------------------|-----|------|------------|-----------------------------------------------------------------------------------|
| 0x46<br>ALARM_S  | 7:6 | R    | ALARM_TYPE | Alarm event caused by:<br>00: No alarm<br>01: Tick<br>10: Timer alarm<br>11: Both |
|                  | 5:0 | R/W  | ALARM_SEC  | 0x00 – 0x3B: Alarm seconds setting                                                |

Table 130: ALARM\_MI

| Register Address | Bit | Type | Label     | Description                        |
|------------------|-----|------|-----------|------------------------------------|
| 0x47<br>ALARM_MI | 7:6 | R    | Reserved  |                                    |
|                  | 5:0 | R/W  | ALARM_MIN | 0x00 – 0x3B: Alarm minutes setting |

Table 131: ALARM\_H

| Register address | Bit | Type | Label      | Description                      |
|------------------|-----|------|------------|----------------------------------|
| 0x48<br>ALARM_H  | 7:5 | R    | Reserved   |                                  |
|                  | 4:0 | R/W  | ALARM_HOUR | 0x00 – 0x17: Alarm hours setting |

Table 132: ALARM\_D

| Register Address | Bit | Type | Label     | Description                     |
|------------------|-----|------|-----------|---------------------------------|
| 0x49<br>ALARM_D  | 7:5 | R    | Reserved  |                                 |
|                  | 4:0 | R/W  | ALARM_DAY | 0x01 – 0x1F: Alarm days setting |

Table 133: ALARM\_MO

| Register Address | Bit | Type | Label    | Description |
|------------------|-----|------|----------|-------------|
| 0x4A             | 7:6 | R    | Reserved |             |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label       | Description                                               |
|------------------|-----|------|-------------|-----------------------------------------------------------|
| ALARM_MO         | 5   | R/W  | TICK_WAKE   | Tick alarm wake-up<br>0: disabled<br>1: enabled           |
|                  | 4   | R/W  | TICK_TYPE   | Tick alarm interval is:<br>0: one second<br>1: one minute |
|                  | 3:0 | R/W  | ALARM_MONTH | 0x01 – 0x0C: Alarm months setting                         |

Table 134: ALARM\_Y

| Register Address | Bit | Type | Label      | Description                                                                                                                       |
|------------------|-----|------|------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 0x4B<br>ALARM_Y  | 7   | R/W  | TICK_ON    | 0: Tick function is disabled<br>1: Periodic tick alarm enabled                                                                    |
|                  | 6   | R/W  | ALARM_ON   | 0: Alarm function is disabled<br>1: Alarm enabled                                                                                 |
|                  | 5:0 | R/W  | ALARM_YEAR | 0x00 – 0x3F: Alarm years setting (0 corresponds to year 2000). A write to this register latches the registers ALARM_MI to ALARM_Y |

Table 135: SECOND\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                                    |
|------------------|-----|------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x4C<br>SECOND_A | 7:0 | R    | SECONDS_A | RTC seconds counter A (LSBs). A read of this register latches the current 32-bit counter into the registers SECOND_A to SECOND_D (coherent for approx. 0.5 s). |

Table 136: SECOND\_B

| Register Address | Bit | Type | Label     | Description           |
|------------------|-----|------|-----------|-----------------------|
| 0x4D<br>SECOND_B | 7:0 | R    | SECONDS_B | RTC seconds counter B |

Table 137: SECOND\_C

| Register Address | Bit | Type | Label     | Description           |
|------------------|-----|------|-----------|-----------------------|
| 0x4E<br>SECOND_C | 7:0 | R    | SECONDS_C | RTC seconds counter C |

Table 138: SECOND\_D

| Register Address | Bit | Type | Label     | Description                  |
|------------------|-----|------|-----------|------------------------------|
| 0x4F<br>SECOND_D | 7:0 | R    | SECONDS_D | RTC seconds counter D (MSBs) |

Table 139: Co-PMIC

| Register Address | Bit | Type | Label    | Description          |
|------------------|-----|------|----------|----------------------|
| 0x50<br>CoPMIC_S | 7:0 | R    | Reserved | Reserved for Co-PMIC |
| 0x67<br>CoPMIC_E | 7:0 | R    | Reserved | Reserved for Co-PMIC |

## System PMIC for Mobile and Automotive Applications

Table 140: CHG\_Co

| Register Address | Bit | Type | Label    | Description                    |
|------------------|-----|------|----------|--------------------------------|
| 0x68<br>CHG_Co_S | 7:0 | R    | Reserved | Reserved for companion charger |
| 0x7F<br>CHG_Co_E | 7:0 | R    | Reserved | Reserved for companion charger |

### A.3 Register Page 1

Table 141: PAGE\_CON

| Register Address | Bit | Type | Label      | Description                                 |
|------------------|-----|------|------------|---------------------------------------------|
| 0x80<br>PAGE_CON | 7   | RW   | REVERT     | See register 0x00, <a href="#">Table 59</a> |
|                  | 6   | RW   | WRITE_MODE |                                             |
|                  | 5:3 | RW   | Reserved   |                                             |
|                  | 2:0 | RW   | REG_PAGE   |                                             |

#### A.3.1 Power Sequencer

Table 142: SEQ

| Register Address | Bit | Type | Label         | Description                                                                  |
|------------------|-----|------|---------------|------------------------------------------------------------------------------|
| 0x81<br>SEQ      | 7:4 | R/W  | NXT_SEQ_START | Start time slot for first sequencing after being modified via register write |
|                  | 3:0 | R    | SEQ_POINTER   | Actual pointer position (time slot) of power sequencer                       |

Table 143: SEQ\_TIMER

| Register Address  | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                          |
|-------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x82<br>SEQ_TIMER | 7:4 | R/W  | SEQ_DUMMY | 0000: 32 $\mu$ s<br>0001: 64 $\mu$ s<br>0010: 96 $\mu$ s<br>0011: 128 $\mu$ s<br>0100: 160 $\mu$ s<br>0101: 192 $\mu$ s<br>0110: 224 $\mu$ s<br>0111: 256 $\mu$ s<br>1000: 288 $\mu$ s<br>1001: 384 $\mu$ s<br>1010: 448 $\mu$ s<br>1011: 512 $\mu$ s<br>1100: 1.024 ms<br><b>1101: 2.048 ms</b><br>1110: 4.096 ms<br>1111: 8.192 ms |

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| Register Address | Bit | Type | Label    | Description                                                                                                                                                                                                                                                                                                                          |
|------------------|-----|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 3:0 | R/W  | SEQ_TIME | 0000: 32 $\mu$ s<br>0001: 64 $\mu$ s<br>0010: 96 $\mu$ s<br>0011: 128 $\mu$ s<br>0100: 160 $\mu$ s<br>0101: 192 $\mu$ s<br>0110: 224 $\mu$ s<br>0111: 256 $\mu$ s<br>1000: 288 $\mu$ s<br>1001: 384 $\mu$ s<br>1010: 448 $\mu$ s<br>1011: 512 $\mu$ s<br><b>1100: 1.024 ms</b><br>1101: 2.048 ms<br>1110: 4.096 ms<br>1111: 8.192 ms |

Table 144: ID\_2\_1

| Register Address | Bit | Type | Label     | Description                                |
|------------------|-----|------|-----------|--------------------------------------------|
| 0x83<br>ID_2_1   | 7:4 | R/W  | LDO2_STEP | Power sequencer time slot for LDO2 control |
|                  | 3:0 | R/W  | LDO1_STEP | Power sequencer time slot for LDO1 control |

Table 145: ID\_4\_3

| Register Address | Bit | Type | Label     | Description                                |
|------------------|-----|------|-----------|--------------------------------------------|
| 0x84<br>ID_4_3   | 7:4 | R/W  | LDO4_STEP | Power sequencer time slot for LDO4 control |
|                  | 3:0 | R/W  | LDO3_STEP | Power sequencer time slot for LDO3 control |

Table 146: ID\_6\_5

| Register Address | Bit | Type | Label     | Description                                |
|------------------|-----|------|-----------|--------------------------------------------|
| 0x85<br>ID_6_5   | 7:4 | R/W  | LDO6_STEP | Power sequencer time slot for LDO6 control |
|                  | 3:0 | R/W  | LDO5_STEP | Power sequencer time slot for LDO5 control |

Table 147: ID\_8\_7

| Register Address | Bit | Type | Label     | Description                                |
|------------------|-----|------|-----------|--------------------------------------------|
| 0x86<br>ID_8_7   | 7:4 | R/W  | LDO8_STEP | Power sequencer time slot for LDO8 control |
|                  | 3:0 | R/W  | LDO7_STEP | Power sequencer time slot for LDO7 control |

Table 148: ID\_10\_9

| Register Address | Bit | Type | Label      | Description                                 |
|------------------|-----|------|------------|---------------------------------------------|
| 0x87<br>ID_10_9  | 7:4 | R/W  | LDO10_STEP | Power sequencer time slot for LDO10 control |
|                  | 3:0 | R/W  | LDO9_STEP  | Power sequencer time slot for LDO9 control  |

Table 149: ID\_12\_11

| Register Address | Bit | Type | Label       | Description                                                                                 |
|------------------|-----|------|-------------|---------------------------------------------------------------------------------------------|
| 0x88<br>ID_12_11 | 7:4 | R/W  | PD_DIS_STEP | Power sequencer time slot for control of blocks to be disabled/paused during POWERDOWN mode |

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| Register Address | Bit | Type | Label             | Description                                 |
|------------------|-----|------|-------------------|---------------------------------------------|
|                  | 3:0 | R/W  | <b>LDO11_STEP</b> | Power sequencer time slot for LDO11 control |

Table 150: ID\_14\_13

| Register Address | Bit | Type | Label                 | Description                                                                               |
|------------------|-----|------|-----------------------|-------------------------------------------------------------------------------------------|
| 0x89<br>ID_14_13 | 7:4 | R/W  | <b>BUCKCORE2_STEP</b> | Power sequencer time slot for control of BUCKCORE2 (disabled in BUCKCORE dual phase mode) |
|                  | 3:0 | R/W  | <b>BUCKCORE1_STEP</b> | Power sequencer time slot for control of BUCKCORE1                                        |

Table 151: ID\_16\_15

| Register Address | Bit | Type | Label               | Description                                      |
|------------------|-----|------|---------------------|--------------------------------------------------|
| 0x8A<br>ID_16_15 | 7:4 | R/W  | <b>BUCK_IO_STEP</b> | Power sequencer time slot for control of BUCKPRO |
|                  | 3:0 | R/W  | <b>BUCKPRO_STEP</b> | Power sequencer time slot for control of BUCKPRO |

Table 152: ID\_18\_17

| Register Address | Bit | Type | Label                | Description                                       |
|------------------|-----|------|----------------------|---------------------------------------------------|
| 0x8B<br>ID_18_17 | 7:4 | R/W  | <b>BUCKPERI_STEP</b> | Power sequencer time slot for control of BUCKPERI |
|                  | 3:0 | R/W  | <b>BUCKMEM_STEP</b>  | Power sequencer time slot for control of BUCKMEM  |

Table 153: ID\_20\_19

| Register Address | Bit | Type | Label               | Description                                               |
|------------------|-----|------|---------------------|-----------------------------------------------------------|
| 0x8C<br>ID_20_19 | 7:4 | R/W  | <b>PERI_SW_STEP</b> | Power sequencer time slot for control of PERI rail switch |
|                  | 3:0 | R/W  | <b>CORE_SW_STEP</b> | Power sequencer time slot for control of CORE rail switch |

Table 154: ID\_22\_21

| Register Address | Bit | Type | Label                | Description                                                |
|------------------|-----|------|----------------------|------------------------------------------------------------|
| 0x8D<br>ID_22_21 | 7:4 | R/W  | <b>GP_FALL1_STEP</b> | Power sequencer time slot for falling edge control of GPO2 |
|                  | 3:0 | R/W  | <b>GP_RISE1_STEP</b> | Power sequencer time slot for rising edge control of GPO2  |

Table 155: ID\_24\_23

| Register Address | Bit | Type | Label                | Description                                                |
|------------------|-----|------|----------------------|------------------------------------------------------------|
| 0x8E<br>ID_24_23 | 7:4 | R/W  | <b>GP_FALL2_STEP</b> | Power sequencer time slot for falling edge control of GPO7 |
|                  | 3:0 | R/W  | <b>GP_RISE2_STEP</b> | Power sequencer time slot for rising edge control of GPO7  |

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Table 156: ID\_26\_25

| Register Address | Bit | Type | Label         | Description                                                |
|------------------|-----|------|---------------|------------------------------------------------------------|
| 0x8F<br>ID_26_25 | 7:4 | R/W  | GP_FALL3_STEP | Power sequencer time slot for falling edge control of GPO8 |
|                  | 3:0 | R/W  | GP_RISE3_STEP | Power sequencer time slot for rising edge control of GPO8  |

Table 157: ID\_28\_27

| Register Address | Bit | Type | Label         | Description                                                |
|------------------|-----|------|---------------|------------------------------------------------------------|
| 0x90<br>ID_28_27 | 7:4 | R/W  | GP_FALL4_STEP | Power sequencer time slot for falling edge control of GPO9 |
|                  | 3:0 | R/W  | GP_RISE4_STEP | Power sequencer time slot for rising edge control of GPO9  |

Table 158: ID\_30\_29

| Register Address | Bit | Type | Label         | Description                                                 |
|------------------|-----|------|---------------|-------------------------------------------------------------|
| 0x91<br>ID_30_29 | 7:4 | R/W  | GP_FALL5_STEP | Power sequencer time slot for falling edge control of GPO11 |
|                  | 3:0 | R/W  | GP_RISE5_STEP | Power sequencer time slot for rising edge control of GPO11  |

Table 159: ID\_32\_31

| Register Address | Bit | Type | Label      | Description                                                                                             |
|------------------|-----|------|------------|---------------------------------------------------------------------------------------------------------|
| 0x92<br>ID_32_31 | 7:4 | R/W  | EN32K_STEP | Power sequencer time slot for enable/disable of 32K output signals                                      |
|                  | 3:0 | R/W  | WAIT_STEP  | Power sequencer time slot that gates the progress with state of GPI10 (or used a dedicated delay timer) |

Table 160: Reserved

| Register Address | Bit | Type | Label    | Description |
|------------------|-----|------|----------|-------------|
| 0x93, 0x94       | 7:0 | R/W  | Reserved |             |

Table 161: SEQ\_A

| Register Address | Bit | Type | Label      | Description                                 |
|------------------|-----|------|------------|---------------------------------------------|
| 0x95<br>SEQ_A    | 7:4 | R/W  | POWER_END  | OTP pointer to last supply of domain POWER  |
|                  | 3:0 | R/W  | SYSTEM_END | OTP pointer to last supply of domain SYSTEM |

Table 162: SEQ\_B

| Register Address | Bit | Type | Label     | Description                                 |
|------------------|-----|------|-----------|---------------------------------------------|
| 0x96<br>SEQ_B    | 7:4 | R/W  | PART_DOWN | OTP pointer for partial POWERDOWN mode      |
|                  | 3:0 | R/W  | MAX_COUNT | OTP pointer to last supply of domain POWER1 |

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Table 163: WAIT

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                  |
|------------------|-----|------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x97<br>WAIT     | 7:6 | R/W  | WAIT_DIR  | <b>00: No wait during power sequencing</b><br>01: Wait during power-up sequence<br>10:: Wait during power-down sequence<br>11: Wait during power-up and power-down sequence                                                                                                  |
|                  | 5   | R/W  | TIME_OUT  | <b>0: No time limit</b><br>1: 500 ms time out for waiting GPIO10 to get active                                                                                                                                                                                               |
|                  | 4   | R/W  | WAIT_MODE | 0: Wait for GPIO10 to be active<br><b>1: Timer mode (start timer and wait for expire)</b>                                                                                                                                                                                    |
|                  | 3:0 | R/W  | WAIT_TIME | 0000: 0.0 $\mu$ s<br>0001: 512 $\mu$ s<br>0010: 1.0 ms<br>0011: 2.0 ms<br>0100: 4.1 ms<br>0101: 8.2 ms<br>0110: 16.4 ms<br>0111: 32.8 ms<br>1000: 65.5 ms<br>1001: 128 ms<br>1010: 256 ms<br><b>1011: 512 ms</b><br>1100: 1.0 s<br>1101: 2.1 s<br>1110: 4.2 s<br>1111: 8.4 s |

Table 164: EN\_32K

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x98<br>EN_32K   | 7   | R/W  | EN_32KOUT | 0: 32K clock buffer off (OUT_32K)<br><b>1: 32K clock buffer enabled (OUT_32K)</b> , when powering up with a power sequence including EN32K_STEP the buffer is enabled when reaching EN32K_STEP, in case the power sequence includes PD_DIS_STEP with OUT_32K_PAUSE asserted the buffer enable is delayed until reaching PD_DIS_STEP on the way up<br><br>Note: with OUT_CLOCK being asserted the buffer enable is delayed until 32 kHz oscillator signal is stable |
|                  | 6   | R/W  | RTC_CLOCK | 0: No gating of RTC calendar clock<br><b>1: Clock to RTC counter is gated until 32 kHz oscillator stabilization timer has expired</b>                                                                                                                                                                                                                                                                                                                              |
|                  | 5   | R/W  | OUT_CLOCK | 0: No gating of OUT_32K and clock signals at GP_FB3<br><b>1: Clock to buffers is gated until 32 kHzoscillation stabilization timer has expired (indicating stable 32 kHz oscillator signal)</b>                                                                                                                                                                                                                                                                    |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label                     | Description                                                                                                                                                                                                                              |
|------------------|-----|------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 4   | R/W  | <b>DELAY_MODE</b>         | <b>0: Start stabilization timer when duty cycle of oscillator signal is in between 30% and 70%</b><br>1: Start stabilization timer when CRYSTAL is asserted, RTC_EN changed or when leaving DELIVERY/NO-POWER mode with CRYSTAL asserted |
|                  | 3   | R/W  | <b>CRYSTAL</b>            | 0: No 32 kHz crystal connected (bypass via XOUT)<br><b>1: 32 kHz crystal connected</b>                                                                                                                                                   |
|                  | 2:0 | R/W  | <b>STABILIZATION_TIME</b> | Time to allow crystal oscillator to stabilize:<br>000: 0.0 s (delay off)<br><b>001: 0.52 s</b><br>010: 1.0 s<br>011: 1.5 s<br>100: 2.1 s<br>101: 2.6 s<br>110: 3.1 s<br>111: 3.6 s                                                       |

**Table 165: RESET**

| Register Address | Bit | Type | Label              | Description                                                                                                                                                                                                                                                                                                               |
|------------------|-----|------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x99<br>RESET    | 7:6 | R/W  | <b>RESET_EVENT</b> | RESET timer started by<br>00: EXT_WAKEUP<br><b>01: SYS_UP</b><br>10: PWR_UP<br>11: leaving PMIC RESET state (do not use in combination with nRES_MODE = 1)                                                                                                                                                                |
|                  | 5:0 | R/W  | <b>RESET_TIMER</b> | 000000: 0.000 ms<br>000001: 1.024 ms<br>000010: 2.048 ms<br>000011: 3.072 ms<br>000100: 4.096 ms<br><b>000101: 5.120 ms</b><br>....<br>011110: 30.720 ms<br>011111: 31.744 ms<br>100000: 32.768 ms<br>100001: 65.536 ms<br>100010: 98.304 ms<br>.....<br>111101: 983.040 ms<br>111110: 1015.808 ms<br>111111: 1048.576 ms |

## System PMIC for Mobile and Automotive Applications

### A.3.2 Regulator Settings

Table 166: BUCK\_ILIM\_A

| Register Address    | Bit | Type | Label            | Description                                                                                                                                                                                                                                                                                                         |
|---------------------|-----|------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x9A<br>BUCK_ILIM_A | 7:4 | R/W  | <b>BMEM_ILIM</b> | BUCKMEM current limit (all limits x2 in MERGE mode)<br>0000:1500 mA<br>0001:1600 mA<br>0010:1700 mA<br>0011:1800 mA<br>0100:1900 mA<br>0101:2000 mA<br>0110:2100 mA<br>0111:2200 mA<br>1000:2300 mA<br>1001:2400 mA<br>1010:2500 mA<br>1011:2600 mA<br>1100:2700 mA<br>1101:2800 mA<br>1110:2900 mA<br>1111:3000 mA |
|                     | 3:0 | R/W  | <b>BIO_ILIM</b>  | BUCKIO current limit<br>0000:1500 mA<br>0001:1600 mA<br>0010:1700 mA<br>0011:1800 mA<br>0100:1900 mA<br>0101:2000 mA<br>0110:2100 mA<br>0111:2200 mA<br>1000:2300 mA<br>1001:2400 mA<br>1010:2500 mA<br>1011:2600 mA<br>1100:2700 mA<br>1101:2800 mA<br>1110:2900 mA<br>1111:3000 mA                                |

## System PMIC for Mobile and Automotive Applications

Table 167: BUCK\_ILIM\_B

| Register Address    | Bit | Type | Label      | Description                                                                                                                                                                                                                                                                                                           |
|---------------------|-----|------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x9B<br>BUCK_ILIM_B | 7:4 | R/W  | BPERI_ILIM | BUCKPERI current limit<br>0000:1500 mA<br>0001:1600 mA<br>0010:1700 mA<br>0011:1800 mA<br>0100:1900 mA<br>0101:2000 mA<br>0110:2100 mA<br>0111:2200 mA<br>1000:2300 mA<br>1001:2400 mA<br>1010:2500 mA<br>1011:2600 mA<br>1100:2700 mA<br>1101:2800 mA<br>1110:2900 mA<br>1111:3000 mA                                |
|                     | 3:0 | R/W  | BPRO_ILIM  | BUCKPRO current limit (all limits x2 in full-current mode)<br>0000:500 mA<br>0001:600 mA<br>0010:700 mA<br>0011:800 mA<br>0100:900 mA<br>0101:1000 mA<br>0110:1100 mA<br>0111:1200 mA<br>1000:1300 mA<br>1001:1400 mA<br>1010:1500 mA<br>1011:1600 mA<br>1100:1700 mA<br>1101:1800 mA<br>1110:1900 mA<br>1111:2000 mA |

Table 168: BUCK\_ILIM\_C

| Register Address    | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                                                             |
|---------------------|-----|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x9C<br>BUCK_ILIM_C | 7:4 | R/W  | BCORE2_ILIM | BUCKCORE2 current limit (all limits x2 in full-current mode)<br>0000:500 mA<br>0001:600 mA<br>0010:700 mA<br>0011:800 mA<br>0100:900 mA<br>0101:1000 mA<br>0110:1100 mA<br>0111:1200 mA<br>1000:1300 mA<br>1001:1400 mA<br>1010:1500 mA<br>1011:1600 mA<br>1100:1700 mA<br>1101:1800 mA<br>1110:1900 mA<br>1111:2000 mA |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label              | Description                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 3:0 | R/W  | <b>BCORE1_ILIM</b> | BUCKCORE1 current limit (all limits x2 in full-current mode)<br>0000:500 mA<br>0001:600 mA<br>0010:700 mA<br>0011:800 mA<br>0100:900 mA<br>0101:1000 mA<br>0110:1100 mA<br>0111:1200 mA<br>1000:1300 mA<br>1001:1400 mA<br>1010:1500 mA<br>1011:1600 mA<br>1100:1700 mA<br>1101:1800 mA<br>1110:1900 mA<br>1111:2000 mA |

**Table 169: BCORE2\_CONF**

| Register Address    | Bit | Type | Label                | Description                                                                                                                                                                                                                |
|---------------------|-----|------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x9D<br>BCORE2_CONF | 7:6 | R/W  | <b>BCORE2_MODE</b>   | 00: Sleep/Synchronous mode controlled via voltage A and B registers<br>01: BUCKCORE2 always operates in Sleep mode<br>10: BUCKCORE2 always operates in Synchronous mode<br><b>11: BUCKCORE2 operates in Automatic mode</b> |
|                     | 5   | R/W  | <b>BCORE2_PD_DIS</b> | <b>0: Enable pull-down resistor (automatically disabled in dual-phase mode)</b><br>1: No pull-down resistor in disabled mode                                                                                               |
|                     | 4:3 |      | <b>Reserved</b>      |                                                                                                                                                                                                                            |
|                     | 2:0 | R/W  | <b>BCORE2_FB</b>     | BUCKCORE2 feedback signal is created out of:<br>xx1: VBUCKCORE2<br>x1x: CORE_SWS<br>1xx: PERI_SWS<br>Each switch connected to the output of the buck may be selected; setting 0b000 is invalid                             |

**Table 170: BCORE1\_CONF**

| Register Address    | Bit | Type | Label                | Description                                                                                                                                                                                                                |
|---------------------|-----|------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x9E<br>BCORE1_CONF | 7:6 | R/W  | <b>BCORE1_MODE</b>   | 00: Sleep/Synchronous mode controlled via voltage A and B registers<br>01: BUCKCORE1 always operates in Sleep mode<br>10: BUCKCORE1 always operates in Synchronous mode<br><b>11: BUCKCORE1 operates in Automatic mode</b> |
|                     | 5   | R/W  | <b>BCORE1_PD_DIS</b> | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                           |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 4:3 |      | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|                  | 2:0 | R/W  | BCORE1_FB | <p>BUCKCORE feedback signal is created out of:</p> <p>000: BCORE_MERGE= 0: VBUCKCORE1<br/>           BCORE_MERGE= 1: Differential remote sensing via VBUCKCORE1 – VBUCKCORE2 and output capacitor voltage sense via port CORE_SWS or GP_FB_2</p> <p>xx1: VBUCKCORE1<br/>           x1x: CORE_SWS<br/>           1xx: PERI_SWS</p> <p>Each switch connected to the output of the buck may be selected; setting 0b000 disables sense voltage mixer for BUCKCORE</p> |

**Table 171: BPRO\_CONF**

| Register Address  | Bit | Type | Label        | Description                                                                                                                                                                                                                                      |
|-------------------|-----|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x9F<br>BPRO_CONF | 7:6 | R/W  | BPRO_MODE    | <p>00: Sleep/Synchronous mode controlled via voltage A and B registers<br/>           10: BUCKPRO always operates in Sleep mode<br/>           10: BUCKPRO always operates in Synchronous<br/> <b>11: BUCKPRO operates in Automatic mode</b></p> |
|                   | 5   | R/W  | BPRO_PD_DIS  | <p><b>0: Enable pull-down resistor</b><br/>           1: No pull-down resistor in disabled mode</p>                                                                                                                                              |
|                   | 4   | R/W  | BPRO_VTT_EN  | <p><b>0: Buck voltage mode</b><br/>           1: VTT mode, buck target voltage tracks 50% of VDDQ sense port (requires BPRO_VTTR_EN to be asserted as well)</p>                                                                                  |
|                   | 3   | R/W  | BPRO_VTTR_EN | <p><b>0: VTTR port is assigned to E_CMP1V2, port VDDQ provides status of E_GPI2</b><br/>           1: VTTR port provides 50% of VDDQ voltage</p>                                                                                                 |
|                   | 2:0 | R/W  | BPRO_FB      | <p>BUCKPRO feedback signal is created out of:</p> <p>xx1: VBUCKPRO<br/>           x1x: CORE_SWS<br/>           1xx: PERI_SWS</p> <p>Each switch connected to the output of the buck may be selected; setting 0b000 is invalid</p>                |

## System PMIC for Mobile and Automotive Applications

Table 172: BIO\_CONF

| Register Address | Bit | Type | Label      | Description                                                                                                                                                                                                  |
|------------------|-----|------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xA0<br>BIO_CONF | 7:6 | R/W  | BIO_MODE   | 00: Sleep/Synchronous mode controlled via voltage A and B registers<br>10: BUCKIO always operates in Sleep mode<br>10: BUCKIO always operates in Synchronous<br><b>11: BUCKIO operates in Automatic mode</b> |
|                  | 5   | R/W  | BIO_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                             |
|                  | 4:3 |      | Reserved   |                                                                                                                                                                                                              |
|                  | 2:0 | R/W  | BIO_FB     | BUCKIO feedback signal is created out of:<br>xx1: VBUCKBIO<br>x1x: CORE_SWS<br>1xx: PERI_SWS<br>Each switch connected to the output of the buck may be selected; setting 0b000 is invalid                    |

Table 173: BMEM\_CONF

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                          |
|-------------------|-----|------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xA1<br>BMEM_CONF | 7:6 | R/W  | BMEM_MODE   | 00: Sleep/Synchronous mode controlled via voltage A and B registers<br>01: BUCKMEM always operates in Sleep mode<br>10: BUCKMEM always operates in Synchronous mode<br><b>11: BUCKMEM operates in Automatic mode</b> |
|                   | 5   | R/W  | BMEM_PD_DIS | <b>0: Enable pull-down resistor</b><br>1: No pull-down resistor in disabled mode                                                                                                                                     |
|                   | 4:3 |      | Reserved    |                                                                                                                                                                                                                      |
|                   | 2:0 | R/W  | BMEM_FB     | BUCKMEM feedback signal is created out of:<br>xx1: VBUCKMEM<br>x1x: CORE_SWS<br>1xx: PERI_SWS<br>Each switch connected to the output of the buck may be selected; setting 0b000 is invalid                           |

Table 174: BPERI\_CONF

| Register Address   | Bit | Type | Label      | Description                                                                                                                                                                                                             |
|--------------------|-----|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xA2<br>BPERI_CONF | 7:6 | R/W  | BPERI_MODE | 00: Sleep/Synchronous mode controlled via voltage A and B registers<br>01: BUCKPERI always operates in Sleep mode<br>10: BUCKPERI always operates in Synchronous mode<br><b>11: BUCKPERI operates in Automatic mode</b> |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label        | Description                                                                                                                                                                                   |
|------------------|-----|------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 5   | R/W  | BPERI_PD_DIS | 0: Enable pull-down resistor<br>1: No pull-down resistor in disabled mode                                                                                                                     |
|                  | 4:3 |      | Reserved     |                                                                                                                                                                                               |
|                  | 2:0 | R/W  | BPERI_FB     | BUCKPERI feedback signal is created out of:<br>xx1: VBUCKPERI<br>x1x: CORE_SWS<br>1xx: PERI_SWS<br>Each switch connected to the output of the buck may be selected; setting 0b0000 is invalid |

Table 175: VBCORE2\_A

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------------|-----|------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xA3<br>VBCORE2_A | 7   | R/W  | BCORE2_SL_A | 0: Configures BUCKCORE2 to Synchronous mode, when selecting A voltage settings<br>1: Configures BUCKCORE2 to Sleep mode, when selecting A voltage settings                                                                                                                                                                                                                                                                                                                                                          |
|                   | 6:0 | R/W  | VBCORE2_A   | 0000000: 0.30 V<br>0000001: 0.31 V<br>0000010: 0.32 V<br>0000011: 0.33 V<br>0000100: 0.34 V<br>0000101: 0.35 V<br>...<br>0100101: 0.67 V<br>0100110: 0.68 V<br>0100111: 0.69 V<br>0101000: 0.70 V<br>0101001: 0.71 V<br>...<br><b>1010000: 1.10 V</b><br>...<br>1110011: 1.45 V<br>1110100: 1.46 V<br>1110101: 1.47 V<br>1110110: 1.48 V<br>1110111: 1.49 V<br>1111000: 1.50 V<br>1111001: 1.51 V<br>1111010: 1.52 V<br>1111011: 1.53 V<br>1111100: 1.54 V<br>1111101: 1.55 V<br>1111110: 1.56 V<br>1111111: 1.57 V |

Table 176: VBCORE1\_A

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                |
|-------------------|-----|------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xA4<br>VBCORE1_A | 7   | R/W  | BCORE1_SL_A | 0: Configures BUCKCORE1 to Synchronous mode, when selecting A voltage settings<br>1: Configures BUCKCORE1 to Sleep mode, when selecting A voltage settings |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                       |
|------------------|-----|------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 6:0 | R/W  | VBCORE1_A | 0000000: 0.30 V<br>0000001: 0.31 V<br>0000010: 0.32 V<br>0000011: 0.33 V<br>0000100: 0.34 V<br>0000101: 0.35 V<br>...<br>0100101: 0.67 V<br>0100110: 0.68 V<br>0100111: 0.69 V                                                                                                                                                    |
|                  |     |      |           | 0101000: 0.70 V<br>0101001: 0.71 V<br>...<br><b>1010000: 1.10 V</b><br>...<br>1110011: 1.45 V<br>1110100: 1.46 V<br>1110101: 1.47 V<br>1110110: 1.48 V<br>1110111: 1.49 V<br>1111000: 1.50 V<br>1111001: 1.51 V<br>1111010: 1.52 V<br>1111011: 1.53 V<br>1111100: 1.54 V<br>1111101: 1.55 V<br>1111110: 1.56 V<br>1111111: 1.57 V |

PWM mode voltage range

Table 177: VBPRO\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                                   |
|------------------|-----|------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xA5<br>VBPRO_A  | 7   | R/W  | BPRO_SL_A | <b>0: Configures BUCKPRO to Synchronous mode, when selecting A voltage settings</b><br>1: Configures BUCKPRO to Sleep mode, when selecting A voltage settings |
|                  | 6:0 | R/W  | VBPRO_A   | 0000000: 0.53 V<br>0000001: 0.54 V<br>0000010: 0.55 V<br>0000011: 0.56 V<br>0000100: 0.57 V<br>0000101: 0.58 V<br>...<br>0010000: 0.69 V                      |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label | Description                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------------|-----|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  |     |      |       | 0010001: 0.70 V<br>0010010: 0.71 V<br>0010011: 0.72 V<br>0010100: 0.73 V<br>0010101: 0.74 V<br>0010110: 0.75 V<br>...<br><b>1000011: 1.20 V</b><br>...<br>1110011: 1.68 V<br>1110100: 1.69 V<br>1110101: 1.70 V<br>1110110: 1.71 V<br>1110111: 1.72 V<br>1111000: 1.73 V<br>1111001: 1.74 V<br>1111010: 1.75 V<br>1111011: 1.76 V<br>1111100: 1.77 V<br>1111101: 1.78 V<br>1111110: 1.79 V<br>1111111: 1.80 V |
|                  |     |      |       | PWM mode voltage range                                                                                                                                                                                                                                                                                                                                                                                        |

Table 178: VBMEM\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                         |
|------------------|-----|------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xA6<br>VBMEM_A  | 7   | R/W  | BMEM_SL_A | <b>0: Configures BUCKMEM to Synchronous mode, when selecting A voltage settings</b><br>1: Configures BUCKMEM to Sleep mode, when selecting A voltage settings                                       |
|                  | 6:0 | R/W  | VBMEM_A   | 0000000: 0.80 V<br>0000001: 0.82 V<br>0000010: 0.84 V<br>...<br><b>0010100: 1.20 V</b><br>...<br>0111100: 2.00 V<br>0111101: 2.02 V<br>0111110: 2.04 V<br>0111111: 2.06 V<br>...<br>1111111: 3.34 V |

Table 179: VBIO\_A

| Register Address | Bit | Type | Label | Description                                                                                                                                                 |
|------------------|-----|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xA7<br>VBIO_A   | 7   | R/W  |       | <b>0: Configures BUCKIO to Synchronous mode, when selecting A voltage settings</b><br>1: Configures BUCKIO to Sleep mode, when selecting A voltage settings |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label  | Description                                                                                                                                                                                         |
|------------------|-----|------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 6:0 | R/W  | VBIO_A | 0000000: 0.80 V<br>0000001: 0.82 V<br>0000010: 0.84 V<br>...<br><b>0010100: 1.20 V</b><br>...<br>0111100: 2.00 V<br>0111101: 2.02 V<br>0111110: 2.04 V<br>0111111: 2.06 V<br>...<br>1111111: 3.34 V |

Table 180: VBPERI\_A

| Register Address | Bit | Type | Label      | Description                                                                                                                                                                                         |
|------------------|-----|------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xA8<br>VBPERI_A | 7   | R/W  | BPERI_SL_A | <b>0: Configures BUCKPERI to Synchronous mode, when selecting A voltage settings</b><br>1: Configures BUCKPERI to Sleep mode, when selecting A voltage settings                                     |
|                  | 6:0 | R/W  | VBPERI_A   | 0000000: 0.80 V<br>0000001: 0.82 V<br>0000010: 0.84 V<br>...<br><b>0110010: 1.80 V</b><br>...<br>0111100: 2.00 V<br>0111101: 2.02 V<br>0111110: 2.04 V<br>0111111: 2.06 V<br>...<br>1111111: 3.34 V |

Table 181: VLDO1\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                      |
|------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xA9<br>VLDO1_A  | 7   | R/W  | LDO1_SL_A | <b>0: Configures LDO to normal mode, when selecting A voltage settings</b><br>1: Configures LDO to Sleep mode, when selecting A voltage settings |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                  |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------------|-----|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 5:0 | R/W  | VLDO1_A | 000000: 0.60 V<br>000001: 0.62 V<br>000010: 0.64 V<br>000011: 0.66 V<br>000100: 0.68 V<br>000101: 0.70 V<br>000110: 0.72 V<br>000111: 0.74 V<br>001000: 0.76 V<br>001001: 0.78 V<br>001010: 0.80 V<br>001011: 0.82 V<br>001100: 0.82 V<br>001101: 0.86 V<br>001110: 0.88 V<br>001111: 0.90 V<br>010000: 0.92 V<br>010001: 0.94 V<br>010010: 0.96 V<br>010011: 0.98 V<br>010100: 1.00 V<br>010101: 1.02 V<br>010110: 1.04 V<br>010111: 1.06 V<br>011000: 1.08 V<br>011001: 1.10 V<br>011010: 1.12 V<br>011011: 1.14 V<br>011100: 1.16 V<br>011101: 1.18 V<br><b>011110: 1.20 V</b><br>011111: 1.22 V<br>100000: 1.24 V<br>100001: 1.26 V<br>...<br>111000: 1.72 V<br>111001: 1.74 V<br>111010: 1.76 V<br>111011: 1.78 V<br>111100: 1.80 V<br>111101: 1.82 V<br>111110: 1.84 V<br>111111: 1.86 V |

Table 182: VLDO2\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                      |
|------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xAA<br>VLDO2_A  | 7   | R/W  | LDO2_SL_A | <b>0: Configures LDO to normal mode, when selecting A voltage settings</b><br>1: Configures LDO to Sleep mode, when selecting A voltage settings |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                  |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------------|-----|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 5:0 | R/W  | VLDO2_A | 000000: 0.60 V<br>000001: 0.62 V<br>000010: 0.64 V<br>000011: 0.66 V<br>000100: 0.68 V<br>000101: 0.70 V<br>000110: 0.72 V<br>000111: 0.74 V<br>001000: 0.76 V<br>001001: 0.78 V<br>001010: 0.80 V<br>001011: 0.82 V<br>001100: 0.82 V<br>001101: 0.86 V<br>001110: 0.88 V<br>001111: 0.90 V<br>010000: 0.92 V<br>010001: 0.94 V<br>010010: 0.96 V<br>010011: 0.98 V<br>010100: 1.00 V<br>010101: 1.02 V<br>010110: 1.04 V<br>010111: 1.06 V<br>011000: 1.08 V<br>011001: 1.10 V<br>011010: 1.12 V<br>011011: 1.14 V<br>011100: 1.16 V<br>011101: 1.18 V<br><b>011110: 1.20 V</b><br>011111: 1.22 V<br>100000: 1.24 V<br>100001: 1.26 V<br>...<br>111000: 1.72 V<br>111001: 1.74 V<br>111010: 1.76 V<br>111011: 1.78 V<br>111100: 1.80 V<br>111101: 1.82 V<br>111110: 1.84 V<br>111111: 1.86 V |

## System PMIC for Mobile and Automotive Applications

Table 183: VLDO3\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xAB<br>VLDO3_A  | 7   | R/W  | LDO3_SL_A | 0: Configures LDO to normal mode, when selecting A voltage settings<br>1: Configures LDO to Sleep mode, when selecting A voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                  | 6:0 | R/W  | VLDO3_A   | 0000000: 0.90 V<br>0000001: 0.92 V<br>0000010: 0.94 V<br>0000011: 0.96 V<br>0000100: 0.98 V<br>0000101: 1.00 V<br>0000110: 1.02 V<br>0000111: 1.04 V<br>0001000: 1.06 V<br>0001001: 1.08 V<br>0001010: 1.10 V<br>0001011: 1.12 V<br>0001100: 1.14 V<br>0001101: 1.16 V<br>0001110: 1.18 V<br><b>0001111: 1.20 V</b><br>0010000: 1.22 V<br>0010001: 1.24 V<br>0010010: 1.26 V<br>0010011: 1.28 V<br>0010100: 1.30 V<br>0010101: 1.32 V<br>...<br>1110000: 3.14 V<br>1110001: 3.16 V<br>1110010: 3.18 V<br>1110011: 3.20 V<br>1110100: 3.22 V<br>1110101: 3.24 V<br>1110110: 3.26 V<br>1110111: 3.28 V<br>1111000: 3.30 V<br>1111001: 3.32 V<br>1111010: 3.34 V<br>1111011: 3.36 V<br>1111100: 3.38 V<br>1111101: 3.40 V<br>1111110: 3.42 V<br>1111111: 3.44 V |

## System PMIC for Mobile and Automotive Applications

Table 184: VLDO4\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xAC<br>VLDO4_A  | 7   | R/W  | LDO4_SL_A | <b>0: Configures LDO to normal mode, when selecting A voltage settings</b><br><b>1: Configures LDO to Sleep mode, when selecting A voltage settings</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                  | 6:0 | R/W  | VLDO4_A   | 0000000: 0.90 V<br>0000001: 0.92 V<br>0000010: 0.94 V<br>0000011: 0.96 V<br>0000100: 0.98 V<br>0000101: 1.00 V<br>0000110: 1.02 V<br>0000111: 1.04 V<br>0001000: 1.06 V<br>0001001: 1.08 V<br>0001010: 1.10 V<br>0001011: 1.12 V<br>0001100: 1.14 V<br>0001101: 1.16 V<br>0001110: 1.18 V<br>0001111: 1.20 V<br>0010000: 1.22 V<br>0010001: 1.24 V<br>0010010: 1.26 V<br>0010011: 1.28 V<br>0010100: 1.30 V<br>0010101: 1.32 V<br>...<br>1110000: 3.14 V<br>1110001: 3.16 V<br>1110010: 3.18 V<br>1110011: 3.20 V<br>1110100: 3.22 V<br>1110101: 3.24 V<br>1110110: 3.26 V<br>1110111: 3.28 V<br><b>1111000: 3.30 V</b><br>1111001: 3.32 V<br>1111010: 3.34 V<br>1111011: 3.36 V<br>1111100: 3.38 V<br>1111101: 3.40 V<br>1111110: 3.42 V<br>1111111: 3.44 V |

## System PMIC for Mobile and Automotive Applications

Table 185: VLDO5\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xAD<br>VLDO5_A  | 7   | R/W  | LDO5_SL_A | 0: Configures LDO to normal mode, when selecting A voltage settings<br>1: Configures LDO to Sleep mode, when selecting A voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO5_A   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br>101000: 2.80 V<br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br><b>110010: 3.30 V</b><br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 186: VLDO6\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xAE<br>VLDO6_A  | 7   | R/W  | LDO6_SL_A | 0: Configures LDO to normal mode, when selecting A voltage settings<br>1: Configures LDO to Sleep mode, when selecting A voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO6_A   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br><b>010100: 1.80 V</b><br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br>101000: 2.80 V<br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br>110010: 3.30 V<br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 187: VLDO7\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xAF<br>VLDO7_A  | 7   | R/W  | LDO7_SL_A | 0: Configures LDO to normal mode, when selecting A voltage settings<br>1: Configures LDO to Sleep mode, when selecting A voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO7_A   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br><b>101000: 2.80 V</b><br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br>110010: 3.30 V<br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 188: VLDO8\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xB0<br>VLDO8_A  | 7   | R/W  | LDO8_SL_A | 0: Configures LDO to normal mode, when selecting A voltage settings<br>1: Configures LDO to Sleep mode, when selecting A voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO8_A   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br><b>101000: 2.80 V</b><br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br>110010: 3.30 V<br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 189: VLDO9\_A

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------------------|-----|------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xB1<br>VLDO9_A  | 7   | R/W  | LDO9_SL_A | 0: Configures LDO to normal mode, when selecting A voltage settings<br>1: Configures LDO to Sleep mode, when selecting A voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                  | 5:0 | R/W  | VLDO9_A   | 000000: not used<br>000001: 0.95 V<br>000010: 0.95 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br><b>100010: 2.50 V</b><br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br>101000: 2.80 V<br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br>110010: 3.30 V<br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 190: VLDO10\_A

| Register Address | Bit | Type | Label      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xB2<br>VLDO10_A | 7   | R/W  | LDO10_SL_A | 0: Configures LDO to normal mode, when selecting A voltage settings<br>1: Configures LDO to Sleep mode, when selecting A voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO10_A   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br>101000: 2.80 V<br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br><b>110010: 3.30 V</b><br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 191: VLDO11\_A

| Register Address | Bit | Type | Label      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xB3<br>VLDO11_A | 7:4 | R/W  | LDO11_SL_A | 0: Configures LDO to normal mode, when selecting A voltage settings<br>1: Configures LDO to Sleep mode, when selecting A voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO11_A   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br>101000: 2.80 V<br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br><b>110010: 3.30 V</b><br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 192: VBCORE2\_B

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                        |
|-------------------|-----|------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|
| 0xB4<br>VBCORE2_B | 7   | R/W  | BCORE2_SL_B | <b>0: Configures BUCKCORE2 to Synchronous mode, when selecting B voltage settings</b><br>1: Configures BUCKCORE2 to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                          |                        |
|                   | 6:0 | R/W  | VBCORE2_B   | 0000000: 0.30 V<br>0000001: 0.31 V<br>0000010: 0.32 V<br>0000011: 0.33 V<br>0000100: 0.34 V<br>0000101: 0.35 V<br>...<br>0100101: 0.67 V<br>0100110: 0.68 V<br>0100111: 0.69 V<br>...<br>0101000: 0.70 V<br>0101001: 0.71 V<br>...<br><b>0111100: 0.90 V</b><br>...<br>1110011: 1.45 V<br>1110100: 1.46 V<br>1110101: 1.47 V<br>1110110: 1.48 V<br>1110111: 1.49 V<br>1111000: 1.50 V<br>1111001: 1.51 V<br>1111010: 1.52 V<br>1111011: 1.53 V<br>1111100: 1.54 V<br>1111101: 1.55 V<br>1111110: 1.56 V<br>1111111: 1.57 V | PWM mode voltage range |

## System PMIC for Mobile and Automotive Applications

Table 193: VBCORE1\_B

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------|-----|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xB5<br>VBCORE1_B | 7   | R/W  | BCORE1_SL_B | 0: Configures BUCKCORE1 to Synchronous mode, when selecting B voltage settings<br><b>1: Configures BUCKCORE1 to Sleep mode, when selecting B voltage settings</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                   | 6:0 | R/W  | VBCORE1_B   | <div> 0000000: 0.30 V<br/> 0000001: 0.31 V<br/> 0000010: 0.32 V<br/> 0000011: 0.33 V<br/> 0000100: 0.34 V<br/> 0000101: 0.35 V<br/> ...<br/> 0100101: 0.67 V<br/> 0100110: 0.68 V<br/> 0100111: 0.69 V<br/> ...<br/> 0101000: 0.70 V<br/> 0101001: 0.71 V<br/> ...<br/> <b>0111100: 0.90 V</b><br/> ...<br/> 1110011: 1.45 V<br/> 1110100: 1.46 V<br/> 1110101: 1.47 V<br/> 1110110: 1.48 V<br/> 1110111: 1.49 V<br/> 1111000: 1.50 V<br/> 1111001: 1.51 V<br/> 1111010: 1.52 V<br/> 1111011: 1.53 V<br/> 1111100: 1.54 V<br/> 1111101: 1.55 V<br/> 1111110: 1.56 V<br/> 1111111: 1.57 V </div> <div>PWM mode voltage range</div> |

## System PMIC for Mobile and Automotive Applications

Table 194: VBPRO\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xB6<br>VBPRO_B  | 7   | R/W  | BPRO_SL_B | 0: Configures BUCKPRO to Synchronous mode, when selecting B voltage settings<br>1: Configures BUCKPRO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                  | 6:0 | R/W  | VBPRO_B   | <div> 0000000: 0.53 V<br/> 0000001: 0.54 V<br/> 0000010: 0.55 V<br/> 0000011: 0.56 V<br/> 0000100: 0.57 V<br/> 0000101: 0.58 V<br/> ...<br/> 0010000: 0.69 V<br/> 0010001: 0.70 V<br/> 0010010: 0.71 V<br/> 0010011: 0.72 V<br/> 0010100: 0.73 V<br/> 0010101: 0.74 V<br/> 0010110: 0.75 V<br/> ...<br/> <b>1000011: 1.20 V</b><br/> ...<br/> 1110011: 1.68 V<br/> 1110100: 1.69 V<br/> 1110101: 1.70 V<br/> 1110110: 1.71 V<br/> 1110111: 1.72 V<br/> 1111000: 1.73 V<br/> 1111001: 1.74 V<br/> 1111010: 1.75 V<br/> 1111011: 1.76 V<br/> 1111100: 1.77 V<br/> 1111101: 1.78 V<br/> 1111110: 1.79 V<br/> 1111111: 1.80 V </div> <div>PWM mode voltage range</div> |

## System PMIC for Mobile and Automotive Applications

Table 195: VBMEM\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                  |
|------------------|-----|------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xB7<br>VBMEM_B  | 7   | R/W  | BMEM_SL_B | 0: Configures BUCKMEM to Synchronous mode, when selecting B voltage settings<br>1: Configures BUCKMEM to Sleep mode, when selecting B voltage settings                                       |
|                  | 6:0 | R/W  | VBMEM_B   | 0000000: 0.80 V<br>0000001: 0.82 V<br>0000010: 0.84 V<br>...<br>0010100: 1.20 V<br>...<br>0111100: 2.00 V<br>0111101: 2.02 V<br>0111110: 2.04 V<br>0111111: 2.06 V<br>...<br>1111111: 3.34 V |

Table 196: VBIO\_B

| Register Address | Bit | Type | Label    | Description                                                                                                                                                                                  |
|------------------|-----|------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xB8<br>VBIO_B   | 7   | R/W  | BIO_SL_B | 0: Configures BUCKIO to Synchronous mode, when selecting B voltage settings<br>1: Configures BUCKIO to Sleep mode, when selecting B voltage settings                                         |
|                  | 6:0 | R/W  | VBIO_B   | 0000000: 0.80 V<br>0000001: 0.82 V<br>0000010: 0.84 V<br>...<br>0010100: 1.20 V<br>...<br>0111100: 2.00 V<br>0111101: 2.02 V<br>0111110: 2.04 V<br>0111111: 2.06 V<br>...<br>1111111: 3.34 V |

Table 197: VBPERI\_B

| Register Address | Bit | Type | Label      | Description                                                                                                                                                                                  |
|------------------|-----|------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xB9<br>VBPERI_B | 7   | R/W  | BPERI_SL_B | 0: Configures BUCKPERI to Synchronous mode, when selecting A voltage settings<br>1: Configures BUCKPERI to Sleep mode, when selecting B voltage settings                                     |
|                  | 6:0 | R/W  | VBPERI_B   | 0000000: 0.80 V<br>0000001: 0.82 V<br>0000010: 0.84 V<br>...<br>0110010: 1.80 V<br>...<br>0111100: 2.00 V<br>0111101: 2.02 V<br>0111110: 2.04 V<br>0111111: 2.06 V<br>...<br>1111111: 3.34 V |

## System PMIC for Mobile and Automotive Applications

Table 198: VLDO1\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------------|-----|------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xBA<br>VLDO1_B  | 7   | R/W  | LDO1_SL_B | 0: Configures LDO to normal mode, when selecting B voltage settings<br>1: Configures LDO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                  | 5:0 | R/W  | VLDO1_B   | 000000: 0.60 V<br>000001: 0.62 V<br>000010: 0.64 V<br>000011: 0.66 V<br>000100: 0.68 V<br>000101: 0.70 V<br>000110: 0.72 V<br>000111: 0.74 V<br>001000: 0.76 V<br>001001: 0.78 V<br>001010: 0.80 V<br>001011: 0.82 V<br>001100: 0.82 V<br>001101: 0.86 V<br>001110: 0.88 V<br>001111: 0.90 V<br>010000: 0.92 V<br>010001: 0.94 V<br>010010: 0.96 V<br>010011: 0.98 V<br>010100: 1.00 V<br>010101: 1.02 V<br>010110: 1.04 V<br>010111: 1.06 V<br>011000: 1.08 V<br>011001: 1.10 V<br>011010: 1.12 V<br>011011: 1.14 V<br>011100: 1.16 V<br>011101: 1.18 V<br><b>011110: 1.20 V</b><br>011111: 1.22 V<br>100000: 1.24 V<br>100001: 1.26 V<br>...<br>111000: 1.72 V<br>111001: 1.74 V<br>111010: 1.76 V<br>111011: 1.78 V<br>111100: 1.80 V<br>111101: 1.82 V<br>111110: 1.84 V<br>111111: 1.86 V |

## System PMIC for Mobile and Automotive Applications

Table 199: VLDO2\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------------|-----|------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xBB<br>VLDO2_B  | 7   | R/W  | LDO2_SL_B | 0: Configures LDO to normal mode, when selecting B voltage settings<br>1: Configures LDO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                  | 5:0 | R/W  | VLDO2_B   | 000000: 0.60 V<br>000001: 0.62 V<br>000010: 0.64 V<br>000011: 0.66 V<br>000100: 0.68 V<br>000101: 0.70 V<br>000110: 0.72 V<br>000111: 0.74 V<br>001000: 0.76 V<br>001001: 0.78 V<br>001010: 0.80 V<br>001011: 0.82 V<br>001100: 0.82 V<br>001101: 0.86 V<br>001110: 0.88 V<br>001111: 0.90 V<br>010000: 0.92 V<br>010001: 0.94 V<br>010010: 0.96 V<br>010011: 0.98 V<br>010100: 1.00 V<br>010101: 1.02 V<br>010110: 1.04 V<br>010111: 1.06 V<br>011000: 1.08 V<br>011001: 1.10 V<br>011010: 1.12 V<br>011011: 1.14 V<br>011100: 1.16 V<br>011101: 1.18 V<br><b>011110: 1.20 V</b><br>011111: 1.22 V<br>100000: 1.24 V<br>100001: 1.26 V<br>...<br>111000: 1.72 V<br>111001: 1.74 V<br>111010: 1.76 V<br>111011: 1.78 V<br>111100: 1.80 V<br>111101: 1.82 V<br>111110: 1.84 V<br>111111: 1.86 V |

## System PMIC for Mobile and Automotive Applications

Table 200: VLDO3\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xBC<br>VLDO3_B  | 7   | R/W  | LDO3_SL_B | <b>0: Configures LDO to normal mode, when selecting B voltage settings</b><br><b>1: Configures LDO to Sleep mode, when selecting B voltage settings</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                  | 6:0 | R/W  | VLDO3_B   | 0000000: 0.90 V<br>0000001: 0.92 V<br>0000010: 0.94 V<br>0000011: 0.96 V<br>0000100: 0.98 V<br>0000101: 1.00 V<br>0000110: 1.02 V<br>0000111: 1.04 V<br>0001000: 1.06 V<br>0001001: 1.08 V<br>0001010: 1.10 V<br>0001011: 1.12 V<br>0001100: 1.14 V<br>0001101: 1.16 V<br>0001110: 1.18 V<br><b>0001111: 1.20 V</b><br>0010000: 1.22 V<br>0010001: 1.24 V<br>0010010: 1.26 V<br>0010011: 1.28 V<br>0010100: 1.30 V<br>0010101: 1.32 V<br>...<br>1110000: 3.14 V<br>1110001: 3.16 V<br>1110010: 3.18 V<br>1110011: 3.20 V<br>1110100: 3.22 V<br>1110101: 3.24 V<br>1110110: 3.26 V<br>1110111: 3.28 V<br>1111000: 3.30 V<br>1111001: 3.32 V<br>1111010: 3.34 V<br>1111011: 3.36 V<br>1111100: 3.38 V<br>1111101: 3.40 V<br>1111110: 3.42 V<br>1111111: 3.44 V |

## System PMIC for Mobile and Automotive Applications

Table 201: VLDO4\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xBD<br>VLDO4_B  | 7   | R/W  | LDO4_SL_B | 0: Configures LDO to normal mode, when selecting B voltage settings<br>1: Configures LDO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                  | 6:0 | R/W  | VLDO4_B   | 0000000: 0.90 V<br>0000001: 0.92 V<br>0000010: 0.94 V<br>0000011: 0.96 V<br>0000100: 0.98 V<br>0000101: 1.00 V<br>0000110: 1.02 V<br>0000111: 1.04 V<br>0001000: 1.06 V<br>0001001: 1.08 V<br>0001010: 1.10 V<br>0001011: 1.12 V<br>0001100: 1.14 V<br>0001101: 1.16 V<br>0001110: 1.18 V<br>0001111: 1.20 V<br>0010000: 1.22 V<br>0010001: 1.24 V<br>0010010: 1.26 V<br>0010011: 1.28 V<br>0010100: 1.30 V<br>0010101: 1.32 V<br>...<br>1110000: 3.14 V<br>1110001: 3.16 V<br>1110010: 3.18 V<br>1110011: 3.20 V<br>1110100: 3.22 V<br>1110101: 3.24 V<br>1110110: 3.26 V<br>1110111: 3.28 V<br><b>1111000: 3.30 V</b><br>1111001: 3.32 V<br>1111010: 3.34 V<br>1111011: 3.36 V<br>1111100: 3.38 V<br>1111101: 3.40 V<br>1111110: 3.42 V<br>1111111: 3.44 V |

## System PMIC for Mobile and Automotive Applications

Table 202: VLDO5\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xBE<br>VLDO5_B  | 7   | R/W  | LDO5_SL_B | 0: Configures LDO to normal mode, when selecting B voltage settings<br>1: Configures LDO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO5_B   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br>101000: 2.80 V<br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br><b>110010: 3.30 V</b><br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 203: VLDO6\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xBF<br>VLDO6_B  | 7   | R/W  | LDO6_SL_B | 0: Configures LDO to normal mode, when selecting B voltage settings<br>1: Configures LDO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO6_B   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br><b>010100: 1.80 V</b><br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br>101000: 2.80 V<br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br>110010: 3.30 V<br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 204: VLDO7\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xC0<br>VLDO7_B  | 7   | R/W  | LDO7_SL_B | 0: Configures LDO to normal mode, when selecting B voltage settings<br>1: Configures LDO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO7_B   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br><b>101000: 2.80 V</b><br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br>110010: 3.30 V<br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 205: VLDO8\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xC1<br>VLDO8_B  | 7   | R/W  | LDO8_SL_B | 0: Configures LDO to normal mode, when selecting B voltage settings<br>1: Configures LDO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO8_B   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br><b>101000: 2.80 V</b><br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br>110010: 3.30 V<br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 206: VLDO9\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xC2<br>VLDO9_B  | 7   | R/W  | LDO9_SL_B | 0: Configures LDO to normal mode, when selecting B voltage settings<br>1: Configures LDO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                  | 5:0 | R/W  | VLDO9_B   | 000000: 0.95 V<br>000001: 0.95 V<br>000010: 0.95 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001000: 1.20 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br><b>100010: 2.50 V</b><br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br>101000: 2.80 V<br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br>110010: 3.30 V<br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 207: VLDO10\_B

| Register Address | Bit | Type | Label      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------|-----|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xC3<br>VLDO10_B | 7   | R/W  | LDO10_SL_B | 0: Configures LDO to normal mode, when selecting B voltage settings<br>1: Configures LDO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                  | 6   | R/W  | Reserved   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                  | 5:0 | R/W  | VLDO10_B   | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br>101000: 2.80 V<br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br><b>110010: 3.30 V</b><br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

Table 208: VLDO11\_B

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xC4<br>VLDO11_B | 7:4 | R/W  | LDO1_SL_B | 0: Configures LDO to normal mode, when selecting B voltage settings<br>1: Configures LDO to Sleep mode, when selecting B voltage settings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                  | 6   | R/W  | Reserved  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                  | 5:0 | R/W  | VLDO11_B  | 000000: 0.90 V<br>000001: 0.90 V<br>000010: 0.90 V<br>000011: 0.95 V<br>000100: 1.00 V<br>000101: 1.05 V<br>000110: 1.10 V<br>000111: 1.15 V<br>001001: 1.25 V<br>001010: 1.30 V<br>001011: 1.35 V<br>001100: 1.40 V<br>001101: 1.45 V<br>001110: 1.50 V<br>001111: 1.55 V<br>010000: 1.60 V<br>010001: 1.65 V<br>010010: 1.70 V<br>010011: 1.75 V<br>010100: 1.80 V<br>010101: 1.85 V<br>...<br>100010: 2.50 V<br>100011: 2.55 V<br>100100: 2.60 V<br>100101: 2.65 V<br>100110: 2.70 V<br>100111: 2.75 V<br>101000: 2.80 V<br>101001: 2.85 V<br>101010: 2.90 V<br>101011: 2.95 V<br>101100: 3.00 V<br>101101: 3.05 V<br>101110: 3.10 V<br>101111: 3.15 V<br>110000: 3.20 V<br>110001: 3.25 V<br><b>110010: 3.30 V</b><br>110011: 3.35 V<br>110100: 3.40 V<br>110101: 3.45 V<br>110110: 3.50 V<br>110111: 3.55 V<br>111000: 3.60 V<br>>111000: 3.60 V |

## System PMIC for Mobile and Automotive Applications

### A.3.3 Backup Battery Charger

Table 209: BBAT\_CONT

| Register Address  | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                            |
|-------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xC5<br>BBAT_CONT | 7:4 | R/W  | BCHG_ISET | <b>0000: disabled</b><br>0001: 100 $\mu$ A<br>0010: 200 $\mu$ A<br>0011: 300 $\mu$ A<br>0100: 400 $\mu$ A<br>0101: 500 $\mu$ A<br>0110: 600 $\mu$ A<br>0111: 700 $\mu$ A<br>1000: 800 $\mu$ A<br>1001: 900 $\mu$ A<br>1010: 1 mA<br>1011: 2 mA<br>1100: 3 mA<br>1101: 4 mA<br>1110: 5 mA<br>1111: 6 mA |
|                   | 3:0 | R/W  | BCHG_VSET | 0000: disabled<br>0001: 1.1 V<br>0010: 1.2 V<br>0011: 1.4 V<br>0100: 1.6 V<br>0101: 1.8 V<br>0110: 2.0 V<br>0111: 2.2 V<br>1000: 2.4 V<br>1001: 2.5 V<br>1010: 2.6 V<br>1011: 2.7 V<br>1100: 2.8 V<br>1101: 2.9 V<br><b>1110: 3.0 V</b><br>1111: 3.1 V                                                 |

## System PMIC for Mobile and Automotive Applications

### A.3.4 High Power GPO PWM

Table 210: GPO11\_LED

| Register Address  | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xC6<br>GPO11_LED | 7   | R/W  | GPO11_DIM | <b>0: PWM ratio changes instantly</b><br>1: GPO ramps between changes in PWM ratio with 32 ms per step                                                                                                                                                                                                                                                                                                                         |
|                   | 6:0 | R/W  | GPO11_PWM | GPO11 LED on-time (low level at GPIO 11, period 21 kHz = 95 cycles of 0.5 $\mu$ s)<br><b>0000000: off</b><br>0000001: 1%<br>0000010: 2% (1 $\mu$ s bursts)<br>0000011: 3%<br>0000100: 4%<br>0000101: 5%<br>0000110: 6%<br>0000111: 7%<br>0001000: 8%<br>0001001: 9%<br>0001010: 10%<br>0001011: 11%<br>0001100: 12%<br>0001101: 13%<br>0001110: 14%<br>0001111: 15%<br>0010000: 16%<br>....<br>1011111: 100%<br>>1011111: 100% |

Table 211: GPO14\_LED

| Register Address  | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xC7<br>GPO14_LED | 7   | R/W  | GPO14_DIM | <b>0: PWM ratio changes instantly</b><br>1: GPO ramps between changes in PWM ratio with 32 ms per step                                                                                                                                                                                                                                                                                                                         |
|                   | 6:0 | R/W  | GPO14_PWM | GPO14 LED on-time (low level at GPIO 14, period 21 kHz = 95 cycles of 0.5 $\mu$ s)<br><b>0000000: off</b><br>0000001: 1%<br>0000010: 2% (1 $\mu$ s bursts)<br>0000011: 3%<br>0000100: 4%<br>0000101: 5%<br>0000110: 6%<br>0000111: 7%<br>0001000: 8%<br>0001001: 9%<br>0001010: 10%<br>0001011: 11%<br>0001100: 12%<br>0001101: 13%<br>0001110: 14%<br>0001111: 15%<br>0010000: 16%<br>....<br>1011111: 100%<br>>1011111: 100% |

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Table 212: GPO15\_LED

| Register Address  | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------------|-----|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xC8<br>GPO15_LED | 7   | R/W  | GPO15_DIM | <b>0: PWM ratio changes instantly</b><br>1: GPO ramps between changes in PWM ratio with 32 ms per step                                                                                                                                                                                                                                                                                                                         |
|                   | 6:0 | R/W  | GPO15_PWM | GPO15 LED on-time (low level at GPIO 15, period 21 kHz = 95 cycles of 0.5 $\mu$ s)<br><b>0000000: off</b><br>0000001: 1%<br>0000010: 2% (1 $\mu$ s bursts)<br>0000011: 3%<br>0000100: 4%<br>0000101: 5%<br>0000110: 6%<br>0000111: 7%<br>0001000: 8%<br>0001001: 9%<br>0001010: 10%<br>0001011: 11%<br>0001100: 12%<br>0001101: 13%<br>0001110: 14%<br>0001111: 15%<br>0010000: 16%<br>....<br>1011111: 100%<br>>1011111: 100% |

## System PMIC for Mobile and Automotive Applications

### A.3.5 GPADC Thresholds

Table 213: ADC\_CFG

| Register Address | Bit | Type | Label      | Description                                                                                                     |
|------------------|-----|------|------------|-----------------------------------------------------------------------------------------------------------------|
| 0xC9<br>ADC_CFG  | 7   | R/W  | ADCIN3_DEB | 0: ADCIN3: debouncing off<br>1: <b>ADCIN3: debouncing on</b>                                                    |
|                  | 6   | R/W  | ADCIN2_DEB | 0: ADCIN2: debouncing off<br>1: <b>ADCIN2: debouncing on</b>                                                    |
|                  | 5   | R/W  | ADCIN1_DEB | 0: ADCIN1: debouncing off<br>1: <b>ADCIN1: debouncing on</b>                                                    |
|                  | 4   | R/W  | ADCIN3_CUR | ADCIN3 current source:<br>0: <b>10 <math>\mu</math>A</b><br>1: 40 $\mu$ A                                       |
|                  | 3:2 | R/W  | ADCIN2_CUR | ADCIN2 current source:<br>00: 1 $\mu$ A<br>01: 2.5 $\mu$ A<br>10: <b>10 <math>\mu</math>A</b><br>11: 40 $\mu$ A |
|                  | 1:0 | R/W  | ADCIN1_CUR | ADCIN1 current source:<br>00: 1 $\mu$ A<br>01: 2.5 $\mu$ A<br>10: <b>10 <math>\mu</math>A</b><br>11: 40 $\mu$ A |

Table 214: AUTO1\_HIGH

| Register Address   | Bit | Type | Label      | Description                                      |
|--------------------|-----|------|------------|--------------------------------------------------|
| 0xCA<br>AUTO1_HIGH | 7:0 | R/W  | AUTO1_HIGH | 00000000 – 11111111: ADCIN1 high level threshold |

Table 215: AUTO1\_LOW

| Register Address  | Bit | Type | Label     | Description                                     |
|-------------------|-----|------|-----------|-------------------------------------------------|
| 0xCB<br>AUTO1_LOW | 7:0 | R/W  | AUTO1_LOW | 00000000 – 11111111: ADCIN1 low level threshold |

Table 216: AUTO2\_HIGH

| Register Address   | Bit | Type | Label      | Description                                      |
|--------------------|-----|------|------------|--------------------------------------------------|
| 0xCC<br>AUTO2_HIGH | 7:0 | R/W  | AUTO2_HIGH | 00000000 – 11111111: ADCIN2 high level threshold |

Table 217: AUTO2\_LOW

| Register Address  | Bit | Type | Label     | Description                                     |
|-------------------|-----|------|-----------|-------------------------------------------------|
| 0xCD<br>AUTO2_LOW | 7:0 | R/W  | AUTO2_LOW | 00000000 – 11111111: ADCIN2 low level threshold |

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Table 218: AUTO3\_HIGH

| Register Address   | Bit | Type | Label      | Description                                      |
|--------------------|-----|------|------------|--------------------------------------------------|
| 0xCE<br>AUTO3_HIGH | 7:0 | R/W  | AUTO3_HIGH | 00000000 – 11111111: ADCIN3 high level threshold |

Table 219: AUTO3\_LOW

| Register Address  | Bit | Type | Label     | Description                                     |
|-------------------|-----|------|-----------|-------------------------------------------------|
| 0xCF<br>AUTO3_LOW | 7:0 | R/W  | AUTO3_LOW | 00000000 – 11111111: ADCIN3 low level threshold |

Table 220: Copmic\_S to Copmic\_E

| Register Address | Bit | Type | Label    | Description          |
|------------------|-----|------|----------|----------------------|
| 0xD0<br>CoPMIC_S | 7:0 | R    | Reserved | Reserved for Co-PMIC |
| 0xDF<br>CoPMIC_E | 7:0 | R    | Reserved | Reserved for Co-PMIC |

Table 221: CHG\_Co\_S to CHG\_Co\_E

| Register Address | Bit | Type | Label    | Description                    |
|------------------|-----|------|----------|--------------------------------|
| 0xE0<br>CHG_Co_S | 7:0 | R    | Reserved | Reserved for companion charger |
| 0xFF<br>CHG_Co_E | 7:0 | R    | Reserved | Reserved for companion charger |

## System PMIC for Mobile and Automotive Applications

### A.4 Register Page 2

Table 222: PAGE\_CON

| Register Address  | Bit | Type | Label      | Description                                 |
|-------------------|-----|------|------------|---------------------------------------------|
| 0x100<br>PAGE_CON | 7   | RW   | REVERT     | See register 0x00, <a href="#">Table 59</a> |
|                   | 6   | RW   | WRITE_MODE |                                             |
|                   | 5:3 | RW   | Reserved   |                                             |
|                   | 2:0 | RW   | REG_PAGE   |                                             |

#### A.4.1 OTP

Table 223: OTP\_CONT

| Register Address  | Bit | Type | Label         | Description                                                                                                                                                                                                                                            |
|-------------------|-----|------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x101<br>OTP_CONT | 7   | R    | GP_WRITE_DIS  | <b>0: Enables write access to GP_ID registers</b><br>1: GP_ID_0 to GP_ID_9 registers are 'read only'                                                                                                                                                   |
|                   | 6   | R    | OTP_CONF_LOCK | 0: Registers 0x0A to 0x36 and 0x82 to 0xCF are not locked for OTP programming (only for evaluation samples)<br><b>1: OTP registers 0x0A to 0x36 and 0x82 to 0xCF are locked in OTP (set for all mass production parts, no further fusing possible)</b> |
|                   | 5   | R    | OTP_APPS_LOCK | 0: Registers 0x104 to 0x117 are not locked for OTP programming (only for evaluation samples)<br><b>1: OTP registers 0x104 to 0x117 are locked in OTP (set for all mass production parts, no further fusing possible)</b>                               |
|                   | 4   | R    | OTP_GP_LOCK   | <b>0: Registers 0x120 to 0x134 are not locked for OTP programming</b><br>1: Registers 0x120 to 0x134 are locked in OTP (no further fusing possible if once fused with 1)                                                                               |
|                   | 3   | R/W  | PC_DONE       | Asserted from Power Commander SW after emulated OTP read has finished (control shared with Co-PMIC), automatically cleared when leaving emulated OTP read                                                                                              |
|                   | 2   | R/W  | OTP_APPS_RD   | Reads on assertion application specific registers (0x104 to 0x117 and OTP_APPS_LOCK) from OTP                                                                                                                                                          |
|                   | 1   | R/W  | OTP_GP_RD     | Reads on assertion device specific registers 0x120 to 0x134 (plus GP_WRITE_DIS and OTP_GP_LOCK) from OTP                                                                                                                                               |
|                   | 0   | R/W  | OTP_TIM       | OTP read timing<br><b>0: normal read</b><br>1: marginal read (for OTP fuse verification)                                                                                                                                                               |

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Table 224: OTP\_ADDR

| Register Address  | Bit | Type | Label    | Description                                   |
|-------------------|-----|------|----------|-----------------------------------------------|
| 0x102<br>OTP_ADDR | 7:0 | R/W  | OTP_ADDR | OTP Array address (shared with Companion ICs) |

Table 225: OTP\_DATA

| Register Address  | Bit | Type | Label    | Description                                                                                                                              |
|-------------------|-----|------|----------|------------------------------------------------------------------------------------------------------------------------------------------|
| 0x103<br>OTP_DATA | 7:0 | R/W  | OTP_DATA | OTP read/write data (shared with Companion ICs)<br>OTP_DATA written to OTP_ADDR selects the IC and accepts unlock sequence (1 + 3 bytes) |

### A.4.2 Customer Trim and Configuration

Table 226: T\_OFFSET

| Register Address  | Bit | Type | Label    | Description                                                                                                                                                             |
|-------------------|-----|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x104<br>T_OFFSET | 7:0 | R    | T_OFFSET | 10000000 – 01111111: signed two's complement calibration offset for junction temperature measurement (loaded from the OTP memory, must be programmed during production) |

Table 227: INTERFACE

| Register Address   | Bit | Type<br>Note 1 | Label        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------------------|-----|----------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x105<br>INTERFACE | 7:4 | R              | IF_BASE_ADDR | 4 MSB of 2-WIRE control interfaces base address<br>XXXX0000<br><b>10110000</b> = 0xB0 write address of PM 2-WIRE interface (page 0 and 1)<br><b>10110001</b> = 0xB1 read address of PM 2-WIRE interface (page 0 and 1)<br><b>10110010</b> = 0xB2 write address of PM-2-WIRE interface (page 2 and 3)<br><b>10110011</b> = 0xB3 read address of PM-2-WIRE interface (page 2 and 3)<br><b>10110100</b> = 0xB4 write address of HS 2-WIRE interface (page 0 and 1)<br><b>10110101</b> = 0xB5 read address of HS 2-WIRE interface (page 0 and 1)<br><b>10110110</b> = 0xB6 write address of HS-2-WIRE interface (page 2 and 3)<br><b>10110111</b> = 0xB7 read address of HS-2-WIRE interface (page 2 and 3)<br>Code '0000' is reserved for unprogrammed OTP (triggers start-up with hardware default interface address) |
|                    | 3   | R              | R/W_POL      | 4-WIRE: Read/Write bit polarity<br>0: Host indicates reading access via R/W bit = 0<br><b>1: Host indicates reading access via R/W bit = 1</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type<br>Note 1 | Label   | Description                                                                                     |
|------------------|-----|----------------|---------|-------------------------------------------------------------------------------------------------|
|                  | 2   | R              | CPHA    | 4-WIRE IF clock phase (see Table 43)                                                            |
|                  | 1   | R              | CPOL    | 4-WIRE IF clock polarity<br><b>0: SK is low during idle</b><br><b>1: SK is high during idle</b> |
|                  | 0   | R              | nCS_POL | 4-WIRE chip select polarity<br><b>0: nCS is active low</b><br><b>1: nCS is active high</b>      |

**Note 1** The interface configuration can be written/modified only for unmarked samples which do not have the control OTP\_APPS\_LOCK asserted/fused.

**Table 228: CONFIG\_A**

| Register Address  | Bit | Type        | Label     | Description                                                                                                                                                         |
|-------------------|-----|-------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x106<br>CONFIG_A | 7   | R<br>Note 1 | IF_TYPE   | <b>0: Power manager IF is 4-WIRE</b><br><b>1: Power manager IF is 2-WIRE</b>                                                                                        |
|                   | 6   | R/W         | PM_IF_HSM | Enables continuous High Speed mode on PM 2-WIRE IF if asserted (no master code required)                                                                            |
|                   | 5   | R/W         | PM_IF_FMP | Selects fast-mode+ timings for PM 2-WIRE IF if asserted                                                                                                             |
|                   | 4   | R/W         | PM_IF_V   | <b>0: Power manager IF in 4-WIRE mode is supplied from VDD_IO1, in 2-WIRE mode from VDDCORE</b><br><b>1: Power manager IF (4-WIRE/2-WIRE) supplied from VDD_IO2</b> |
|                   | 3   | R/W         | IRQ_TYPE  | nIRQ output is:<br><b>0: Active low</b><br><b>1: Active high (invert signal)</b>                                                                                    |
|                   | 2   | R/W         | PM_O_TYPE | nRESET, nIRQ output are:<br><b>0: Push-pull</b><br><b>1: Open drain (requires external pull-up resistor)</b>                                                        |
|                   | 1   | R/W         | PM_O_V    | OUT_32K, OUT_32K_2, E_GPI_2, COMP1V2, nRESET, nIRQ are supplied from:<br><b>0: VDD_IO1</b><br><b>1: VDD_IO2</b>                                                     |
|                   | 0   | R/W         | PM_I_V    | nOFF, nSHUTDOWN, SYS_EN, PWR_EN, PWR1_EN, KEEP_ACT, nVIB_BRAKE are supplied from:<br><b>0: VDDCORE</b><br><b>1: VDD_IO2</b>                                         |

**Note 1** The interface configuration can be written/modified only for unmarked samples which do not have the control OTP\_APPS\_LOCK asserted/fused.

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Table 229: CONFIG\_B

| Register Address  | Bit | Type | Label         | Description                                                                                                                                               |
|-------------------|-----|------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x107<br>CONFIG_B | 7   | R/W  | Reserved      |                                                                                                                                                           |
|                   | 6:4 | R/W  | VDD_HYST_ADJ  | Hysteresis adjust of VDD_FAULT comparator (VDD_FAULT_UPPER) in 50 mV steps<br>000: 100 mV<br><b>001: 150 mV</b><br>...<br>111: 450 mV                     |
|                   | 3:0 | R/W  | VDD_FAULT_ADJ | Setting of VDD_FAULT_LOWER comparator in 50 mV steps<br>0000: 2.50 V<br>0001: 2.55 V<br>...<br><b>0110: 2.80 V</b><br>...<br>1110: 3.20 V<br>1111: 3.25 V |

Table 230: CONFIG\_C

| Register Address  | Bit | Type | Label            | Description                                                                                                   |
|-------------------|-----|------|------------------|---------------------------------------------------------------------------------------------------------------|
| 0x108<br>CONFIG_C | 7   | R/W  | BPERI_CLK_INV    | BUCKPERI clock polarity<br>0: Normal<br>1: Inverted                                                           |
|                   | 6   | R/W  | BIO_CLK_INV      | BUCKIO clock polarity<br>0: Normal<br>1: Inverted                                                             |
|                   | 5   | R/W  | BMEM_CLK_INV     | BUCKMEM clock polarity<br>0: Normal<br>1: Inverted                                                            |
|                   | 4   | R/W  | BPRO_CLK_INV     | BUCKPRO clock polarity (should be configured opposite to BUCKMEM clock polarity)<br>0: Normal<br>1: Inverted  |
|                   | 3   | R/W  | BCORE1_CLK_INV   | BUCKCORE1 clock polarity (BUCKCORE2 always runs on opposite clock polarity)<br>0: Normal<br>1: Inverted       |
|                   | 2   | R/W  | BUCK_ACTV_DISCHG | Enable active discharge of buck rails                                                                         |
|                   | 1:0 | R/W  | LDO1_TRACK       | LDO1 follows voltage transitions of<br><b>00: none</b><br>01: VBUCK_PRO<br>10: VBUCK_CORE1<br>11: VBUCK_CORE2 |

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Table 231: CONFIG\_D

| Register Address  | Bit | Type | Label        | Description                                                                                                                                           |
|-------------------|-----|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x109<br>CONFIG_D | 7   | R/W  | GP_FB3_TYPE  | GP_FB3 output is:<br><b>0: Active low</b><br>1: Active high (invert signal)                                                                           |
|                   | 6   | R/W  | GP_FB2_TYPE  | GP_FB2 output is:<br>0: Active low (invert signal, push-pull for PWR_OK)<br><b>1: Active high (open drain for PWR_OK)</b>                             |
|                   | 5   | R/W  | FORCE_RESET  | Asserts port nRESET in case of being set                                                                                                              |
|                   | 4   | R/W  | HS_IF_HSM    | Enables continuous High Speed mode on HS 2-WIRE IF (no master code required)                                                                          |
|                   | 3   | R/W  | HS_IF_FMP    | Selects fast-mode+ timings for HS 2-WIRE IF if asserted                                                                                               |
|                   | 2   | R/W  | SYSTEM_EN_RD | During second OTP read control SYSTEM_EN is<br><b>0: updated from OTP</b><br>1: not changed                                                           |
|                   | 1   | R/W  | nIRQ_MODE    | nIRQ will be asserted from events during POWERDOWN mode (and modes lower than ACTICE)<br><b>0: immediately</b><br>1: after powering up to ACTIVE mode |
|                   | 0   | R/W  | GPI_V        | GPis (not configured as Power Manager control inputs) and HS-2-WIRE IF are supplied from:<br><b>0: VDDCORE</b><br>1: VDD_IO2                          |

Table 232: CONFIG\_E

| Register Address  | Bit | Type | Label        | Description                                                                            |
|-------------------|-----|------|--------------|----------------------------------------------------------------------------------------|
| 0x10A<br>CONFIG_E | 7   | R/W  | PERI_SW_AUTO | Selects PERI_SW (during powering up):<br>0: configured from PERI_SW_CONF<br>1: enabled |
|                   | 6   | R/W  | CORE_SW_AUTO | Selects CORE_SW (during powering up):<br>0: configured from CORE_SW_CONF<br>1: enabled |
|                   | 5   | R/W  | BPERI_AUTO   | Selects BUCKPERI (during powering up):<br>0: configured from BPERI_CONF<br>1: enabled  |
|                   | 4   | R/W  | BIO_AUTO     | Selects BUCKIO (during powering up):<br>0: configured from BIO_CONF<br>1: enabled      |
|                   | 3   | R/W  | BMEM_AUTO    | Selects BUCKMEM (during powering up):<br>0: configured from BMEM_CONF<br>1: enabled    |
|                   | 2   | R/W  | BPRO_AUTO    | Selects BUCKPRO (during powering up):<br>0: configured from BPRO_CONF<br>1: enabled    |

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| Register Address | Bit | Type | Label              | Description                                                                             |
|------------------|-----|------|--------------------|-----------------------------------------------------------------------------------------|
|                  | 1   | R/W  | <b>BCORE2_AUTO</b> | Selects BUCKCORE2 (during powering up):<br>0: configured from BCORE2_CONF<br>1: enabled |
|                  | 0   | R/W  | <b>BCORE1_AUTO</b> | Selects BUCKCORE1 (during powering up):<br>0: configured from BCORE1_CONF<br>1: enabled |

Table 233: CONFIG\_F

| Register Address  | Bit | Type | Label             | Description                                                                        |
|-------------------|-----|------|-------------------|------------------------------------------------------------------------------------|
| 0x10B<br>CONFIG_F | 7   | R/W  | <b>LDO11_BYP</b>  | <b>0: LDO11 is configured for regulator mode</b><br>1: LDO11 bypass mode enabled   |
|                   | 6   | R/W  | <b>LDO8_BYP</b>   | <b>0: LDO8 is configured for regulator mode</b><br>1: LDO8 bypass mode enabled     |
|                   | 5   | R/W  | <b>LDO7_BYP</b>   | <b>0: LDO7 is configured for regulator mode</b><br>1: LDO7 bypass mode enabled     |
|                   | 4   | R/W  | <b>LDO4_BYP</b>   | <b>0: LDO4 is configured for regulator mode</b><br>1: LDO4 bypass mode enabled     |
|                   | 3   | R/W  | <b>LDO3_BYP</b>   | <b>0: LDO3 is configured for regulator mode</b><br>1: LDO3 bypass mode enabled     |
|                   | 2   | R/W  | <b>LDO11_AUTO</b> | Selects LDO11 (during powering up):<br>0: configured from LDO11_CONF<br>1: enabled |
|                   | 1   | R/W  | <b>LDO10_AUTO</b> | Selects LDO10 (during powering up):<br>0: configured from LDO10_CONF<br>1: enabled |
|                   | 0   | R/W  | <b>LDO9_AUTO</b>  | Selects LDO9 (during powering up):<br>0: configured from LDO9_CONF<br>1: enabled   |

Table 234: CONFIG\_G

| Register Address  | Bit | Type | Label            | Description                                                                      |
|-------------------|-----|------|------------------|----------------------------------------------------------------------------------|
| 0x10C<br>CONFIG_G | 7   | R/W  | <b>LDO8_AUTO</b> | Selects LDO8 (during powering up):<br>0: configured from LDO8_CONF<br>1: enabled |
|                   | 6   | R/W  | <b>LDO7_AUTO</b> | Selects LDO7 (during powering up):<br>0: configured from LDO7_CONF<br>1: enabled |
|                   | 5   | R/W  | <b>LDO6_AUTO</b> | Selects LDO6 (during powering up):<br>0: configured from LDO6_CONF<br>1: enabled |
|                   | 4   | R/W  | <b>LDO5_AUTO</b> | Selects LDO5 (during powering up):<br>0: configured from LDO5_CONF<br>1: enabled |
|                   | 3   | R/W  | <b>LDO4_AUTO</b> | Selects LDO4 (during powering up):<br>0: configured from LDO4_CONF<br>1: enabled |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label            | Description                                                                      |
|------------------|-----|------|------------------|----------------------------------------------------------------------------------|
|                  | 2   | R/W  | <b>LDO3_AUTO</b> | Selects LDO3 (during powering up):<br>0: configured from LDO3_CONF<br>1: enabled |
|                  | 1   | R/W  | <b>LDO2_AUTO</b> | Selects LDO2 (during powering up):<br>0: configured from LDO2_CONF<br>1: enabled |
|                  | 0   | R/W  | <b>LDO1_AUTO</b> | Selects LDO1 (during powering up):<br>0: configured from LDO1_CONF<br>1: enabled |

Table 235: CONFIG\_H

| Register Address  | Bit | Type | Label              | Description                                                                                                                                                                                                                                                                                                                                                |
|-------------------|-----|------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x10D<br>CONFIG_H | 7   | R/W  | <b>BUCK_MERGE</b>  | Has to be set if the outputs of BUCKMEM and BUCKIO are merged towards a single coil; the control from BUCKIO registers is disabled                                                                                                                                                                                                                         |
|                   | 6   | R/W  | <b>BCORE1_OD</b>   | If set, BUCKCORE1 changes to full-current mode (double pass device and current limit)                                                                                                                                                                                                                                                                      |
|                   | 5   | R/W  | <b>BCORE2_OD</b>   | If set, BUCKCORE2 changes to full-current mode (double pass device and current limit)                                                                                                                                                                                                                                                                      |
|                   | 4   | R/W  | <b>BPRO_OD</b>     | If set, BUCKPRO changes to full-current mode (double pass device and current limit)                                                                                                                                                                                                                                                                        |
|                   | 3   | R/W  | <b>BCORE_MERGE</b> | Has to be set if the outputs of BUCKCORE1 and BUCKCORE2 are merged towards a dual phase buck; the control from BUCKCORE2 registers is disabled                                                                                                                                                                                                             |
|                   | 2   | R/W  | <b>MERGE_SENSE</b> | In case BUCKCORE is merged and configured for remote sensing the output capacitor voltage rail is routed to port:<br><b>0: GP_FB_2 (setting disables normal GP_FB_2 functionality)</b><br>1: CORE_SWS (setting disables CORE rail switch pull-down functionality)<br>Note: In case MERGE_SENSE is asserted all Bxxx_FB control settings 0bxx1x are invalid |
|                   | 1   | R/W  | <b>LDO8_MODE</b>   | <b>0: LDO mode (external capacitor required)</b><br>1: Vibration motor driver (no external capacitor)                                                                                                                                                                                                                                                      |
|                   | 0   | R/W  | <b>PWM_CLK</b>     | <b>0: 2.0 MHz (31.25 kHz repetition frequency)</b><br>1: 1.0 MHz (15.6 kHz repetition frequency)                                                                                                                                                                                                                                                           |

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Table 236: CONFIG\_I

| Register Address  | Bit | Type | Label        | Description                                                                                                                                                                                                                                                                                                                                                          |
|-------------------|-----|------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x10E<br>CONFIG_I | 7   | R/W  | LDO_SD       | If asserted LDO3, 4, 7, 8 and 11 will shut down after current limit was hit for more than 200 ms                                                                                                                                                                                                                                                                     |
|                   | 6   | R/W  | INT_SD_MODE  | Shut down sequence from internal fault condition is:<br><b>0: Normal</b><br><b>1: Fast (skipping seq and dummy slot timers)</b>                                                                                                                                                                                                                                      |
|                   | 5   | R/W  | HOST_SD_MODE | Shut down sequence from SHUTDOWN (register bit or port nSHUTDOWN) is:<br><b>0: Normal</b><br><b>1: Fast (skipping seq and dummy slot timers)</b>                                                                                                                                                                                                                     |
|                   | 4   | R/W  | KEY_SD_MODE  | User triggered (nONKEY, GPIO14/15) shutdown sequence is:<br><b>0: Normal</b><br><b>1: PMU POR:</b> triggers an instant disable of all regulators incl. LDOCORE (RTC and FAULTLOG registers remain unchanged). After leaving POR automatically the RESET_DURATION timer must expire before starting a power-up sequence.                                              |
|                   | 3   | R/W  | GPI14_15_SD  | <b>0: Disables shutdown via parallel assertion of GPI14 and GPI15</b><br><b>1: Enables shutdown via GPI14 &amp; GPI15</b>                                                                                                                                                                                                                                            |
|                   | 2   | R/W  | nONKEY_SD    | nONKEY is configured<br><b>0: without shutdown via long press of nONKEY</b><br><b>1: with shutdown via long press of nONKEY</b>                                                                                                                                                                                                                                      |
|                   | 1:0 | R/W  | nONKEY_PIN   | nONKEY is configured to<br><b>00: Port mode</b><br><b>01: Key mode with key lock during SW triggered POWERDOWN mode</b><br><b>10: Key mode with key locked autonomous powering down (multi-functional key)</b><br><b>11: Key mode with autonomous powering down to partial or key locked full POWERDOWN mode (dedicated power key)</b><br>Details: see Section 6.1.1 |

Table 237: CONFIG\_J

| Register Address  | Bit | Type | Label      | Description                                                                       |
|-------------------|-----|------|------------|-----------------------------------------------------------------------------------|
| 0x10F<br>CONFIG_J | 7   | R/W  | IF_RESET   | Enables automatic reset of all control interfaces when port nSHUTDOWN is asserted |
|                   | 6   | R/W  | TWOWIRE_TO | Enables automatic reset of 2-WIRE-IF in case of clock ceases to toggle for >19 ms |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label                 | Description                                                                                                                                                                  |
|------------------|-----|------|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 5:4 | R/W  | <b>RESET_DURATION</b> | Power controller stays in RESET mode for minimum duration of<br>00: 20 ms<br>01: 100 ms<br><b>10: 500 ms</b><br>11: 1000 ms                                                  |
|                  | 3:2 | R/W  | <b>SHUT_DELAY</b>     | Long press time threshold for shutdown feature from nONKEY and GPIO14/15:<br>00: KEY_DELAY + 0 s<br>01: KEY_DELAY + 4 s<br><b>10: KEY_DELAY + 5 s</b><br>11: KEY_DELAY + 6 s |
|                  | 1:0 | R/W  | <b>KEY_DELAY</b>      | Long press threshold for nONKEY lock:<br>00: nONKEY_LOCK after 1 s<br>01: nONKEY_LOCK after 1.5 s<br><b>10: nONKEY_LOCK after 2 s</b><br>11: nONKEY_LOCK after 7 s           |

**Note 1** This setting may trigger glides on regulator outputs and disable the automatic RESET/POR of slave PMUs).

**Table 238: CONFIG\_K**

| Register Address  | Bit | Type | Label             | Description                                                                                                                                                                                                                                      |
|-------------------|-----|------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x110<br>CONFIG_K | 7   | R/W  | <b>GPIO7_PUPD</b> | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE) |
|                   | 6   | R/W  | <b>GPIO6_PUPD</b> | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE) |
|                   | 5   | R/W  | <b>GPIO5_PUPD</b> | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE) |
|                   | 4   | R/W  | <b>GPIO4_PUPD</b> | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE) |
|                   | 3   | R/W  | <b>GPIO3_PUPD</b> | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE) |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label      | Description                                                                                                                                                                                                                                         |
|------------------|-----|------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 2   | R/W  | GPIO2_PUPD | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |
|                  | 1   | R/W  | GPIO1_PUPD | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |
|                  | 0   | R/W  | GPIO0_PUPD | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |

Table 239: CONFIG\_L

| Register Address  | Bit | Type | Label       | Description                                                                                                                                                                                                                                         |
|-------------------|-----|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x111<br>CONFIG_L | 7   | R/W  | GPIO15_PUPD | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |
|                   | 6   | R/W  | GPIO14_PUPD | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |
|                   | 5   | R/W  | GPIO13_PUPD | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |
|                   | 4   | R/W  | GPIO12_PUPD | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |
|                   | 3   | R/W  | GPIO11_PUPD | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label       | Description                                                                                                                                                                                                                                         |
|------------------|-----|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 2   | R/W  | GPIO10_PUPD | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |
|                  | 1   | R/W  | GPIO9_PUPD  | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |
|                  | 0   | R/W  | GPIO8_PUPD  | <b>0: GPI: pull-down resistor disabled<br/>GPO (open drain): pull-up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull-up resistor enabled<br>(supply rail selected via GPIOx_TYPE) |

Table 240: CONFIG\_M

| Register Address  | Bit | Type | Label    | Description                                                                                                                                  |
|-------------------|-----|------|----------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 0x112<br>CONFIG_M | 7:4 | R/W  | OSC_FRQ  | Offset for internal HF oscillator frequency<br>1000: -10.67 %<br>...<br>1111: -1.33 %<br>0000: 0.00 %<br>0001: 1.33 %<br>...<br>0111: 9.33 % |
|                   | 3:0 | R/W  | Reserved |                                                                                                                                              |

Table 241: Reserved

| Register Address | Bit | Type | Label    | Description |
|------------------|-----|------|----------|-------------|
| 0x113            | 7:0 | R/W  | Reserved |             |

Table 242: MON\_REG\_1

| Register Address   | Bit | Type | Label      | Description                                                                                                                                                                     |
|--------------------|-----|------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x114<br>MON_REG_1 | 7:6 | R/W  | UVOV_DELAY | Range comparison is enabled after regulator enable:<br>00: immediately<br>01: with one measurement delay<br>10: with two measurements delay<br>11: with four measurements delay |

## System PMIC for Mobile and Automotive Applications

| Register Address | Bit | Type | Label     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------------------|-----|------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 5:4 | R/W  | MON_MODE  | Regulator monitor executes<br><b>00: Under-voltage/Over-voltage lockout with an E_REG_UVOV event (nIRQ assertion) and regulator shutdown from an output voltage being out of the selected range</b><br>01: Normal auto measurement with an E_REG_UVOV event (nIRQ assertion) from any finished auto measurement on A8, A9 and A10<br>10: Burst auto measurement with an E_REG_UVOV event (nIRQ assertion) generated after the time slot of A10 has been processed<br>11: reserved |
|                  | 3   | R/W  | MON_DEB   | 0: Regulator monitor (A8, 9, 10): debouncing off<br><b>1: Regulator monitor (A8, 9, 10): debouncing on</b>                                                                                                                                                                                                                                                                                                                                                                        |
|                  | 2   | R/W  | MON_RES   | Control requires M_REG_UVOV = 1:<br>1: Enables assertion of nRESET from out-of-range detection<br>Note: It is not recommended to assert this control inside OTP                                                                                                                                                                                                                                                                                                                   |
|                  | 1:0 | R/W  | MON_THRES | Regulator Monitor Threshold<br>00: Approx = 25 %<br>01: Approx = 12.5 %<br>10: Approx = 6.25 %<br>11: Approx = 3.125 %                                                                                                                                                                                                                                                                                                                                                            |

Table 243: MON\_REG\_2

| Register Address   | Bit | Type | Label       | Description                      |
|--------------------|-----|------|-------------|----------------------------------|
| 0x115<br>MON_REG_2 | 7   | R/W  | LDO8_MON_EN | Enable LDO8 regulator monitoring |
|                    | 6   | R/W  | LDO7_MON_EN | Enable LDO7 regulator monitoring |
|                    | 5   | R/W  | LDO6_MON_EN | Enable LDO6 regulator monitoring |
|                    | 4   | R/W  | LDO5_MON_EN | Enable LDO5 regulator monitoring |
|                    | 3   | R/W  | LDO4_MON_EN | Enable LDO4 regulator monitoring |
|                    | 2   | R/W  | LDO3_MON_EN | Enable LDO3 regulator monitoring |
|                    | 1   | R/W  | LDO2_MON_EN | Enable LDO2 regulator monitoring |
|                    | 0   | R/W  | LDO1_MON_EN | Enable LDO1 regulator monitoring |

Table 244: MON\_REG\_3

| Register Address   | Bit | Type | Label        | Description                       |
|--------------------|-----|------|--------------|-----------------------------------|
| 0x116<br>MON_REG_3 | 7:3 | R/W  | Reserved     |                                   |
|                    | 2   | R/W  | LDO11_MON_EN | Enable LDO11 regulator monitoring |
|                    | 1   | R/W  | LDO10_MON_EN | Enable LDO10 regulator monitoring |
|                    | 0   | R/W  | LDO9_MON_EN  | Enable LDO9 regulator monitoring  |

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Table 245: MON\_REG\_4

| Register Address   | Bit | Type | Label                | Description                           |
|--------------------|-----|------|----------------------|---------------------------------------|
| 0x117<br>MON_REG_4 | 7   | R/W  | <b>BPERI_MON_EN</b>  | Enable BUCKPERI regulator monitoring  |
|                    | 6   | R/W  | <b>BMEM_MON_EN</b>   | Enable BUCKMEM regulator monitoring   |
|                    | 5   | R/W  | <b>BIO_MON_EN</b>    | Enable BUCKIO regulator monitoring    |
|                    | 4   | R/W  | <b>BPRO_MON_EN</b>   | Enable BUCKPRO regulator monitoring   |
|                    | 3   | R/W  | <b>BCORE2_MON_EN</b> | Enable BUCKCORE2 regulator monitoring |
|                    | 2   | R/W  | <b>BCORE1_MON_EN</b> | Enable BUCKCORE1 regulator monitoring |
|                    | 1:0 | R/W  | <b>Reserved</b>      |                                       |

Table 246: MON\_REG\_5

| Register Address   | Bit | Type | Label      | Description                                                                                                                                                       |
|--------------------|-----|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x11E<br>MON_REG_5 | 7   | R    | Reserved   |                                                                                                                                                                   |
|                    | 6:4 | R/W  | MON_A9_IDX | Latest measurement at channel A9 was:<br>000: none<br>001: BUCKIO<br>010: BUCKMEM<br>011: BUCKPERI<br>100: LDO1<br>101: LDO2<br>101: LDO5<br>> 110: reserved      |
|                    | 3   | R/W  | Reserved   |                                                                                                                                                                   |
|                    | 2:0 | R/W  | MON_A8_IDX | Latest measurement at channel A8 was:<br>000: none<br>001: BUCKCORE1<br>010: BUCKCORE2<br>011: BUCKPRO<br>100: LDO3<br>101: LDO4<br>110: LDO11<br>> 110: reserved |

Table 247: MON\_REG\_6

| Register Address   | Bit | Type | Label       | Description                                                                                                                              |
|--------------------|-----|------|-------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 0x11F<br>MON_REG_6 | 7:3 | R/W  | Reserved    |                                                                                                                                          |
|                    | 2:0 | R/W  | MON_A10_IDX | Latest measurement at channel A10 was:<br>000: none<br>001: LDO6<br>010: LDO7<br>011: LDO8<br>100: LDO9<br>101: LDO10<br>> 101: reserved |

## System PMIC for Mobile and Automotive Applications

Table 248: TRIM\_CLDR

| Register Address   | Bit | Type | Label    | Description                                                                                                                                                                                                               |
|--------------------|-----|------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x120<br>TRIM_CLDR | 7:0 | R/W  | TRIM_32K | Bits for correction of the 32K oscillator frequency for internal calendar:<br>10000000: -244.1 ppm<br>...<br>11111111: -1.9 ppm<br><b>00000000: off</b><br>00000001: 1.9 ppm (1/(32768*16))<br>...<br>01111111: 242.2 ppm |

Table 249: GP\_ID\_0

| Register Address | Bit | Type                          | Label | Description                |
|------------------|-----|-------------------------------|-------|----------------------------|
| 0x121<br>GP_ID_0 | 7:0 | R/W<br><a href="#">Note 1</a> | GP_0  | Data from fuse array (OTP) |

**Note 1** Write access can be disabled by OTP if required.

Table 250: GP\_ID\_1

| Register Address | Bit | Type                          | Label | Description                |
|------------------|-----|-------------------------------|-------|----------------------------|
| 0x122<br>GP_ID_1 | 7:0 | R/W<br><a href="#">Note 1</a> | GP_1  | Data from fuse array (OTP) |

**Note 1** Write access can be disabled by OTP if required.

Table 251: GP\_ID\_2

| Register Address | Bit | Type                          | Label | Description                |
|------------------|-----|-------------------------------|-------|----------------------------|
| 0x123<br>GP_ID_2 | 7:0 | R/W<br><a href="#">Note 1</a> | GP_2  | Data from fuse array (OTP) |

**Note 1** Write access can be disabled by OTP if required.

Table 252: GP\_ID\_3

| Register Address | Bit | Type                          | Label | Description                |
|------------------|-----|-------------------------------|-------|----------------------------|
| 0x124<br>GP_ID_3 | 7:0 | R/W<br><a href="#">Note 1</a> | GP_3  | Data from fuse array (OTP) |

**Note 1** Write access can be disabled by OTP if required.

Table 253: GP\_ID\_4

| Register Address | Bit | Type                          | Label | Description                |
|------------------|-----|-------------------------------|-------|----------------------------|
| 0x125<br>GP_ID_4 | 7:0 | R/W<br><a href="#">Note 1</a> | GP_4  | Data from fuse array (OTP) |

**Note 1** Write access can be disabled by OTP if required.

Table 254: GP\_ID\_5

| Register Address | Bit | Type                          | Label | Description                |
|------------------|-----|-------------------------------|-------|----------------------------|
| 0x126<br>GP_ID_5 | 7:0 | R/W<br><a href="#">Note 1</a> | GP_5  | Data from fuse array (OTP) |

## System PMIC for Mobile and Automotive Applications

**Note 1** Write access can be disabled by OTP if required.

**Table 255: GP\_ID\_6**

| Register Address | Bit | Type                          | Label | Description                |
|------------------|-----|-------------------------------|-------|----------------------------|
| 0x127<br>GP_ID_6 | 7:0 | R/W<br><a href="#">Note 1</a> | GP_6  | Data from fuse array (OTP) |

**Note 1** Write access can be disabled by OTP if required.

**Table 256: GP\_ID\_7**

| Register Address | Bit | Type                          | Label | Description                |
|------------------|-----|-------------------------------|-------|----------------------------|
| 0x128<br>GP_ID_7 | 7:0 | R/W<br><a href="#">Note 1</a> | GP_7  | Data from fuse array (OTP) |

**Note 1** Write access can be disabled by OTP if required.

**Table 257: GP\_ID\_8**

| Register Address | Bit | Type                          | Label | Description                |
|------------------|-----|-------------------------------|-------|----------------------------|
| 0x129<br>GP_ID_8 | 7:0 | R/W<br><a href="#">Note 1</a> | GP_8  | Data from fuse array (OTP) |

**Note 1** Write access can be disabled by OTP if required.

**Table 258: GP\_ID\_9**

| Register Address | Bit | Type                          | Label | Description                |
|------------------|-----|-------------------------------|-------|----------------------------|
| 0x12A<br>GP_ID_9 | 7:0 | R/W<br><a href="#">Note 1</a> | GP_9  | Data from fuse array (OTP) |

**Note 1** Write access can be disabled by OTP if required.

**Table 259: GP\_ID\_10**

| Register Address  | Bit | Type | Label | Description                                                                    |
|-------------------|-----|------|-------|--------------------------------------------------------------------------------|
| 0x12B<br>GP_ID_10 | 7:0 | R/W  | GP_10 | Data from fuse array (OTP), no OTP reload after powering up from NO-POWER mode |

**Table 260: GP\_ID\_11**

| Register Address  | Bit | Type | Label | Description                |
|-------------------|-----|------|-------|----------------------------|
| 0x12C<br>GP_ID_11 | 7:0 | R/W  | GP_11 | Data from fuse array (OTP) |

**Table 261: Reserved**

| Register Address          | Bit | Type | Label    | Description |
|---------------------------|-----|------|----------|-------------|
| 0x12D – 0x134<br>Reserved | 7:0 | R    | Reserved | Reserved    |

**Table 262: Co-PMIC2**

| Register Address   | Bit | Type | Label    | Description          |
|--------------------|-----|------|----------|----------------------|
| 0x140<br>CoPMIC2_S | 7:0 | R    | Reserved | Reserved for Co-PMIC |

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| Register Address   | Bit | Type | Label    | Description          |
|--------------------|-----|------|----------|----------------------|
| 0x14F<br>CoPMIC2_E | 7:0 | R    | Reserved | Reserved for Co-PMIC |

Table 263: CHG\_Co2

| Register Address   | Bit | Type | Label    | Description                    |
|--------------------|-----|------|----------|--------------------------------|
| 0x150<br>CHG_Co_S2 | 7:0 | R    | Reserved | Reserved for companion charger |
| 0x17F<br>CHG_Co_E2 | 7:0 | R    | Reserved | Reserved for companion charger |

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Table 264: PAGE\_CON

| Register Address  | Bit | Type | Label      | Description                                 |
|-------------------|-----|------|------------|---------------------------------------------|
| 0x180<br>PAGE_CON | 7   | RW   | REVERT     | See register 0x00, <a href="#">Table 59</a> |
|                   | 6   | RW   | WRITE_MODE |                                             |
|                   | 5:3 | RW   | Reserved   |                                             |
|                   | 2:0 | RW   | REG_PAGE   |                                             |

Table 265: DEVICE\_ID

| Register Address   | Bit | Type | Label     | Description          |
|--------------------|-----|------|-----------|----------------------|
| 0x181<br>DEVICE_ID | 7:0 | R    | DEVICE_ID | Read back of chip ID |

Table 266: VARIANT\_ID

| Register Address    | Bit | Type | Label | Description                             |
|---------------------|-----|------|-------|-----------------------------------------|
| 0x182<br>VARIANT_ID | 7:4 | R    | MRC   | Read back of mask revision code (MRC)   |
|                     | 3:0 | R    | VRC   | Read back of package variant code (VRC) |

Table 267: CUSTOMER\_ID

| Register Address     | Bit | Type | Label       | Description                                                                           |
|----------------------|-----|------|-------------|---------------------------------------------------------------------------------------|
| 0x183<br>CUSTOMER_ID | 7:0 | R    | CUSTOMER_ID | ID for customer and target application platform, written during production of variant |

Table 268: CONFIG\_ID

| Register Address   | Bit | Type | Label      | Description                                                                                                                                                    |
|--------------------|-----|------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x184<br>CONFIG_ID | 7:0 | R    | CONFIG_REV | ID for revision of OTP settings, written during production of variant<br>00000000 – OTP unprogrammed (RESERVED)<br>> 00000000 – OTP configuration revision xxx |

## System PMIC for Mobile and Automotive Applications

**Table 269: PMIC\_STATUS**

| Register Address     | Bit | Type | Label           | Description                                                                                                            |
|----------------------|-----|------|-----------------|------------------------------------------------------------------------------------------------------------------------|
| 0x1A8<br>PMIC_STATUS | 7   | R    | <b>PC_DONE</b>  | Power Commander download complete                                                                                      |
|                      | 6:5 | R/W  | <b>Reserved</b> |                                                                                                                        |
|                      | 4:0 | R    | <b>STATUS</b>   | Decimal Decode:<br>03 = RESET (Shutdown)<br>28 = SYSTEM<br>25 = POWER<br>23 = POWER-DOWN<br>20 = POWER1<br>17 = ACTIVE |

## System PMIC for Mobile and Automotive Applications

### Status Definitions

| Revision | Datasheet Status | Product Status | Definition                                                                                                                                                                                                                                                                                                                                                                                           |
|----------|------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.<n>    | Target           | Development    | This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.                                                                                                                                                                                                                                                               |
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