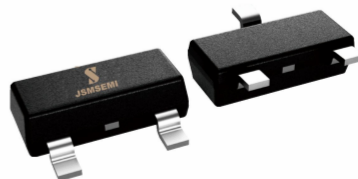


DESCRIPTION

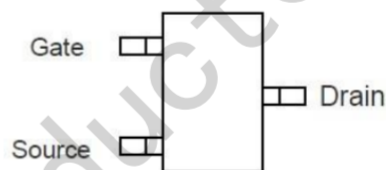
The JSM2305 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package.

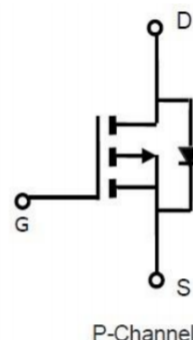


FEATURE

- ◆ -20V/-4.3A, $R_{DS(ON)}=30m\Omega$ (typ.)@ $V_{GS}=-4.5V$
- ◆ -20V/-3.5A, $R_{DS(ON)}=40m\Omega$ (typ.)@ $V_{GS}=-2.5V$
- ◆ -20V/-2.0A, $R_{DS(ON)}=56m\Omega$ (typ.)@ $V_{GS}=-1.8V$
- ◆ -20V/-1.0A, $R_{DS(ON)}=85m\Omega$ (typ.)@ $V_{GS}=-1.5V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOT23-3 package design



TOP VIEW
SOT-23



APPLICATIONS

- ◆ Power Management
- ◆ Portable Equipment
- ◆ DC/DC Converter
- ◆ Load Switch
- ◆ DSC
- ◆ LCD Display inverter

ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}C$ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V _{DSS}	Drain-Source Voltage		-20	V
V _{GSS}	Gate-Source Voltage		±10	V
I _D	Continuous Drain Current (T _C =25℃)	V _{GS} =-10V	-4.2	A
	Continuous Drain Current (T _C =70℃)		-3.5	A
I _{DM}	Pulsed Drain Current		-20	A
P _D	Power Dissipation	T _A =25℃	1.5	W
		T _A =70℃	0.9	
T _J	Operation Junction Temperature		150	℃
T _{STG}	Storage Temperature Range		-55~+150	℃
R _{θJA}	Thermal Resistance Junction to Ambient		120	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

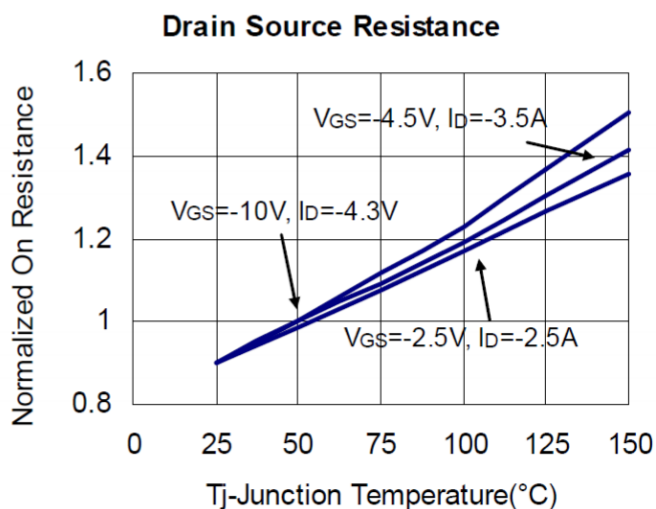
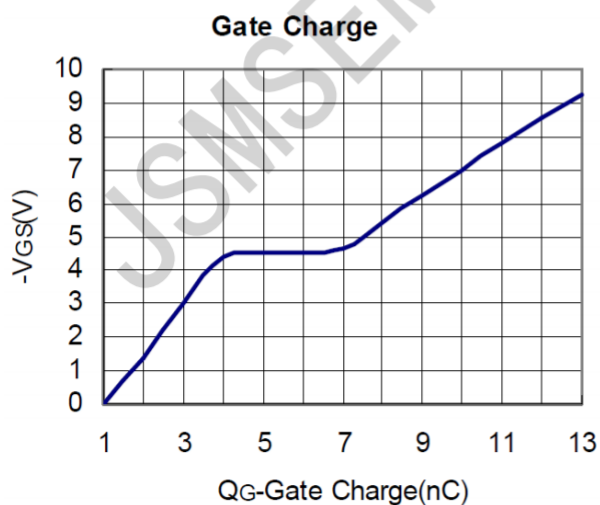
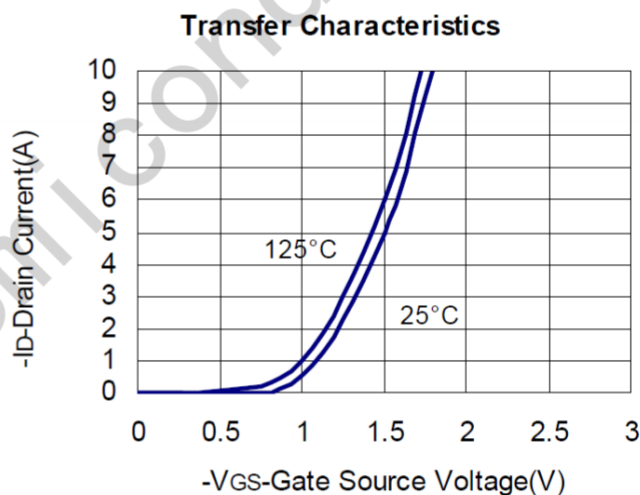
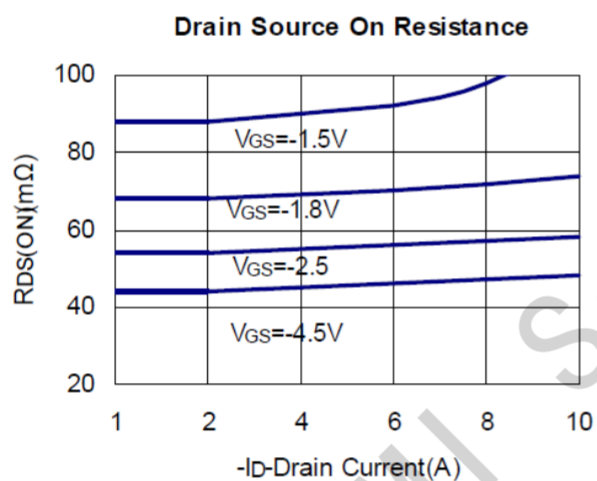
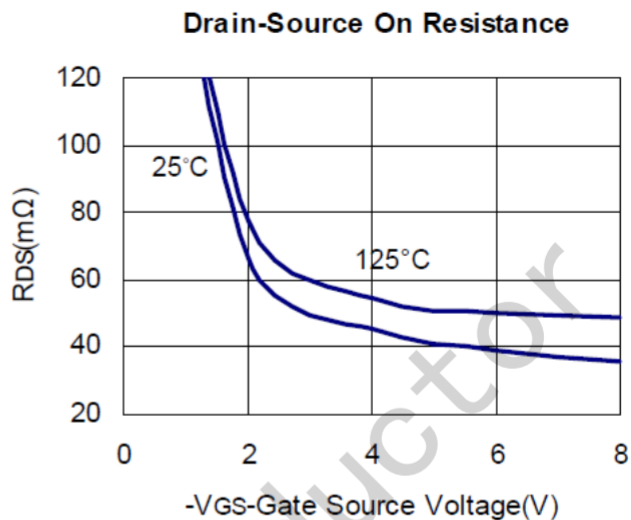
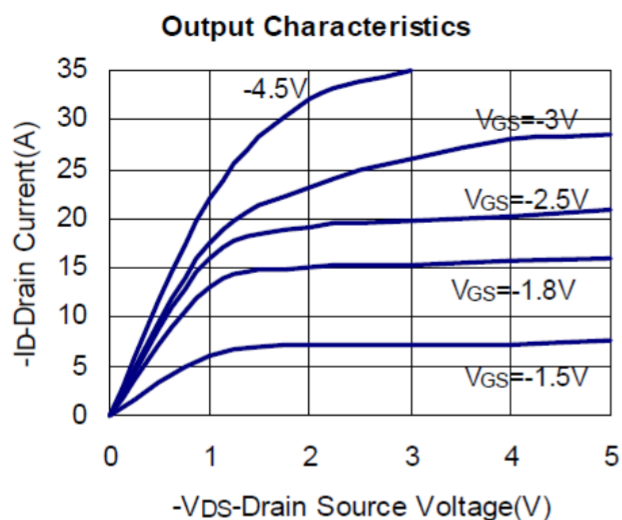
ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

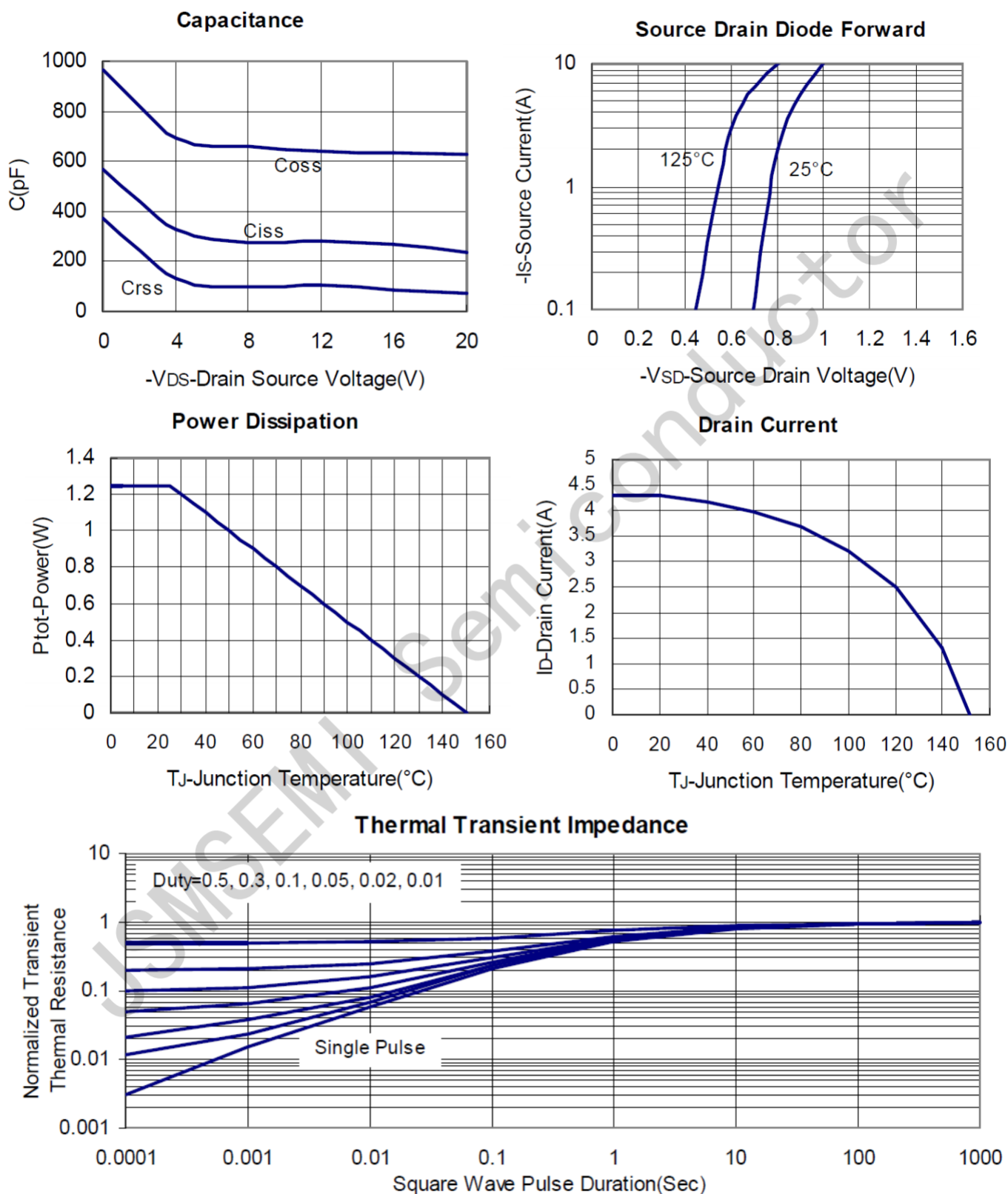
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-0.3		-1.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±10V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-20V, V _{GS} =0			-1	uA
		V _{DS} =-20V, V _{GS} =0 T _J =55°C			-5	
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-4.0A		30	40	mΩ
		V _{GS} =-2.5V, I _D =-4.0A		40	60	
		V _{GS} =-1.8V, I _D =-2.0A		56	78	
		V _{GS} =-1.5V, I _D =-1.0A		85	110	
Gfs	Forward Transconductance	V _{DS} =-5V, I _D =-4.0A		22		S
Source-Drain Diode						
V _{SD}	Diode Forward Voltage	I _S =-1.0A, V _{GS} =0V		-0.67	-1.2	V
Dynamic Parameters						
Q _g	Total Gate Charge	V _{DS} =-10V V _{GS} =-4.5V I _D =-4.0A		11.1		nC
Q _{gs}	Gate-Source Charge			3.1		
Q _{gd}	Gate-Drain Charge			2.4		
C _{iss}	Input Capacitance	V _{DS} =-10V		989		pF
C _{oss}	Output Capacitance	V _{GS} =0V		167		
C _{rss}	Reverse Transfer Capacitance	f=1MHz		75.5		
T _{d(on)}	Turn-On Time	V _{DS} =-10V I _D =-3.7A V _{GEN} =-4.5V R _G =1Ω		712		nS
T _r				1386		
T _{d(off)}	Turn-Off Time			9.1		
T _f				4		

Note: 1. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

2. Static parameters are based on package level with recommended wire bonding

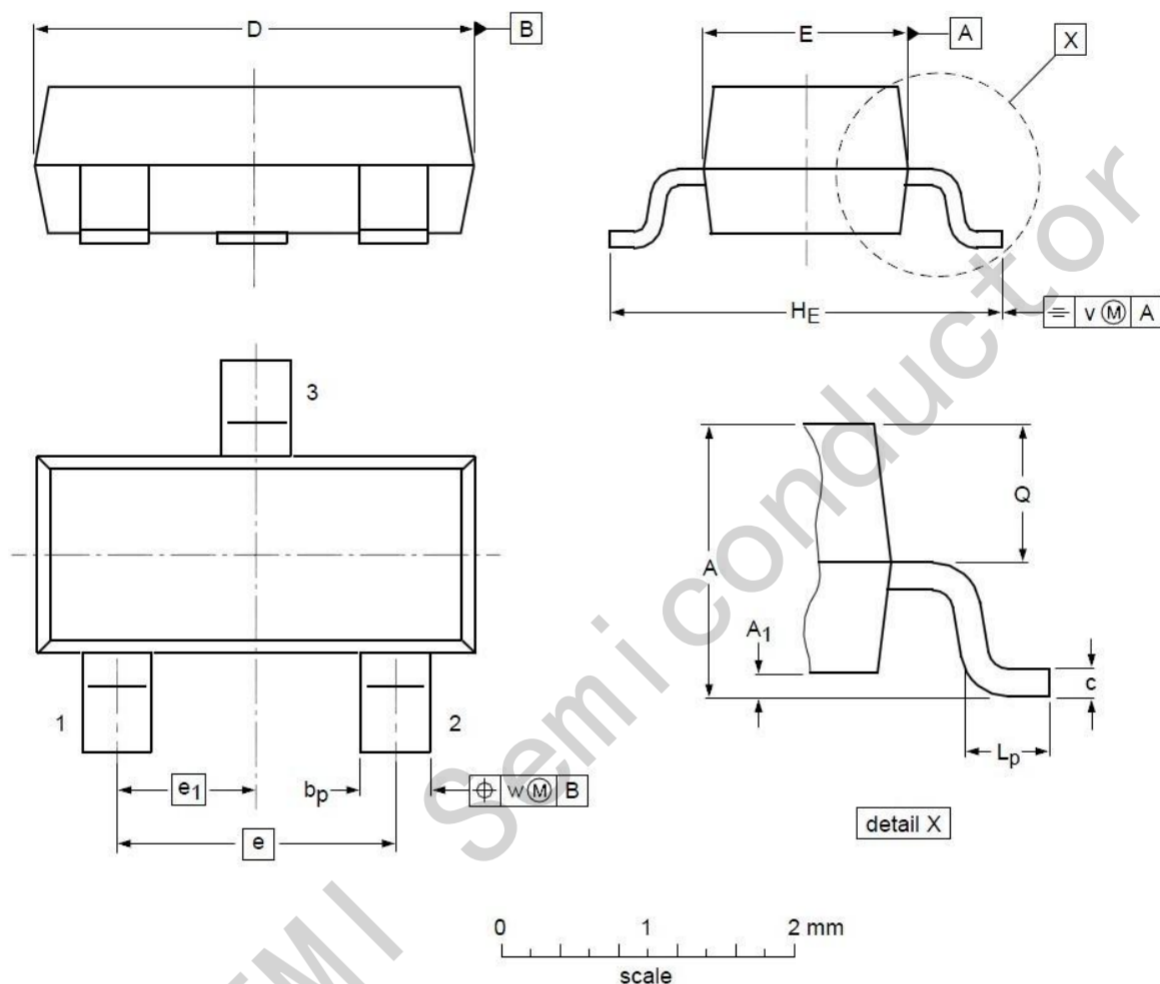
TYPICAL CHARACTERISTICS (25°C Unless Note)



TYPICAL CHARACTERISTICS (continuous)


Package Information

SOT-23-3



DIMENSIONS (unit : mm)

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.90	1.01	1.15	A ₁	0.01	0.05	0.10
b _p	0.30	0.42	0.50	c	0.08	0.13	0.15
D	2.80	2.92	3.00	E	1.20	1.33	1.40
e	--	1.90	--	e ₁	--	0.95	--
H _E	2.25	2.40	2.55	L _p	0.30	0.42	0.50
Q	0.45	0.49	0.55	v	--	0.20	--
w	--	0.10	--				