

## High Performance PDM Stereo Audio ADC

### FEATURES

- High performance advanced delta-sigma audio ADC
- 90 dB dynamic range at 26 dB PGA
- -85 dB THD+N
- Low noise PGA
- 8 to 96 kHz sampling frequency
- Low power

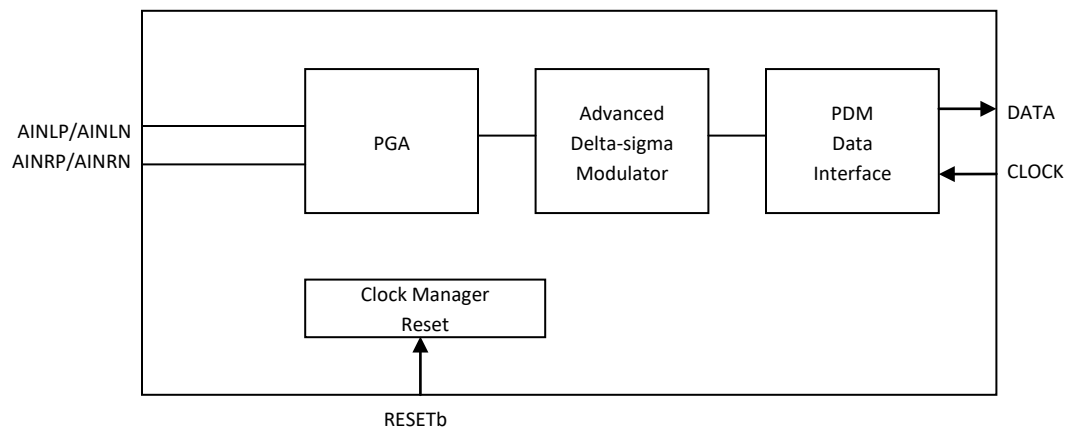
### APPLICATIONS

- Mic Array
- Soundbar
- Audio Interface
- Digital TV
- A/V Receiver
- DVR
- NVR

### ORDERING INFORMATION

ES7201 -40°C ~ +85°C  
QFN-12

### BLOCK DIAGRAM



1. PIN OUT AND DESCRIPTION ..... 3

2. TYPICAL APPLICATION CIRCUIT..... 4

3. ELECTRICAL CHARACTERISTICS ..... 4

    ABSOLUTE MAXIMUM RATINGS..... 4

    RECOMMENDED OPERATING CONDITIONS ..... 4

    ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS ..... 5

    DC CHARACTERISTICS ..... 5

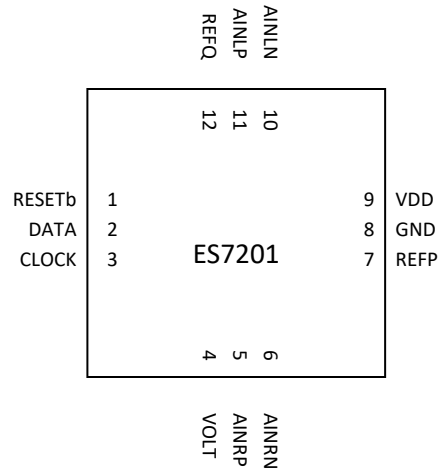
    PDM DATA SWITCHING SPECIFICATIONS ..... 5

4. PACKAGE..... 6

5. CORPORATE INFORMATION ..... 7

6. IMPORTANT NOTICE AND DISCLAIMER..... 7

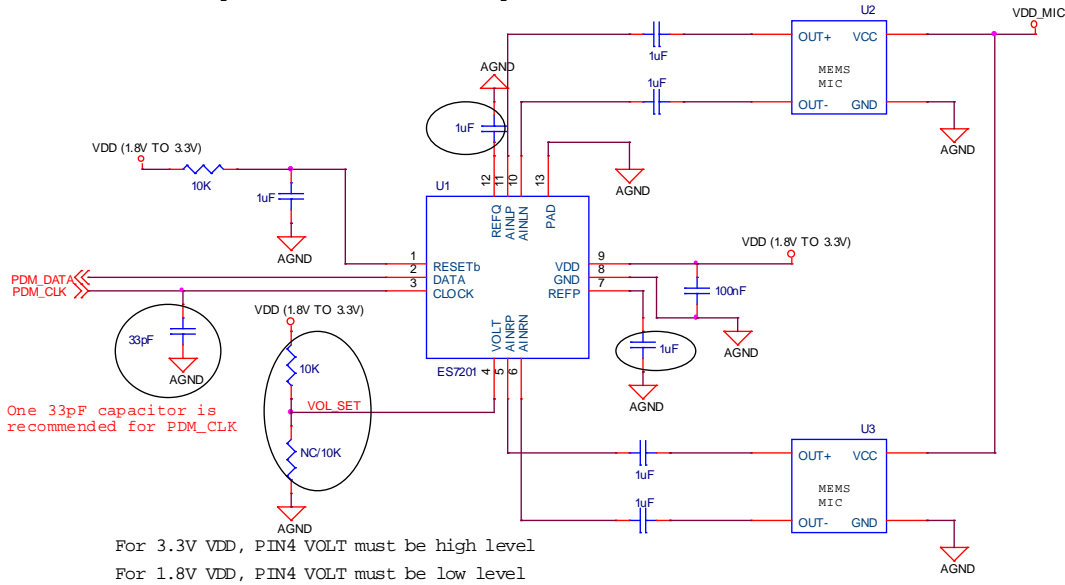
## 1. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
DATA, CLOCK	2, 3	O, I	PDM clock and data
RESETb	1	I	Active low reset
VOLT	4	I	High: VDD = 3.3V Low: VDD = 1.8V
AINLP, AINLN	11,10	I	Analog left inputs
AINRP, AINRN	5, 6	I	Analog right inputs
VDD, GND	9, 8	I	Power supply
REFP	7	O	Filtering capacitor connection
REFQ	12	O	Filtering capacitor connection

## 2. TYPICAL APPLICATION CIRCUIT

The filter capacitors on REFP and REFQ pins must be located as close to ES7201 package as possible. 4.7uF or 10uF capacitor is for better audio performance.



## 3. ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	GND-0.3V	VDD+0.3V
Digital Input Voltage Range	GND-0.3V	VDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDD	1.7	1.8/3.3	3.6	V

**ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS**

Test conditions are as the following unless otherwise specify: VDD=3.3V, GND=0V, ambient temperature=25°C, CLOCK=6.144 MHz.

PARAMETER	MIN	TYP	MAX	UNIT
<b>ADC Performance</b>				
Dynamic Range (A-weight, 26 dB PGA)	87	90	93	dB
THD+N (26 dB PGA)	-88	-85	-82	dB
Channel Separation (1KHz)	97	100	103	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
<b>Analog Input</b>				
Full Scale Input Level		±0.0708*VDD/3.3		Vrms
Input Impedance		9.6 (23 dB PGA)		KΩ

**DC CHARACTERISTICS**

PARAMETER	MIN	TYP	MAX	UNIT
<b>Normal Operation Mode</b>				
VDD=3.3V (16 kHz)		22		mW
VDD=1.8V (16 kHz)		4.6		
Power Down Mode		0		uA
<b>Digital Voltage Level</b>				
Input High-level Voltage	0.7*VDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		VDD		V
Output Low-level Voltage		0		V

**PDM DATA SWITCHING SPECIFICATIONS**

PARAMETER		Symbol	MIN	MAX	UNIT
CLOCK frequency			0.512	6.144	MHz
CLOCK duty cycle	≤ 3.072 MHz		40	60	%
			45	55	
DATA valid	VDDD=3.3V VDDD=1.8V	T <sub>VALID</sub>	11 19	27 61	ns
DATA hold	VDDD=3.3V VDDD=1.8V	T <sub>HOLD</sub>	10 18	26 56	ns

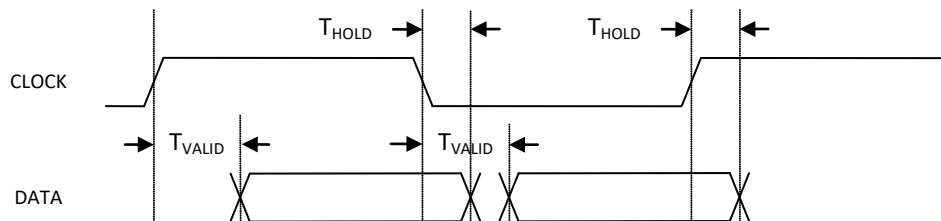
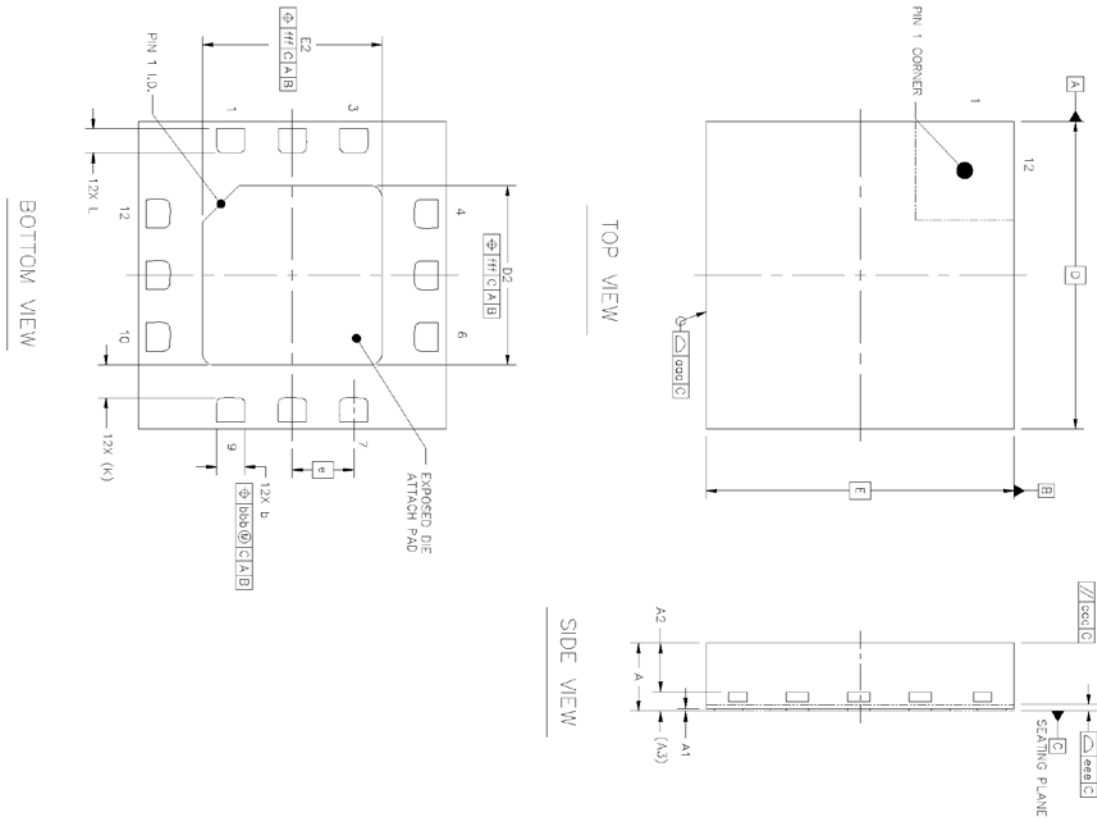


Figure 1 PDM Data Timing

4. PACKAGE (UNIT: MM)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.4	---
L/F THICKNESS	A3		0.152 REF	
LEAD WIDTH	b	0.18	0.23	0.28
BODY SIZE	X		2.5 BSC	
	Y		2.5 BSC	
LEAD PITCH	X		0.5 BSC	
	Y		0.5 BSC	
EP SIZE	X	1.36	1.46	1.56
	E2	1.36	1.46	1.56
LEAD LENGTH	L	0.1425	0.1925	0.2425
	K		0.265 REF	
LEAD TIP TO EXPOSED PAD EDGE	ccc		0.1	
PACKAGE EDGE TOLERANCE	eee		0.1	
MOLD FLATNESS	fff		0.05	
COP PLANARITY	bbb		0.1	
LEAD OFFSET	fff		0.1	
EXPOSED PAD OFFSET				

NOTES  
 1:REFER TO JEDEC MO-220;  
 2:COP PLANARITY APPLIES TO LEADS, CORNER LE

## 5. CORPORATE INFORMATION

Everest Semiconductor Co., Ltd.

No. 1355 Jinjihu Drive, Suzhou Industrial Park, Jiangsu, P.R. China, Zip Code 215021

苏州工业园区金鸡湖大道 1355 号国际科技园, 邮编 215021

Email: [info@everest-semi.com](mailto:info@everest-semi.com)



## 6. IMPORTANT NOTICE AND DISCLAIMER

Everest Semiconductor publishes reliable technical information about its products. Information contained herein is subject to change without notice. It may be used by a party at their own discretion and risk. Everest Semiconductor disclaims responsibility for any claims, damages, costs, losses, and liabilities arising out of your use of the information. This publication is not to be taken as a license to operate under any existing patents and intellectual properties.