Click here to ask an associate for production status of specific part numbers.

Field-Side Self-Powered, 4-Channel, 12-bit, Isolated ADC

MAX22530–MAX22532

General Description

The MAX22530–MAX22532 are galvanically isolated, 4-channel, multiplexed, 12-bit, analog-to-digital converters (ADC) in the MAXSafe™ family product line. An integrated, isolated, DC-DC converter powers all field-side circuitry, and this allows field-side diagnostics even when no input signal is present.

The MAX22530–MAX22532 family continually digitizes the input voltage on the field-side of an isolation barrier and transmits the data across the isolation barrier to the logic-side of the devices where the magnitude of the input voltage is compared to programmable thresholds. The 12-bit ADC core has a sample rate of 20ksps (typ) per-channel. ADC data is available through the SPI interface either directly or filtered. Filtering averages the most recent 4 readings depending on the setting.

Each input has a comparator with programmable high and low thresholds, and an interrupt is asserted when any input crosses its programmed level based on the mode setting. The comparator output pin (COUT_) is high when the input voltage is above the upper threshold and low when it is below the lower threshold in digital input mode. Typical response time of the comparator to an input change is less than 75µs with filtering disabled. With filtering enabled, the comparator uses the moving average of the last 4 ADC readings.

The MAX22530 in a 16-pin wide SOIC package provides 8mm of creepage and clearance, and 5kVRMS isolation. The MAX22531 in a 20-pin SSOP package and the MAX22532 in a 28-pin SSOP package, both provide 5.5mm of creepage and clearance, and 3.5kVRMS isolation. All package material has a minimum comparative tracking index (CTI) of 400, which gives it a group II rating in creepage tables.

All devices are rated for operation at ambient temperatures between -40°C to +125°C.

Applications

- High-Voltage Binary Input
- Substation Automation
- Distribution Automation
- Process Automation
- Motion Control

Benefits and Features

- Enable Robust Detection of Multichannel Analog/Binary Inputs
- Withstands 3.5kV_{RMS} Isolation for 60s (V_{ISO}) for the SSOP Package
- Withstands 5kV_{RMS} Isolation for 60s (V_{ISO}) for the Wide SOIC Package
- 5.5mm of Creepage and Clearance for 20-pin or 28-pin SSOP Package
- 8mm of Creepage and Clearance for 16-pin Wide SOIC Package
- Group II CTI Package Material
- Reduces BOM and Board Space Through High Integration
- Field-Side Self-Powered with Integrated DC-DC Supply
- 12-bit, 20ksps Per-Channel ADC
- Programmable Threshold Comparators for each Channel
- Isolation for both Data and DC-DC Supply
- Integrated 1.8V Reference
- Increase System “Up Time” and Simplifies System Design & Maintenance
  - Field-Side ADC Functionality Diagnostics
  - Field-Side Continuous Power Monitoring
  - Communication System Self-Diagnostics
- Flexible Control and Interface
  - Programmable Upper and Lower Input Threshold Enable Programmable Hysteresis
  - Comparator Output (COUT_) Pins for Fastest Response
  - SPI Interface with CRC Option
  - Precision Internal Reference ±1% (typ)
  - -40°C to +125°C Operating Temperature Range

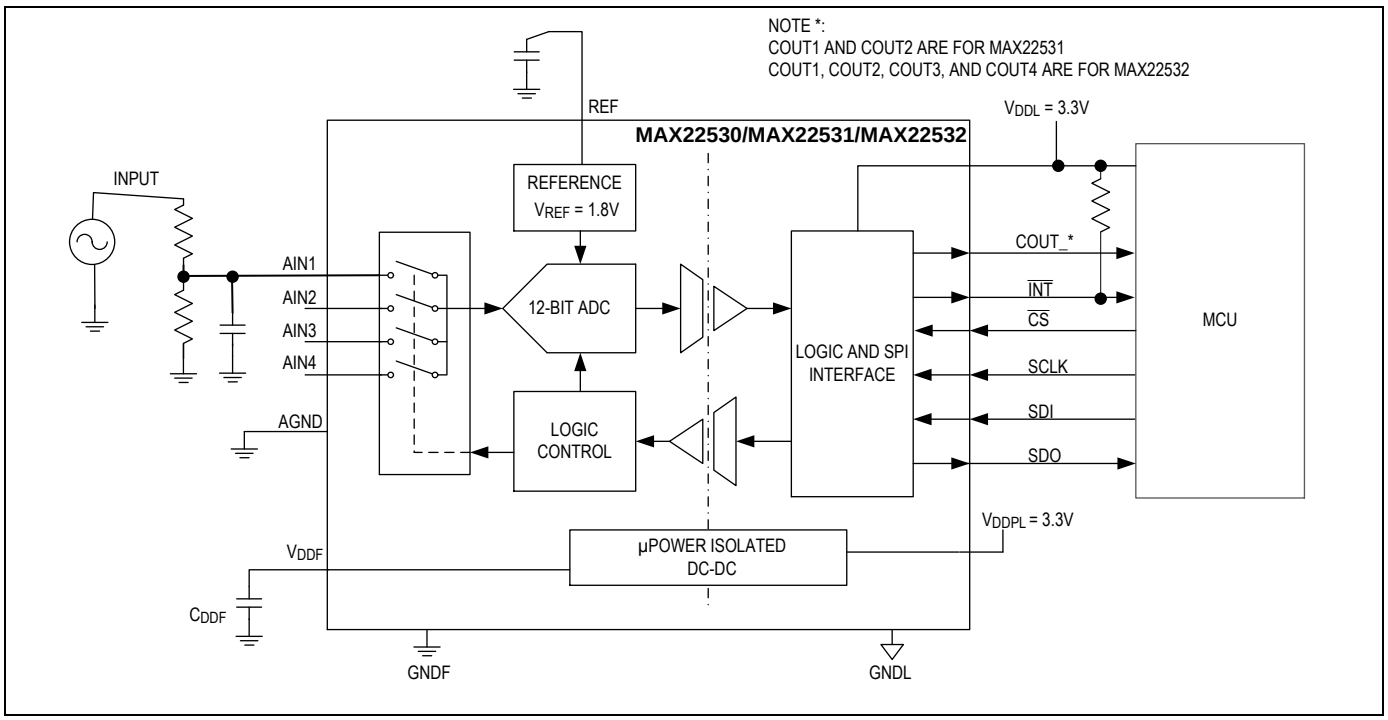
Safety Regulatory Approvals

- UL According to UL1577
- cUL According to CSA Bulletin 5A

***Ordering Information* appears at the end of the data sheet.**

19-100989; Rev 1; 9/21

Four-Channel Isolated ADC



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Absolute Maximum Ratings

V_{DDL} to GNDL.....-0.3V to 6V

V_{DDPL} to GNDL.....-0.3V to 6V

SDI, CS, INT (To GNDL).....-0.3V to 6V

SDO, COUT_ (To GNDL).....-0.3V to (V_{DDL} + 0.3V)

V_{DDF} to GNDF.....-0.3V to 6V

REF, AIN_ to AGND.....-0.3V to 2V

AGND to GNDF.....-0.3V to 0.3V

Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 14.1mW/°C above +70°C. 16-pin Wide SOIC) 1127mW

Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 11.9mW/°C above +70°C. 20-pin SSOP) 964mW

Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 6.96mW/°C above +70°C. 28-pin SSOP) 556.72mW

Operating Temperature Range .....-40°C to +125°C

Maximum Junction Temperature.....+150°C

Storage Temperature Range.....-65°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 W SOIC

Package Code	W16MS+14
Outline Number	*21-0042*
Land Pattern Number	*90-0107*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	68.8°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	41.6°C/W

20 SSOP

Package Code	A20MS+7
Outline Number	*21-0056*
Land Pattern Number	*90-0094*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	216°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	49°C/W

28 SSOP

Package Code	A28MS+5
Outline Number	*21-0056*
Land Pattern Number	*90-0095*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	143.70°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	47.90°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DDL} - V_{GNDL} = 1.71V to 5.5V, V_{DDPL} - V_{GNDL} = 3.0V to 5.5V, C_{DDF} = 1µF, C_{REF} = 1µF. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.) (*Note 1* *Note 2*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC-SIDE POWER SUPPLY						
Logic Power Supply	V_{DDL}		1.71		5.5	V
Logic Supply Current	I_{DDL}			1	2.5	mA
Logic-Supply UVLO Threshold	V_{DDL_UVLO}		1.5	1.6	1.66	V
Logic-Supply UVLO Hysteresis	V_{DDL_UHYS}			50		mV
Logic Power-Up Time	t_{LPU}	Valid SPI access		0.6	1	ms
Isolated DC-DC Supply	V_{DDPL}		3.0	3.3	5.5	V
Isolated DC-DC Supply Current	I_{DDPL}	V_{DDPL} = 3.3V		7	10	mA
Isolated DC-DC Supply UVLO Threshold	V_{DDPL_UVLO}		2.7	2.8	2.95	V
Isolated DC-DC Supply UVLO Hysteresis	V_{DDPL_UHYS}			100		mV
FIELD-SIDE PARAMETERS						
V_{DDF} Supply Voltage	V_{DDF}	Internally generated	2.7	3.1	5.5	V
Isolated DC-DC Power Up Time	t_{PWRUP}	C_{DDF} = 1 µF			10	ms
ADC AND COMPARATOR						
Input-Voltage Range	V_{AIN}		0		1.8	V
ADC Resolution			12			Bits
Gain Error	GE	V_{AIN} = 98% V_{REF}, excluding offset error and reference error	-0.2		+0.2	%FS
Offset Error	OE	V_{AIN} = 2% V_{REF}, offset calculated	-0.1		+0.1	%FS
Differential Nonlinearity	DNL				±1.5	LSB
Integral Nonlinearity	INL	Included in the gain and offset window			±2.0	LSB
Input-Leakage Current	IN_{LKG}		-600		+600	nA
Throughput per Channel			18	20	22	ksps
Latency (No filtering)		AIN# step input to COUT transition (*Note 3*)		75		µs
Latency (4 Readings)		AIN# step input to COUT transition (*Note 3*)		300		µs
CMTI		(*Note 4*)		50		kV/µs
INTERNAL VOLTAGE REFERENCE						
Nominal Output Voltage	V_{REF}	T_A = +25°C	1.78	1.80	1.82	V
Output-Voltage Accuracy	V_{REF_TOL}	T_A = -25°C to +85°C	-1.5		+1.5	%
		T_A = -40°C to +125°C	-2		+2	
Output-Voltage Temperature Drift	T_{CVOUT}			50		ppm/°C
LOGIC INTERFACE (SCLK, SDI, SDO, CS**, COUT,** INT**)**						
Input Logic-High Voltage	V_{IH}	SCLK, SDI, CS	0.7 x V_{DDL}			V

(V_{DDL} - V_{GNDL} = 1.71V to 5.5V, V_{DDPL} - V_{GNDL} = 3.0V to 5.5V, C_{DDF} = 1µF, C_{REF} = 1µF. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.) (*Note 1* *Note 2*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Logic-Low Voltage	V_{IL}	SCLK, SDI, CS			0.3 x V_{DDL}	V
Input Hysteresis	V_{HYST}	SCLK, SDI, CS		50		mV
Input Leakage Current	I_{IN_LKG}	SCLK, SDI, CS	-1		+1	µA
Input Capacitance	C_{IN}	SCLK, SDI, CS, f = 1MHz		2		pF
Output Logic-High Voltage	V_{OH}	SDO, COUT, sourcing 4mA	V_{DDL}- 0.4			V
Output Logic-Low Voltage	V_{OL}	SDO, COUT, INT, sinking 4mA			0.4	V
Output High-Impedance Leakage Current	I_{OLKG}	INT, SDO	-1		+1	µA
SPI TIMING CHARACTERISTICS						
SCLK Clock Frequency	f_{SCLK}				10	MHz
SCLK Clock Period	t_{SCLK}		100			ns
SCLK Pulse-Width High	t_{SCLKH}		40			ns
SCLK Pulse-Width Low	t_{SCLKL}		40			ns
CS Fall-to-SCLK Rise Time	$t_{CS(LEAD)}$		20			ns
SCLK Fall-to-CS Rise Time	$t_{CS(LAQ)}$		80			ns
SDI Hold Time	t_{DINH}		20			ns
SDI Setup Time	t_{DINSU}		20			ns
SDO Disable Time (CS Rising to SDO Three-State)	$t_{DOUT(DIS)}$		40			ns
Output Data Propagation Delay	t_{DO}				50	ns
Inter-Access Gap	t_{IAG}		920			ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications for all temperature limits are guaranteed by design.

Note 2: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to their respective ground (GNDL or GNDF), unless otherwise noted.

Note 3: Latency numbers are based on the following condition: a full-scale step is applied at the ADC input and COUTHI_ (register address 0x9 to 0xC) upper threshold (THU) is set to maximum value (0xFFFh). Latency is the delay from the step at the ADC input to the digital comparator output.

Note 4: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDF and GNDL (V_{CM} = 1000V).

Timing Diagram

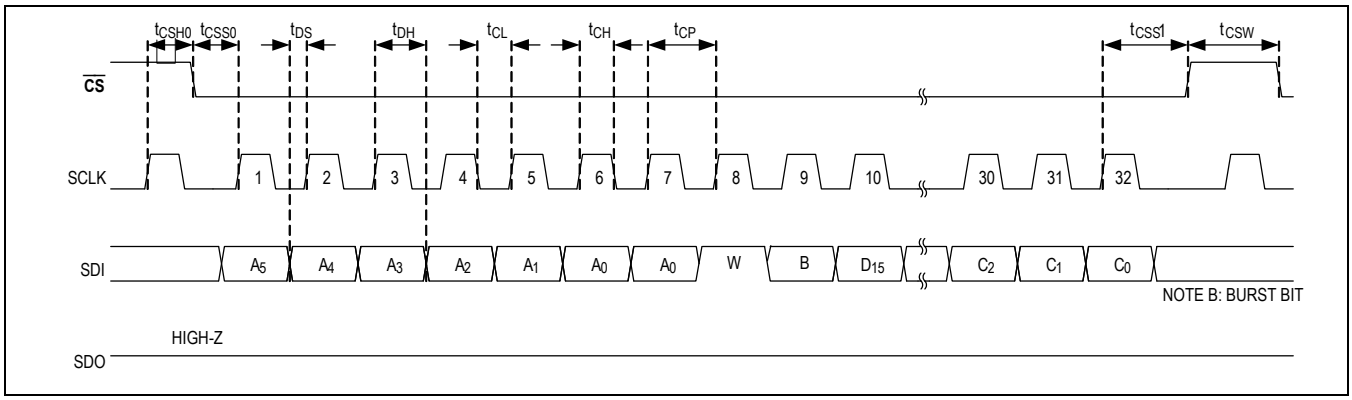


Figure 1. SPI Write Timing Diagram (with CRC Enabled)

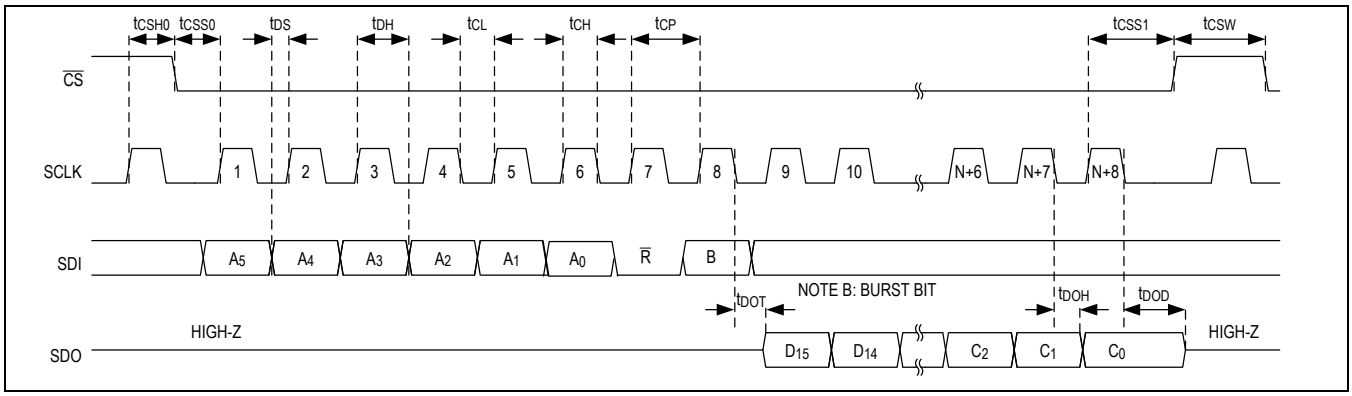


Figure 2. SPI Read Timing Diagram (with CRC Enabled)

Insulation Characteristics

16-pin Wide SOIC

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	2250	V_P
Maximum Repetitive-Peak-Isolation Voltage	V_{IORM}	(*Note 5*)	1200	V_P
Maximum Working-Isolation Voltage	V_{IOWM}	Continuous RMS voltage (*Note 5*)	848	V_{RMS}
Maximum Transient-Isolation Voltage	V_{IOTM}	(*Note 5*)	7000	V_P
Maximum Withstanding-Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (*Note 5*, *Note 6*)	5000	V_{RMS}
Maximum Surge-Isolation Voltage	V_{IOSM}	Basic Insulation, 1.2/50µs pulse per IEC61000-4-5	10000	V_P
Insulation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V, T_S = 150°C	> 10^9	
Barrier Capacitance Field Side-to-Logic Side	C_{IO}	f_{SW} = 1MHz (*Note 7*)	2	pF
Minimum Creepage Distance	CPG		8	mm
Minimum Clearance Distance	CLR		8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	> 400	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

20-pin and 28-pin SSOP

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	1182	V_P
Maximum Repetitive-Peak-Isolation Voltage	V_{IORM}	(*Note 5*)	630	V_P
Maximum Working-Isolation Voltage	V_{IOWM}	Continuous RMS voltage (*Note 5*)	445	V_{RMS}
Maximum Transient-Isolation Voltage	V_{IOTM}	(*Note 5*)	5300	V_P
Maximum Withstanding-Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (*Note 5*, *Note 6*)	3750	V_{RMS}
Maximum Surge-Isolation Voltage	V_{IOSM}	Basic Insulation, 1.2/50µs pulse per IEC61000-4-5	10000	V_P
Insulation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V, T_S = 150°C	> 10^9	
Barrier Capacitance Field Side-to-Logic Side	C_{IO}	f_{SW} = 1MHz (*Note 7*)	2	pF
Minimum Creepage Distance	CPG		5.5	mm
Minimum Clearance Distance	CLR		5.5	mm

Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	> 400	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 5: V_{ISO}, V_{IOWM}, and V_{IORM} are defined by the IEC 60747-5-5 standard.

Note 6: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.

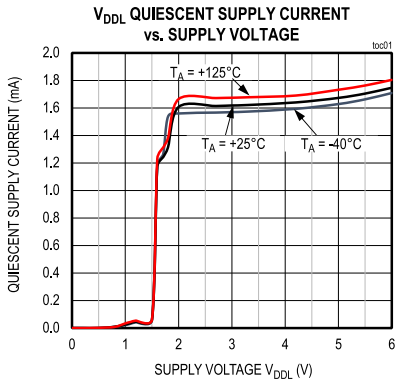
Note 7: Capacitance is measured with all pins on field-side and logic-side tied together.

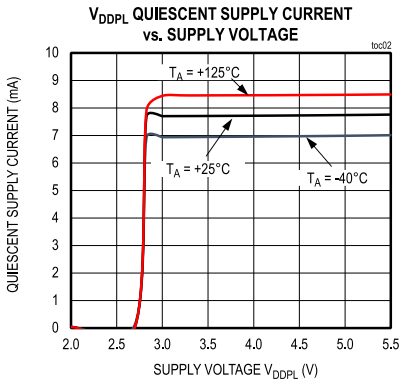
ESD and Transient Immunity Characteristics

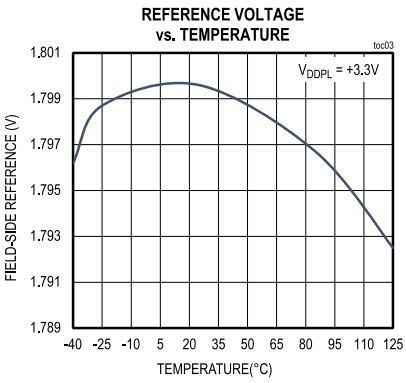
PARAMETER	SYMBOL	CONDITIONS	VALUE (TYP)	UNITS
Surge	AIN_ to GNDF	≥ 60kΩ input resistor, IEC 61000-4-5 1.2µs/50µs pulse	±7.2	kV
	AIN_ to AIN_	≥ 60kΩ input resistors, IEC 61000-4-5 1.2µs/50µs pulse	±4	
EFT	AIN_ to GNDF	Capacitive clamp to input cable pair (AIN_- GNDF) with 60kΩ input divider resistor connected AIN_- GNDF, 1nF Y-CAP to earth, IEC61000-4-4	±4	kV
ESD	AIN_ Contact	≥ 60kΩ resistor in series with AIN_ with respect to GNDF, IEC 61000-4-2	±8	kV
	AIN_ Air Gap	≥ 60kΩ resistor in series with AIN_ with respect to GNDF, IEC 61000-4-2	±15	
	Any pin to Any pin	Human Body Model	±3	

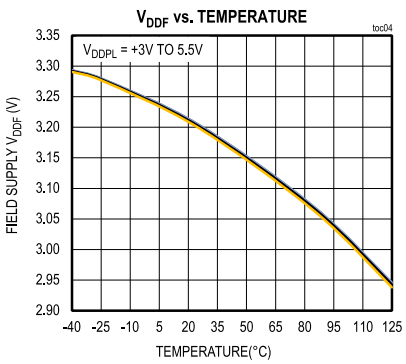
Typical Operating Characteristics

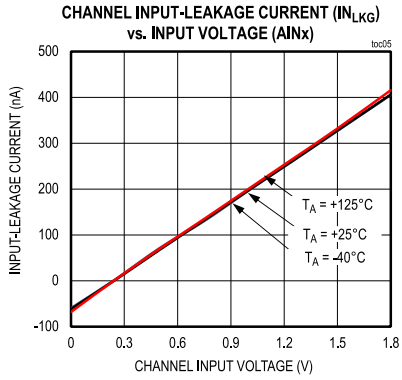
(V_{DDL} - V_{GNDL} = 3.3V, V_{DDPL} - V_{GNDL} = 3.3V, C_{DDF} = 1µF, C_{REF} = 1µF, T_A = +25°C, unless otherwise noted.)

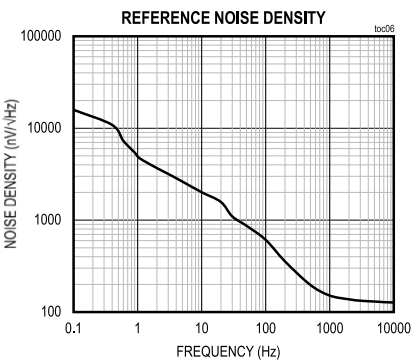


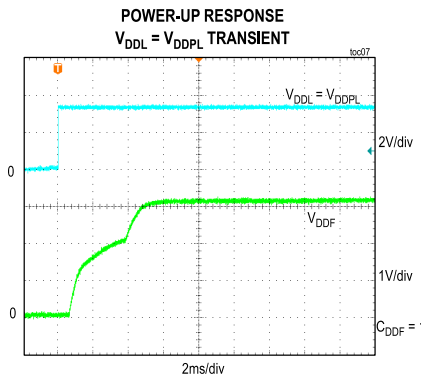


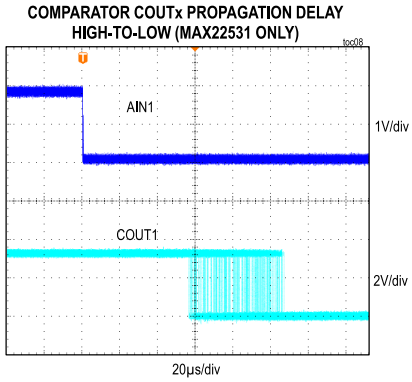


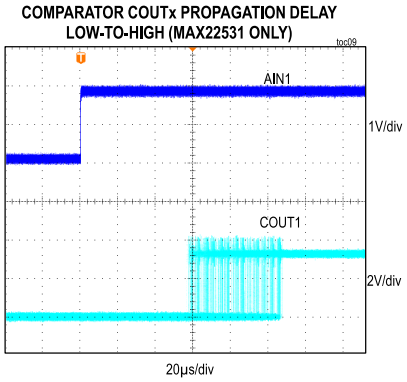






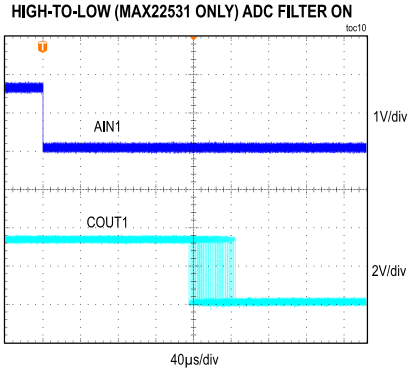




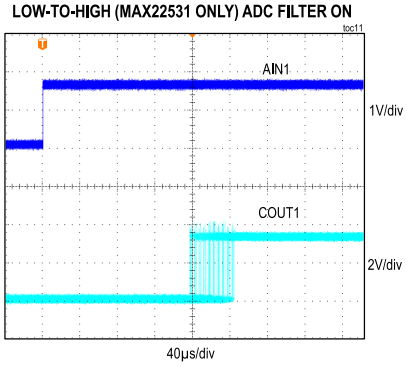


(V_{DDL} - V_{GNDL} = 3.3V, V_{DDPL} - V_{GNDL} = 3.3V, C_{DDF} = 1µF, C_{REF} = 1µF, T_A = +25°C, unless otherwise noted.)

COMPARATOR COUTx PROPAGATION DELAY
HIGH-TO-LOW (MAX22531 ONLY) ADC FILTER ON

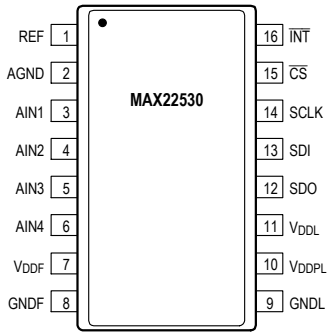


COMPARATOR COUTx PROPAGATION DELAY
LOW-TO-HIGH (MAX22531 ONLY) ADC FILTER ON



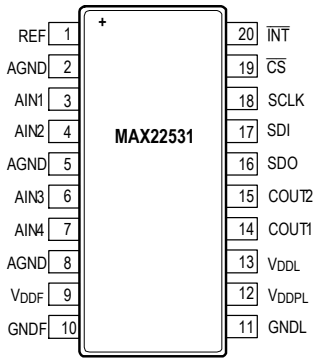
Pin Configurations

TOP VIEW

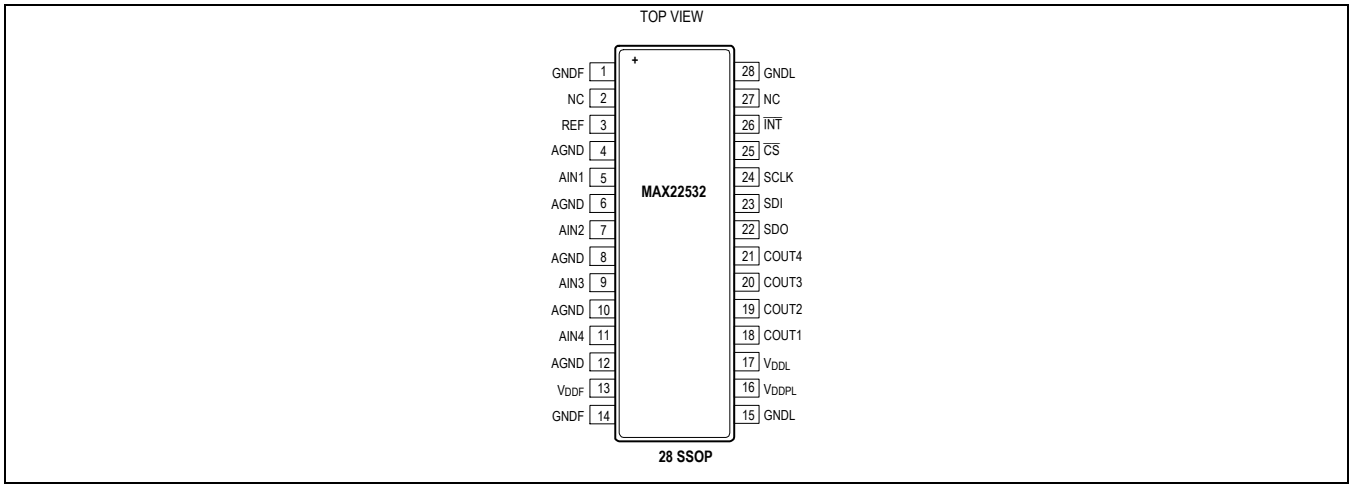


16 W SOIC

TOP VIEW



20 SSOP

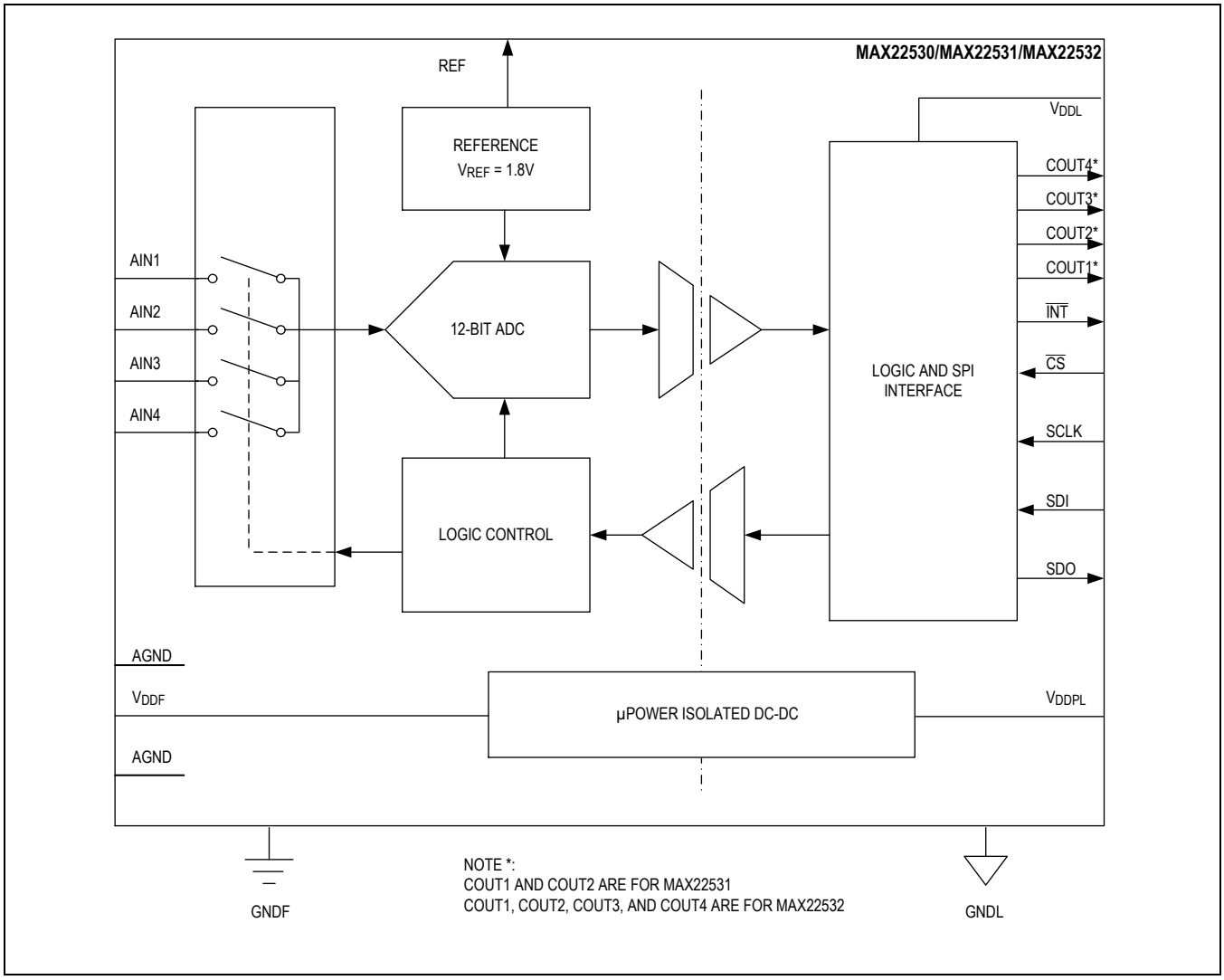


Pin Descriptions

PIN			NAME	FUNCTION	REF SUPPLY
MAX22530	MAX22531	MAX22532			
7	9	13	V_{DDF}	Output of the DC-DC Converter. Bypass to GNDF with 1µF||0.01µF capacitors. The 0.01µF capacitor should be placed as close as possible to the pin.	
8	10	1, 14	GNDF	Field-Side Ground for Everything Except the ADC Front-End and Voltage Reference	VDDF
11	13	17	V_{DDL}	Power Input for the Logic-Side. Bypass with 1µF||0.01µF capacitors to GNDL.	
10	12	16	V_{DDPL}	Power Input for the Isolated DC-DC Converter. The DC-DC converter powers the field-side. Bypass with 1µF||0.01µF capacitors to GNDL.	VDDL
9	11	15, 28	GNDL	Power and Signal Ground for All Logic-Side Pins	
–	–	2, 27	N.C.	Not Connected	
1	1	3	REF	External Filter Capacitor. Connect a 1µF||0.01µF capacitor from REF to AGND.	VDDF
2	2	4	AGND	Analog Ground Reference for AIN_ and REF	VDDF
3	3	5	AIN1	Analog Input Channel 1 The ADC measures the voltage on this pin with respect to AGND	VDDF
4	4	7	AIN2	Analog Input Channel 2. The ADC measures the voltage on this pin with respect to AGND.	VDDF
5	6	9	AIN3	Analog Input Channel 3. The ADC measures the voltage on this pin with respect to AGND.	VDDF
6	7	11	AIN4	Analog Input Channel 4. The ADC measures the voltage on this pin with respect to AGND.	VDDF
-	5, 8	6, 8, 10, 12	AGND	Analog Ground Reference for AIN_ and REF	VDDF
12	16	22	SDO	Serial Data Out for SPI Interface (MISO)	VDDL
13	17	23	SDI	Serial Data Input for SPI Interface (MOSI)	VDDL
14	18	24	SCLK	Serial Clock for SPI Interface	VDDL
15	19	25	CS	Chip Select for SPI Interface. Assert low to enable SPI functions and SDO. SDO and COUT_ are high impedance when CS is high.	VDDL
-	14	18	COUT1	Digital Comparator Output. COUT1 is high when AIN1 is above the upper threshold (COUTHI1) and low when AIN1 is below the	VDDL

				lower threshold (COUTLO1) in digital input mode. See the *Digital Status Mode* section.	
-	15	19	COUT2	Digital Comparator Output. COUT2 is high when AIN2 is above the upper threshold (COUTHI2) and low when AIN2 is below the lower threshold (COUTLO2) in digital input mode. See the *Digital Status Mode* section.	VDDL
-	-	20	COUT3	Digital Comparator Output. COUT3 is high when AIN3 is above the upper threshold (COUTHI3) and low when AIN3 is below the lower threshold (COUTLO3) in digital input mode. See the *Digital Status Mode* section.	VDDL
-	-	21	COUT4	Digital Comparator Output. COUT4 is high when AIN4 is above the upper threshold (COUTHI4) and low when AIN4 is below the lower threshold (COUTLO4) in digital input mode. See the *Digital Status Mode* section.	VDDL
16	20	26	INT	Open-Drain Output that Asserts Low during a number of Different Error Conditions. The cause of the error is latched in the INTERRUPT STATUS register. See the *Diagnostic and Fault Reporting Features* section for details on clearing INT.	VDDL

Functional Diagrams



Detailed Description

The MAX22530–MAX22532 family consists up of 12-bit, 4-channel ADCs with either a 3.5kV$_{RMS}$ or 5kV$_{RMS}$ isolated SPI interface depending upon the package option. Additional features include comparators with programmable upper and lower threshold levels. The ADC and all field-side circuits are powered by an integrated, isolated, DC-DC converter that allows field-side functionality to be verified even when there is no input signal or other field-side supply. This makes the MAX22530–MAX22532 family ideally suited for high-density, multirange, group-isolated, binary-input modules, and provides a complete solution to any system that requires monitoring inputs without a separate isolated power supply.

ADC

The devices' ADC employs a 12-bit SAR architecture with a nominal sampling rate of 20ksps per channel and has an input-voltage range of 0V to +1.8V with respect to AGND. After power-up, the ADC runs continually at the nominal sampling rate. The 12-bit unfiltered ADC reading and filtered ADC reading are both available through the SPI interface. Filtering averages the most recent 4 readings. For rapid response without requiring the SPI interface, the MAX22530–MAX22532 family provides the output of a digital comparator (COUT_) that compares user-programmed thresholds to the ADC reading or the filtered ADC reading. The comparator has two thresholds, the comparator output is high when the input voltage is above the upper threshold and low when it is below the lower threshold in default digital-input mode. The response time of the comparator is less than 75µs (typ) with filtering disabled. With filtering enabled, the comparator uses the moving average of the last 4 ADC readings for a response time of 300µs (typ). The comparator output pin (COUT_) changes based on the latest ADC reading, the upper threshold (COTHI_[11:0], register address 0x9, 0xA, 0xB and 0xC) and the lower threshold (COTLO_[11:0], register address 0x10, 0xD, 0xE and 0xF) according to the CO_MODE_ setting. If enabled, the interrupt pin INT asserts whenever COUT_ changes.

Internal Voltage Reference

The MAX22530-MAX22532 family features a precision internal voltage reference. The 1.8V internal reference has a maximum error of ±2% over the entire operating temperature range. The MAX22530-MAX22532 family is not intended to be used with an external voltage reference.

Input Comparator with Programmable Thresholds and Two Operational Modes (CO_MODE)

The input signal can be recognized in two different ways; one is the digital input mode and the other is the digital status mode. The mode of operation is set for each input channel in the COUTHI_ registers (address 0x9, 0xA, 0xB and 0xC) with the CO_MODE bits.

Digital Input Mode

The Digital input mode (see *Figure 3*) treats the digitized input (from the ADC) as a digital signal of "1" or "0" with hysteresis where the values for "1" and "0" are set by the upper- and lower-limit thresholds programmed into registers COUTHI_ and COUTLO_ (see COUT_BLK in register map).

1. Upper limit and lower limit are used as hysteresis (like a Schmitt trigger input).
2. The status of COUT_ changes to "1" only when the ADC (or FADC) value crosses over the upper limit during a low-to-high transition, and to "0" when it crosses below the lower limit during a high-to-low transition.
3. The status of COUT_ can be "0" or "1" between the lower and upper limits based on the previous status.

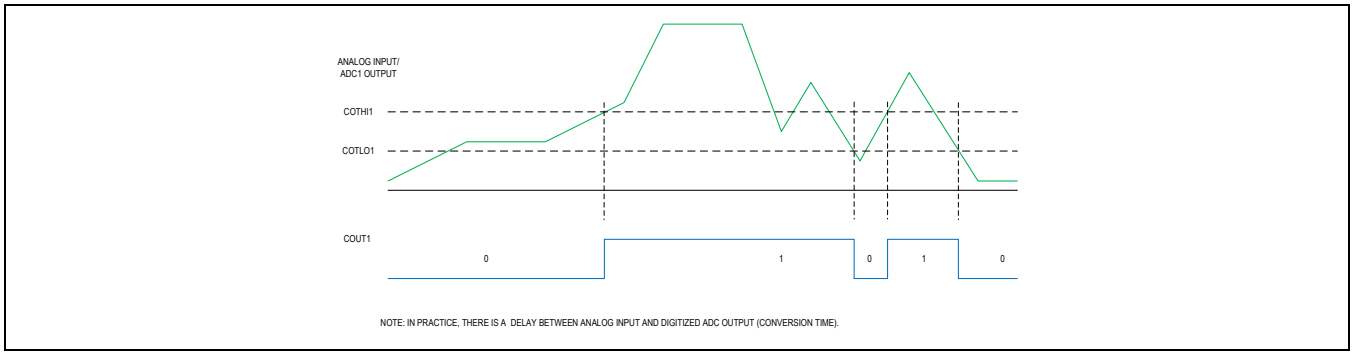


Figure 3. Digital Input Mode

Digital Status Mode

The Digital status mode (see *Figure 4*) monitors the input in “Normal” status vs. “OVLO/UVLO” status:

1. The status of COUT_ is “0” when the digitized output of ADC (or FADC) is between the lower limit and the upper limit.
2. The status of COUT_ is “1” when the digitized output of ADC (or FADC) is higher than the upper limit or lower than the lower limit.

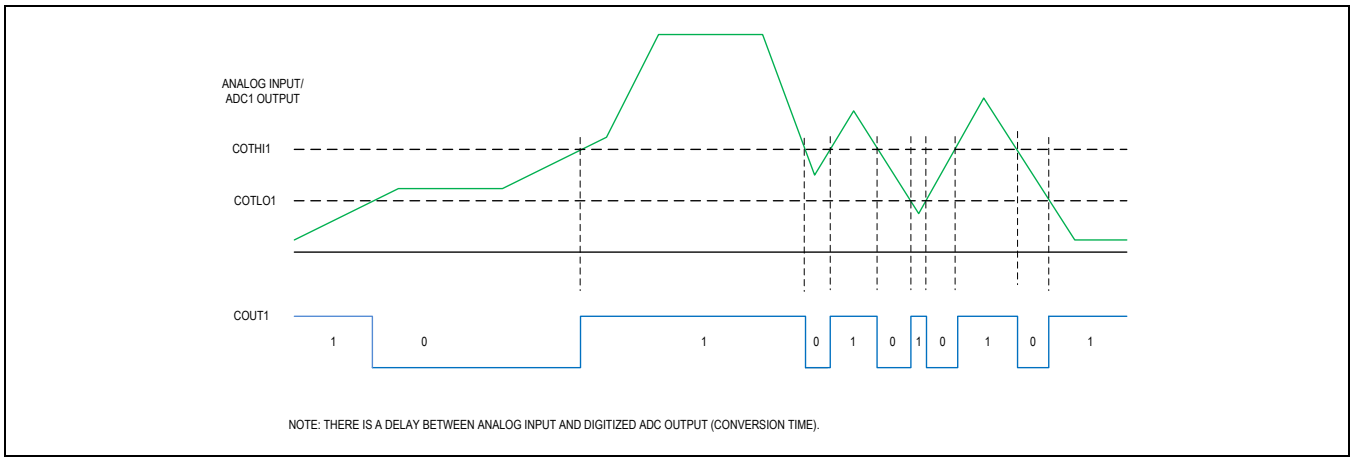


Figure 4. Digital Status Mode

Isolated Power and Data Transfer

A simplified view of the isolated power and data transfer sections is shown in the *Functional Diagram*. The logic-side supply V_{DDPL} powers an integrated, inductively coupled DC-DC converter that generates a nominal field supply V_{DDF} of 3.1V with just enough output current to power the field-side of the MAX22530–MAX22532 family. Note that V_{DDF} is not intended to power an external load.

Serial data is transferred by capacitively-isolated differential transceivers. To verify reliable communication through the isolation barrier, a cyclic redundancy check (8-bit CRC) is embedded in the transmitted serial data streams. If a CRC fails, the data is discarded, and no action is taken. If CRC fails, the SPICRC bits in the INTERRUPT STATUS register is set and INT is asserted if the ENCRC interrupt enable bit is set in the INTERRUPT ENABLE register.

Configuration and Monitoring

An SPI interface is used for transferring configuration, control, and diagnostic data as well as ADC readings between a host (FPGA or microcontroller) and the MAX22530–MAX22532. The interface consists of four signals: SCLK, CS, SDI and SDO, and does not support daisy-chain configuration. An optional CRC improves reliability in the data communication to and from the MAX22530–MAX22532. This feature, disabled by default after reset or power-up, can be enabled or disabled at any time through the SPI interface. When enabled, it affects both read and write SPI transactions.

SPI Interface

SPI communication includes the following features (see **Table 3**):

- Serial clock up to 10MHz
- CRC function uses SMBus polynomial: C(x) = (x8 + x2 + x1 + 1) that is added if the ENCRC bit is set in the CONTROL register.
- Burst Mode for reading multiple registers

The functionality of each SPI pin can be summarized as follows:

- Serial Clock (SCLK): Input for the master serial clock signal. The clock signal determines the speed of the data transfer (up to 10MHz max). All receiving and transmitting is done synchronous to this clock.
- Chip Select (CS): The CS input enables the SPI interface. A logic-high on CS forces SDO to high-impedance and any SCLK transitions are ignored. During a CS logic-low state, data is transferred on the edges of SCLK.
- Serial Input (SDI): SDI or MOSI is the serial input port of the SPI shift register and data is clocked LSB first into the shift register on the rising edge of SCLK. To provide sufficient setup/hold time, the driver should have SDI data transitions at the falling edge of SCLK. On the rising edge of CS, the input data is latched into the internal registers.

- Serial Output (SDO): SDO or MISO is the serial output port of the SPI shift register, and is in a high-impedance state until the CS pin goes to a logic-low state and at the end of the BURST data bit. Data is clocked LSB first out of the shift register on the falling edge of SCLK.

The MAX22530–MAX22532 offers burst and single-register SPI transactions. Single-register SPI transactions can be used to access any register address and are 3-bytes long without CRC and 4-bytes long with CRC. The CRC byte is calculated on the previous 3 bytes. The single-register SPI transaction format consists of a 6-bit register address, a read/write bit, a burst mode bit, 16 bits of payload, and the optional CRC byte, as illustrated in **Table 1** for write transaction and in **Table 2** for read transactions. See **Figure 1** and **Figure 2** for SPI write and read timing diagrams.

-

Table 1. SPI Write Command

HEADER			PAYLOAD	
A[5:0]	W/**R** = 1	BURST = 0	Data D[15:0]	CRC (optional), C[7:0]

Note: The BURST bit in the header is ignored in SPI write transactions

Table 2. SPI Read Command

HEADER			PAYLOAD	
A[5:0]	W/**R** = 0	BURST = 0	Data D[15:0]	CRC (optional), C[7:0]

Burst mode can only be used for reading the filtered or unfiltered ADC data registers and the interrupt status register in one SPI transaction. Burst SPI transactions are 11-bytes long without CRC and 12-bytes long with CRC. The CRC byte is calculated on the previous 11 bytes. The burst SPI transaction format consists of the 6-bit register address for ADC1 or FADC1, a read/write bit, a burst mode bit, the contents of the four filtered or unfiltered ADC registers depending on the 6-bit address entered, the content of the interrupt status register, and the optional CRC byte, as illustrated in **Table 3**. The burst bit is ignored for all other register addresses during read transactions.

The MAX22530–MAX22532 knows that it should receive 24, 32, 88, or 94 bits depending on the combination of CRC setting and burst mode. If more SPI cycles than expected are received, the transaction is executed. If fewer SPI cycles than expected are received, the transaction fails.

Table 3. SPI Burst Read Command

HEADER			PAYLOAD					
A[5:0]	W/**R** = 0	BURST = 1	F/ADC_1 D[15:0]	F/ADC_2 D[15:0]	F/ADC_3 D[15:0]	F/ADC_4 D[15:0]	INTERRUPT STATUS[15:0]	8-bits CRC (optional), C[7:0]

- For burst read transactions, if Address A[5:0] is 0x01 (ADC_1), the data read is the unfiltered ADC data. If Address A[5:0] is 0x05 (FADC_1), the data read is the filtered ADC data.
- The burst bit is ignored for all other register addresses during read transactions.

Diagnostic and Fault Reporting Features

The MAX22530–MAX22532 continuously monitor multiple possible fault conditions, and a hardware alert is provided through the open drain INT pin, which asserts low when an enabled fault is detected. The possible faults are: ADC functionality error, SPI framing error, CRC errors from SPI communications, and loss of internal isolated data stream.

The bits in the INTERRUPT ENABLE (0x13) register determine how the INT output responds to the various error conditions and asserts the INT output if the corresponding bit is enabled in the INTERRUPT ENABLE register.

If the corresponding bit in the INTERRUPT ENABLE register is not set, when an error is flagged, INT is not asserted, but the bit in the INTERRUPT STATUS register (0x12) is still latched and remains set until the register is read, which automatically clears all bits in the INTERRUPT STATUS register. Note that if a fault condition still exists when the register is read, the cleared fault bit is immediately set again.

In a typical application, INT triggers an interrupt routine in the microcontroller or FPGA, which reads the INTERRUPT STATUS register to determine the cause of the interrupt.

ADC Functionality Error

ADC functionality is checked by looking for changes in the ADC output. To ensure that a change should have occurred, a special test measurement is made while injecting a small current at the input of the ADC. This special measurement used for ADC functionality verification is interleaved between normal measurements and does not affect the ADC sampling time. If the ADC reading does not change, or data is outside of the limits for at least four frames, an ADC functional failure is declared and bit FADC (bit 11) in the INTERRUPT STATUS (0x12) register is set.

SPI Framing Error

After CS transitions from low to high, if the number of bits clocked in while CS was low is not 24, 32, 88, or 96 bits, an SPI framing error is declared and bit SPIFRM (bit 9) in the INTERRUPT STATUS (0x12) register is set. The instruction in the SPI shift register is not decoded and no register value is changed.

Loss of Data Stream

The field-side sends ADC data across the isolation barrier to the logic-side every 50µs except for the startup period. Field-side loss-of-data (FLD) interrupts are masked for the first 100ms of operation after power-on or reset, and after that if an internal monitoring signal is not received, an error is flagged. If the periodic field-side data is not received, a loss-of-data-stream fault is declared and bit FLD (bit 10) in the INTERRUPT STATUS (0x12) register is set. It is possible to recover from a loss of data stream fault by asserting a hard reset using bit REST (bit 0) in the CONTROL (0x14) register, which causes field-side power to be rebooted and returns all of the registers to their default state, requiring the MAX22530–MAX22532 to go through the startup configuration process.

CRC Error from Internal Communication

Internal communication across the isolation barrier includes a CRC code to ensure that corrupt data does not cause system problems. If the CRC indicates an error, the received data is discarded. If six consecutive CRCs fail, a CRC fault is declared and bit SPICRC (bit 8) in the INTERRUPT STATUS (0x12) register is set.

Control Modes

The CONTROL (0x14) register includes a number of bits which the host can program and which take immediate effect on the device.

Hardware Reset Control

If the control bit REST is set to 1, the field-side power supply is shut down and restarted, and the main reset input to the digital core is asserted, resulting in setting the digital core back to its power-on reset state and all registers are brought back to their default values, including the control bit, REST.

Software Reset Control

The software reset is initiated by setting bit SRES to 1. Unlike the hardware reset that is effective immediately after assertion, SRES takes affect after the completion of the frame, during which it is asserted. At that time, the digital core is reset and all registers are brought back to their default values. The field-side power supply is not affected by SRES.

Clear POR Control

The CLRPOR bit can be set to 1 to clear the ‘Wake Up from Power-On Reset’ POR bit in the PROD_ID (0x00) register. Note that a hardware reset (REST) causes the POR bit to be reasserted, but a software reset, SRES, has no effect on the status bit POR.

DISPWR Control

Setting bit DISPWR to 1 disables field-side power (V_{DDF}), effectively stopping ADC conversions. The logic-side or digital core is not affected.

Filter Clearing Control

The control bits FLT_CLR_1 to FLT_CLR_4 can be set to 1 to clear the ADC moving average filter for that specific channel at the start of the frame following this assertion. Once the filter reset operation takes place the control bits remain set at 0 for normal operation.

Comparator Limit Control

The control bit ECOM can be set to 1 to apply the settings of COUTHI1 and COUTLO1 to all four channels regardless of what values are programmed in the high and low threshold registers for the other three channels. Setting the ECOM bit to 1 does not change what the host reads back from the threshold registers for channels 2 to 4.

CRC Control

If control bit ENCRC is 0, CRC functionality is not enabled, and SPI transactions are 24-bits in length. But if control bit ENCRC is 1, CRC functionality is enabled making each SPI transaction 32-bits in length. At power-on, or after a hardware or software reset, the default CRC is disabled. All SPI transactions following the write transaction that sets ENCRC must have the 8-bit CRC suffix.

Interrupts

In a system, the MAX22530–MAX22531 device operations can be monitored by the host (typically a microcontroller or FPGA) by either polling the ADC_ registers or by using the end-of-conversion (EOC) interrupt bit in the INTERRUPT ENABLE (0x13) register to assert the interrupt pin, INT. The ADC core continually digitizes the inputs for the four channels in succession, and the host can determine the ADC conversion state by polling the ADCs bit in each ADC_ register (bit 15), or by enabling the EOC to be shown on the INT every 50 µs. If the EOC interrupt is enabled, bit EOC (bit 12) in the INTERRUPT STATUS (0x12) register is set to 1 and causes the INT pin to be asserted for a duration of 10µs at the end of channel 4 ADC (ADC_4) conversion. After 10µs the INT pin is deasserted whether the INTERRUPT STATUS register is read or not.

At that time, the unfiltered (ADC_) and filtered (FADC_) data are available to be read through SPI, as well as the comparator status and comparator-related interrupts.

If the host is polling the SPI interface for ADC status, the burst read command allows it to read all four ADC registers (ADC1 to ADC4, or FADC1 to FADC4. See ADC_STATUS BLK in register map section) in addition to the INTERRUPT STATUS register. Bit 15 in each ADC_ register is the ADCs bit. If ADCs is 0 the register contents have been updated (new conversion data) since the last read operation. By performing a data read operation, the ADCs bit is automatically set to 1, indicating the data has not been refreshed since the last read operation. Upon receiving the INT signal, the host interrupt service routine can perform a burst read, which automatically clears the bits in the INTERRUPT STATUS register, thereby deasserting the INT pin.

If the host does not access the ADC_ data registers at least once per frame (whether by polling or responding to INT being asserted) then data loss occurs, and the register contents are overwritten with new conversion data.

If the ADC_ data register refreshing event occurs while CS is low (i.e., during an SPI transaction), the data refreshing event is postponed until the deassertion of CS. This scheme eliminates possible data corruption and data loss. However, it assumes that the rate of the SPI transaction is equal to or greater than the rate of ADC sampling (20ksps), and that the duration of any SPI transaction is shorter than that of a 4-channel conversion frame. The host can safely read the ADC_ data registers during the 50µs following the assertion of the end-of-conversion interrupt.

The host can set the limits against which the ADC data is compared. The host can select if a given channel uses the unfiltered (ADC_) or the filtered ADC (FADC_) data for comparison against the limits using the control bits CO_MODE (bit 15) and CO_IN_SEL (bit 14) in each COUTHI_ register. The CO_MODE bits determine the comparator mode of operation (Digital Data Mode if the bit is set to 0 or Digital Status Mode if the bit is set to 1) and CO_IN_SEL selects between unfiltered ADC data (bit set to 0) of filtered ADC data (bit set to 1). The status of the comparison for each channel can be read from register COUT STATUS (0x11).

In addition to the diagnostics bits, the comparator outputs can be programmed to assert the INT pin if enabled. If a positive edge is detected by the comparator, the bit CO_POS_ is set to 1 indicating the ADC_ data is greater than the upper limit (COUTHI_). Similarly, if a negative edge is detected by the comparator, the bit CO_NEG_ is set to 1 indicating the ADC_ data is lower than the lower limit (COUTLO_).

Changes to comparator control register contents take effect on the next frame. For example, if COUTHI_4[11:0] is changed during frame N, the new threshold value is used starting frame N+1.

To clear an interrupt and deactivate the INT pin, the host must perform a read operation of the INTERRUPT STATUS register. All bits in the INTERRUPT STATUS register are “Read Clears All.” Interrupts are cleared whether the CRC is properly decoded by the host or not. Note that if a fault condition still exists when the register is read, the cleared fault bit is immediately set again.

If an interrupt is not set at the time that the INTERRUPT STATUS register is read, and if that interrupt gets asserted while the interrupt register is being read, that interrupt bit is not cleared upon the end of the SPI read transaction.

However, if an interrupt that is set at the time that the interrupt register is read, and if another identical interrupt gets asserted while the interrupt register is being read, that interrupt bit is cleared upon the end of the SPI transaction. This means that the host should read the interrupt register upon assertion of INT, or poll the interrupt registers several times per conversion cycles to avoid missing interrupts.

In a system, the MAX22530–MAX22531 device operations can be monitored by the host (typically a microcontroller or FPGA) by either polling the ADC_ registers or by using the end-of-conversion (EOC) interrupt bit in the INTERRUPT ENABLE (0x13) register to assert the interrupt pin, INT. The ADC core continually digitizes the inputs for the four channels in succession, and the host can determine the ADC conversion state by polling the ADCs bit in each ADC_ register (bit 15), or by enabling the EOC to be shown on the INT every 50 µs. If the EOC interrupt is enabled, bit EOC (bit 12) in the INTERRUPT STATUS (0x12) register is set to 1 and causes the INT pin to be asserted for a duration of 10µs at the end of channel 4 ADC (ADC_4) conversion. After 10µs the INT pin is deasserted whether the INTERRUPT STATUS register is read or not.

At that time, the unfiltered (ADC_) and filtered (FADC_) data are available to be read through SPI, as well as the comparator status and comparator-related interrupts.

If the host is polling the SPI interface for ADC status, the burst read command allows it to read all four ADC registers (ADC1 to ADC4, or FADC1 to FADC4) in addition to the INTERRUPT STATUS register. Bit 15 in each ADC_ register is the ADCs bit. If ADCs is 0 the register contents have been updated (new conversion data) since the last read operation. By performing a data read operation, the ADCs bit is automatically set to 1, indicating the data has not been refreshed since the last read operation. Upon receiving the INT signal, the host interrupt service routine can perform a burst read, which automatically clears the bits in the INTERRUPT STATUS register, thereby deasserting the INT pin.

If the host does not access the ADC_ data registers at least once per frame (whether by polling or responding to INT being asserted) then data loss occurs, and the register contents are overwritten with new conversion data.

If the ADC_ data register refreshing event occurs while CS is low (i.e., during an SPI transaction), the data refreshing event is postponed until the deassertion of CS. This scheme eliminates possible data corruption and data loss. However, it assumes that the rate of the SPI transaction is equal to or greater than the rate of ADC sampling (20ksps), and that the duration of any SPI transaction is shorter than that of a 4-channel conversion frame. The host can safely read the ADC_ data registers during the 50µs following the assertion of the end-of-conversion interrupt.

The host can set the limits against which the ADC data is compared. The host can select if a given channel uses the unfiltered (ADC_) or the filtered ADC (FADC_) data for comparison against the limits using the control bits CO_MODE (bit 15) and CO_IN_SEL (bit 14) in each COUTHI_ register. The CO_MODE bits determine the comparator mode of operation (Digital Data Mode if the bit is set to 0 or Digital Status Mode if the bit is set to 1) and CO_IN_SEL selects between unfiltered ADC data (bit set to 0) of filtered ADC data (bit set to 1). The status of the comparison for each channel can be read from register COUT STATUS.

In addition to the diagnostics bits, the comparator outputs can be programmed to assert the INT pin if enabled. If a positive edge is detected by the comparator, the bit CO_POS_ is set to 1 indicating the ADC_ data is greater than the upper limit (COUTHI_). Similarly, if a negative edge is detected by the comparator, the bit CO_NEG_ is set to 1 indicating the ADC_ data is lower than the lower limit (COUTLO_).

Changes to comparator control register contents take effect on the next frame. For example, if COUTHI_4[11:0] is changed during frame N, the new threshold value is used starting frame N+1.

To clear an interrupt and deactivate the INT pin, the host must perform a read operation of the INTERRUPT STATUS register (0x12). All bits in the INTERRUPT STATUS register are “Read Clears All.” Interrupts are cleared whether the CRC is properly decoded by the host or not. Note that if a fault condition still exists when the register is read, the cleared fault bit is immediately set again.

If an interrupt is not set at the time that the INTERRUPT STATUS register is read, and if that interrupt gets asserted while the interrupt register is being read, that interrupt bit is not cleared upon the end of the SPI read transaction.

However, if an interrupt that is set at the time that the interrupt register is read, and if another identical interrupt gets asserted while the interrupt register is being read, that interrupt bit is cleared upon the end of the SPI transaction. This means that the host should read the interrupt register upon assertion of INT, or poll the interrupt registers several times per conversion cycles to avoid missing interrupts.

Digital Isolation

The MAX22530-MAX22532 provide basic galvanic isolation for both power and digital signals that are transmitted from the field side to the logic side.

The MAX22530 device withstands differences in ground potential between the two power domains of up to $5kV_{RMS}$ (V_{ISO}) for up to 60s, and up to $848V_{RMS}$ (V_{IOWM}) for extended periods of time. The MAX22530 is available is 16-pin wide body SOIC package with 8mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 400V to give a group II rating in creepage tables. See *Table 4* for certification information.

The MAX22531 and MAX22532 device withstand differences in ground potential between the two power domains of up to 3.75KVRMS (V_{ISO}) for up to 60s, and up to $445V_{RMS}$ (V_{IOWM}) for extended periods of time. The MAX22531 is available in 20-pin SSOP and MAX22532 is available in 28-pin SSOP with 5.5mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 400V to give a group II rating in creepage tables. See *Table 4* for certification information.

Table 4. Safety Regulatory Approvals

UL
The MAX22530, MAX22531 are certified under UL1577. For more details, refer to File E351759
The MAX22530 is rated up to $5000V_{RMS}$ isolation voltage for single protection.
The MAX22531 is rated up to $3750V_{RMS}$ isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX22530 is certified up to $5000V_{RMS}$ isolation voltage. For more details, refer to File E351759
The MAX22531 is rated up to $3750V_{RMS}$ isolation voltage. For more details, refer to File E351759

Applications Information

Power Supply Decoupling

It is recommended to decouple both the V_{DDL} and V_{DDPL} supplies with 1µF capacitors in parallel with 0.01µF capacitors to GNDL. Place the 0.01µF capacitors as close to V_{DDL} and V_{DDPL} as possible. The V_{DDF} pin is the integrated DC-DC converter output and it is recommended to decouple it with low-ESR capacitors of 1µF in parallel with 0.01µF to GNDF. Place the 0.01µF capacitor as close to V_{DDF} as possible.

Layout Considerations

The PCB designer should follow some critical recommendations to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low inductance, avoid using vias.
- Have a solid ground plane underneath the signal layer to minimize the noise.
- Keep the area underneath the MAX22530–MAX22532 free from ground and signal planes. Any galvanic or metallic connection between the field side and logic side defeats the isolation.
- Ensure that the decoupling capacitors between VDDL, VDDPL and GNDL, and between VDDF and GNDF are located as close as possible to the IC to minimize inductance.
- Route important signal lines close to the ground plane to minimize possible external influences. On the field-side, it is good practice to separate the ADC input and voltage reference ground AGND from the VDDF reference ground GNDF.
- MAX22531 has two extra AGND pins, and MAX22532 has four extra AGND pins to provide analog ground reference points for the respective AIN_ channels.

Radiated Emissions

The MAX22530–MAX22532 family features an integrated DC-DC converter to generate a nominal 3.1V supply, powering the field side of the MAX22530–MAX22532. The DC-DC converter passes power from the logic side across the isolation barrier through an internal transformer. Due to the isolated nature of the device, the split of the ground planes (GNDL and GNDF) prevents the return current from flowing back to the logic side; thus, causing high-frequency signals to radiate when crossing the isolation barrier. A spread-spectrum option is added to the DC-DC converter to reduce the radiated emissions.

The MAX22530–MAX22532 can meet CISPR 22 and FCC radiated emission standards with proper PCB design. A stitching capacitance of 50pF minimum is recommended to be built into the PCB to pass the CISPR 22 and FCC Class B limits. See Figure 7 and Figure 8.

To achieve optimal radiated emission performance, the following layout guidelines are recommended:

- Use at least a 4-layer PCB stackup with GNDL and GNDF ground planes on two adjacent internal layers.
- Extend the GNDF and GNDL planes on two adjacent layers so they overlap each other; thus, creating a stitching capacitance between GNDL and GNDF. See Figure 5 and Figure 6.

Calculate the stitching capacitance value by using the following equation, where A is the overlapping area between the GNDL and GNDF planes.

$$C = A \times \varepsilon 0 \times \varepsilon r \times d$$

where,

ε0 = Permittivity of free space (8.854 x 10-12 F/m),

εr = Relative permittivity of the PCB insulation material, and

d = Dielectric thickness between two adjacent layers.

- Adjust the overlapping area (A) or the dielectric thickness (d) to achieve a minimum 50pF stitching capacitance. Make sure that the creepage and clearance between the GNDF plane and the GNDL plane on the same layer as well as between two different layers large enough to meet isolation standards for various applications.
- Multiple GNDL and GNDF vias are recommended to be placed next to the GNDF and GNDL pins to provide a good connection between the stitching capacitor and the device ground pins.
- Apply edge guarding vias to stitch the GNDF and GNDL planes on all layers together to limit the emission from escaping from the PCB edges.

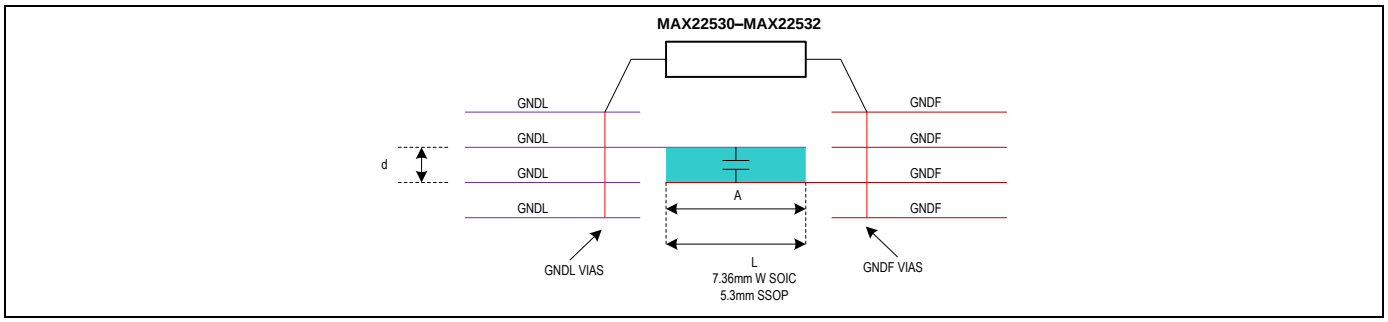


Figure 5. Stitching Capacitance Example on a 4- Layer PCB

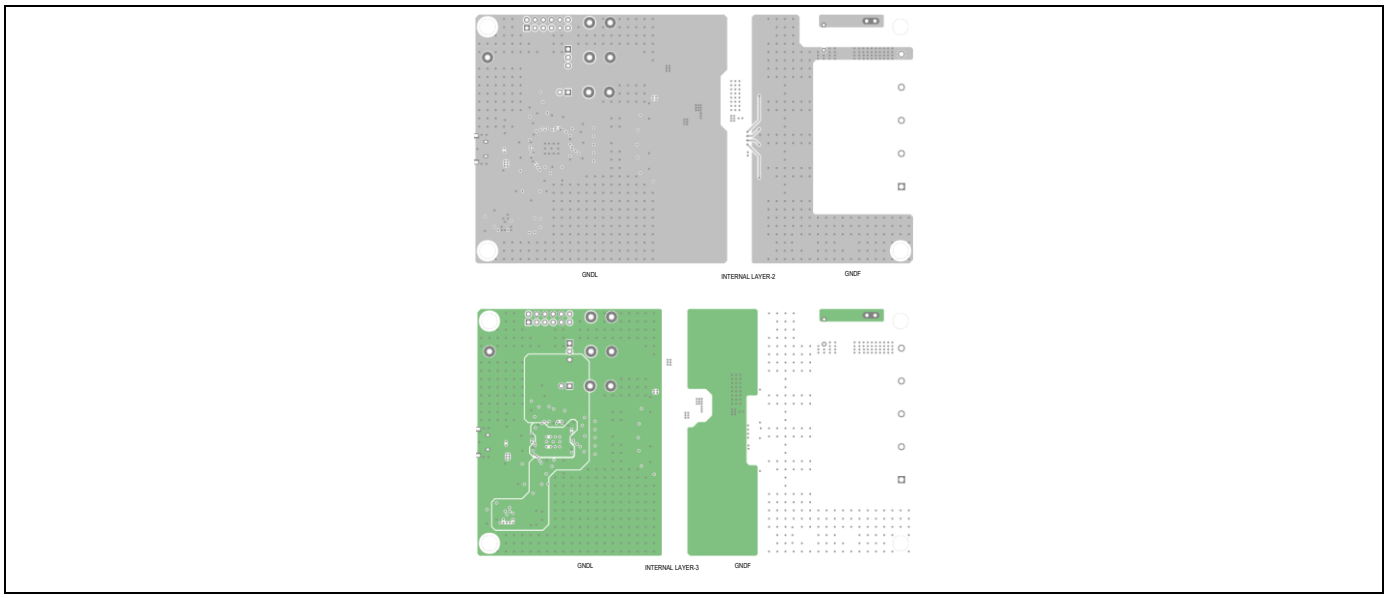


Figure 6. Stitching Capacitance on Internal Layers

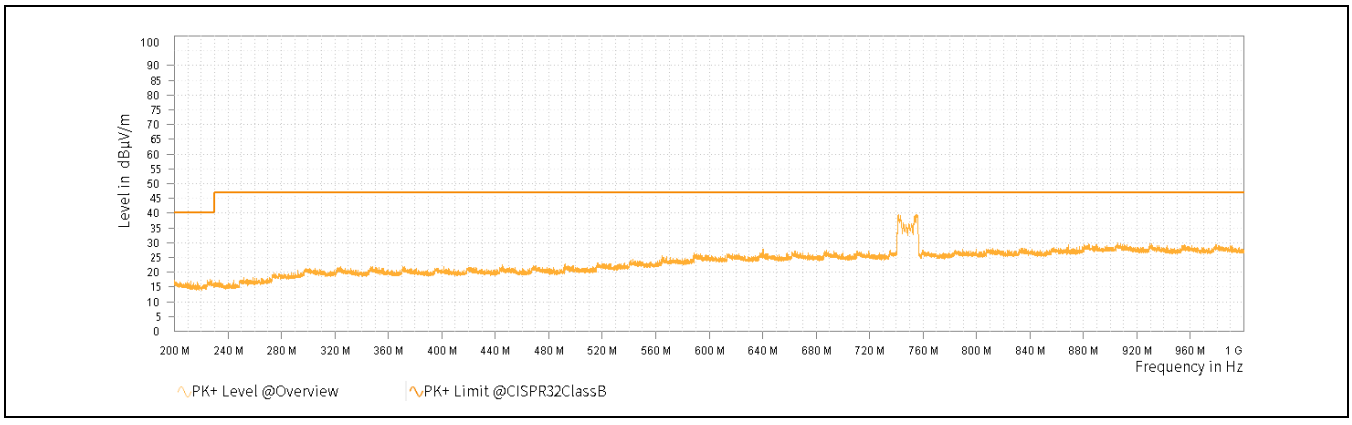


Figure 7. MAX22530 Radiated Emission with 90pF Stitching Capacitance, 3-Meter Antenna Distance, Horizontal Scan

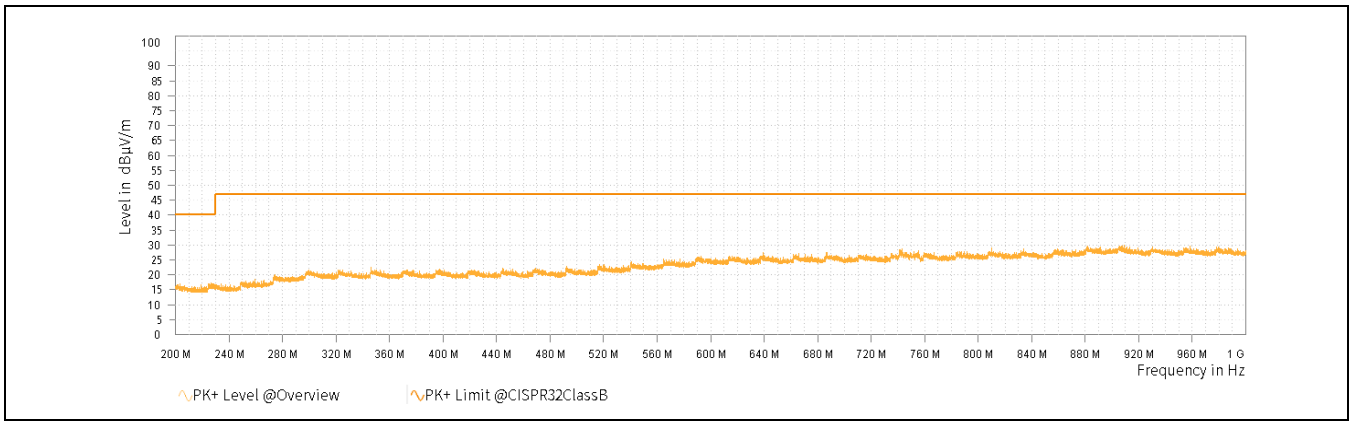


Figure 8. MAX22530 Radiated Emission with 90pF Stitching Capacitance, 3-Meter Antenna Distance, Vertical Scan

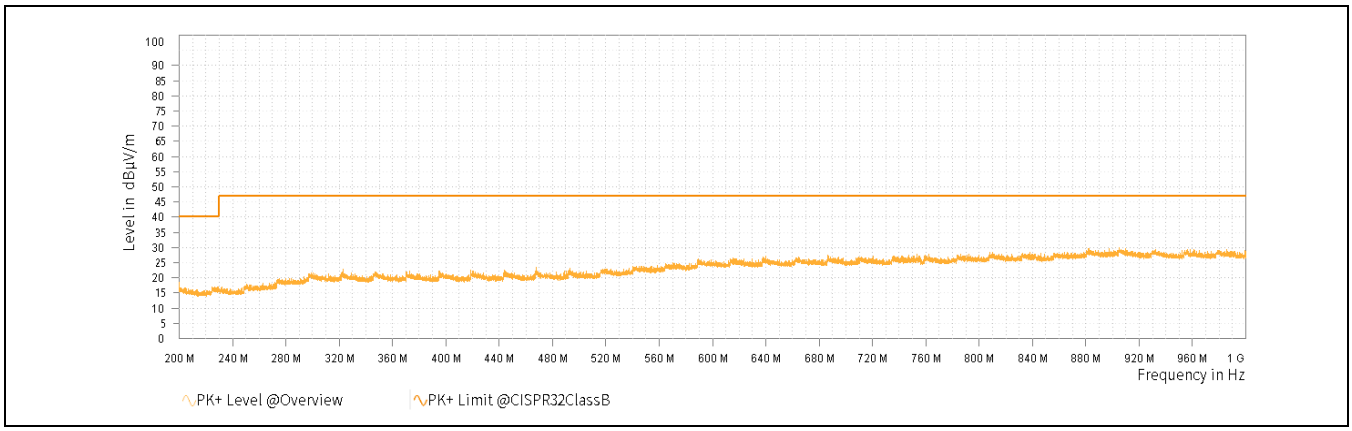


Figure 9. MAX22531 Radiated Emission with 100pF Stitching Capacitance, 3-Meter Antenna Distance, Horizontal Scan

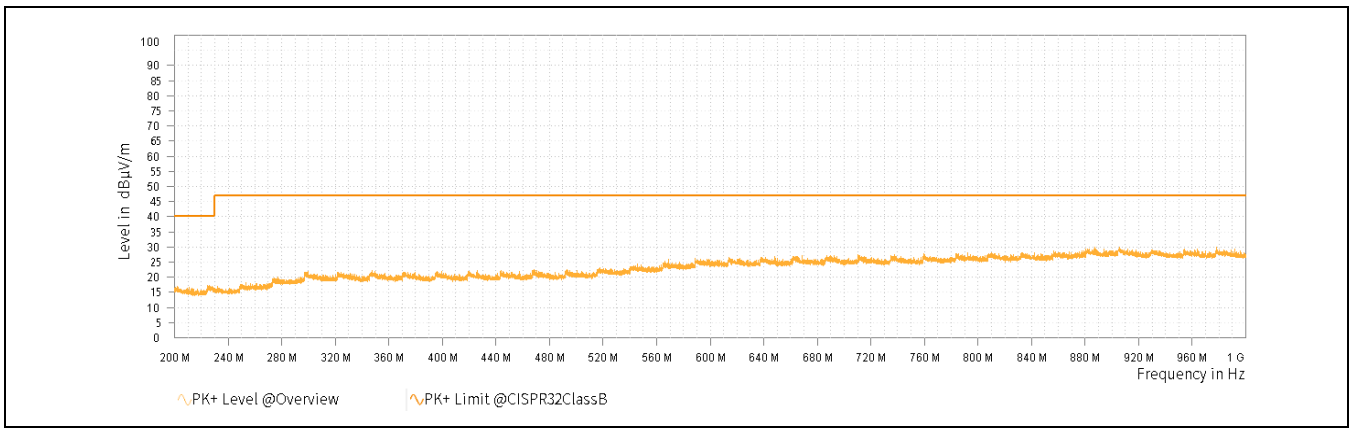


Figure 10. MAX22531 Radiated Emission with 100pF Stitching Capacitance, 3-Meter Antenna Distance, Vertical Scan

Register Map

SPI_Register_MAP

ADDRESS	NAME	MSB							LSB
ID_BLK									
0x00	PROD_ID[15:8]	DEVICE_ID[7:0]							
	PROD_ID[7:0]	POR	DEVICE_REV[6:0]						
ADC_STATUS BLK									
0x01	ADC 1[15:8]	ADCS	–	–	–	ADC[11:8]			
	ADC 1[7:0]	ADC[7:0]							
0x02	ADC 2[15:8]	ADCS	–	–	–	ADC[11:8]			
	ADC 2[7:0]	ADC[7:0]							
0x03	ADC 3[15:8]	ADCS	–	–	–	ADC[11:8]			
	ADC 3[7:0]	ADC[7:0]							
0x04	ADC 4[15:8]	ADCS	–	–	–	ADC[11:8]			
	ADC 4[7:0]	ADC[7:0]							
0x05	FADC 1[15:8]	–	–	–	–	FADC[11:8]			
	FADC 1[7:0]	FADC[7:0]							
0x06	FADC 2[15:8]	–	–	–	–	FADC[11:8]			
	FADC 2[7:0]	FADC[7:0]							
0x07	FADC 3[15:8]	–	–	–	–	FADC[11:8]			
	FADC 3[7:0]	FADC[7:0]							
0x08	FADC 4[15:8]	–	–	–	–	FADC[11:8]			
	FADC 4[7:0]	FADC[7:0]							
COUT_BLK									
0x09	COUTHI 1[15:8]	CO_MODE	CO_IN_SEL	–	–	COTHI[11:8]			
	COUTHI 1[7:0]	COTHI[7:0]							
0x0A	COUTHI 2[15:8]	CO_MODE	CO_IN_SEL	–	–	COTHI[11:8]			

ADDRESS	NAME	MSB							LSB
	COUTHI 2[7:0]	COTHI[7:0]							
0x0B	COUTHI 3[15:8]	CO_MODE	CO_IN_SEL	–	–	COTHI[11:8]			
	COUTHI 3[7:0]	COTHI[7:0]							
0x0C	COUTHI 4[15:8]	CO_MODE	CO_IN_SEL	–	–	COTHI[11:8]			
	COUTHI 4[7:0]	COTHI[7:0]							
0x0D	COUTLO 1[15:8]	–	–	–	–	COTLO[11:8]			
	COUTLO 1[7:0]	COTLO[7:0]							
0x0E	COUTLO 2[15:8]	–	–	–	–	COTLO[11:8]			
	COUTLO 2[7:0]	COTLO[7:0]							
0x0F	COUTLO 3[15:8]	–	–	–	–	COTLO[11:8]			
	COUTLO 3[7:0]	COTLO[7:0]							
0x10	COUTLO 4[15:8]	–	–	–	–	COTLO[11:8]			
	COUTLO 4[7:0]	COTLO[7:0]							
CONTROL_STATUS									
0x11	COUT STATUS[15:8]	–	–	–	–	–	–	–	–
	COUT STATUS[7:0]	–	–	–	–	CO_4	CO_3	CO_2	CO_1
0x12	INTERRUPT STATUS[15:8]	–	–	–	EOC	ADCF	FLD	SPIFRM	SPICRC
	INTERRUPT STATUS[7:0]	CO_POS_4	CO_POS_3	CO_POS_2	CO_POS_1	CO_NEG_4	CO_NEG_3	CO_NEG_2	CO_NEG_1
0x13	INTERRUPT ENABLE[15:8]	–	–	–	EEOC	EFADC	EFLD	ESPIFRM	ESPICRC
	INTERRUPT ENABLE[7:0]	ECO_POS_4	ECO_POS_3	ECO_POS_2	ECO_POS_1	ECO_NEG_4	ECO_NEG_3	ECO_NEG_2	ECO_NEG_1
0x14	CONTROL[15:8]	ENCRC	ECOM	–	–	–	–	–	–
	CONTROL[7:0]	FLT_CLR_4	FLT_CLR_3	FLT_CLR_2	FLT_CLR_1	DISPWR	CLRPOR	SRES	REST

Register Details

PROD_ID (0x0)

Device ID Register

BIT	15	14	13	12	11	10	9	8
Field	DEVICE_ID[7:0]							
Reset	0x00							
Access Type	Read Only							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	POR	DEVICE_REV[6:0]						
Reset	0b0	0x01						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
DEVICE_ID	15:8	Device ID	0x0: MAX22530/MAX22531/MAX22532
POR	7	Power-On Reset	0x0: Normal Operation 0x1: Wake up from Power-On Reset
DEVICE_REV	6:0	Revision Control of die	0x0: Initial Die Revision

ADC (0x1, 0x2, 0x3, 0x4)

ADC_ Data Register

BIT	15	14	13	12	11	10	9	8
Field	ADCS	–	–	–	ADC[11:8]			
Reset	0b0	–	–	–	0x000			
Access Type	Read Sets All	–	–	–	Read Only			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	ADC[7:0]							
Reset	0x000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADCS	15	ADC Data Read Check function	0x0: ADC has been updated since last read operation 0x1: ADC has not been updated since last read operation
ADC	11:0	Unfiltered ADC Data	

FADC (0x5, 0x6, 0x7, 0x8)

Filtered ADC_ Data Register

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	FADC[11:8]			
Reset	–	–	–	–	0x000			
Access Type	–	–	–	–	Read Only			
BIT	7	6	5	4	3	2	1	0
Field	FADC[7:0]							
Reset	0x000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FADC	11:0	Filtered ADC Data

COUTHI (0x9, 0xA, 0xB, 0xC)

BIT	15	14	13	12	11	10	9	8
Field	CO_MODE	CO_IN_SEL	–	–	COTHI[11:8]			
Reset	0b0	0b0	–	–	0xB32			
Access Type	Write, Read	Write, Read	–	–	Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	COTHI[7:0]							
Reset	0xB32							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CO_MODE	15	Comparator Output Operation Mode Selection	0x0: Digital Input Mode 0x1: Digital Status Mode
CO_IN_SEL	14	Comparator Input Selection	0x0: Unfiltered ADC data is used as input to the comparator 0x1: Filtered ADC data is used as input to the comparator
COTHI	11:0	Comparator Threshold High Value	0xB32h: 70% of range

COUTLO (0x10, 0xD, 0xE, 0xF)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	COTLO[11:8]			
Reset	–	–	–	–	0x4CC			
Access Type	–	–	–	–	Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	COTLO[7:0]							
Reset	0x4CC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
COTLO	11:0	Comparator Threshold Low Value	0x4CCh: 30% of range

COUT STATUS (0x11)

Digital Comparator COUT_ Status Register

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CO_4	CO_3	CO_2	CO_1

Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
CO_4	3	Comparator Output status: when CO_MODE = 0/1	0x0: MODE 0: The ADC value is lower than COUTLO value. MODE 1: The ADC value is within COUTHI and COUTLO. 0x1: MODE 0: The ADC value is higher than COUTHI value. MODE 1: The ADC value is higher than COUTHI value or lower than COUTLO value.
CO_3	2	Comparator Output status: when CO_MODE = 0/1	0x0: MODE 0: The ADC value is lower than COUTLO value. MODE 1: The ADC value is within COUTHI and COUTLO. 0x1: MODE 0: The ADC value is higher than COUTHI value. MODE 1: The ADC value is higher than COUTHI value or lower than COUTLO value.
CO_2	1	Comparator Output status: when CO_MODE = 0/1	0x0: MODE 0: The ADC value is lower than COUTLO value. MODE 1: The ADC value is within COUTHI and COUTLO. 0x1: MODE 0: The ADC value is higher than COUTHI value. MODE 1: The ADC value is higher than COUTHI value or lower than COUTLO value.
CO_1	0	Comparator Output status: when CO_MODE = 0/1	0x0: MODE 0: The ADC value is lower than COUTLO value. MODE 1: The ADC value is within COUTHI and COUTLO. 0x1: MODE 0: The ADC value is higher than COUTHI value. MODE 1: The ADC value is higher than COUTHI value or lower than COUTLO value.

INTERRUPT STATUS (0x12)

Interrupt Status Register

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	EOC	ADCF	FLD	SPIFRM	SPICRC
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	CO_POS_4	CO_POS_3	CO_POS_2	CO_POS_1	CO_NEG_4	CO_NEG_3	CO_NEG_2	CO_NEG_1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
EOC	12	Enable End of ADC Conversion Interrupt	0x0: No end of conversion event 0x1: End of conversion of one cycle of Channel 1 to 4 event detected
ADCF	11	ADC Functionality Interrupt	0x0: Correct ADC functionality: ADC Diagnostic values are in range 0x1: Faulty ADC functionality: ADC Diagnostic values are not in range
FLD	10	Field Data Interrupt	0x0: No data loss 0x1: Loss of data occurred
SPIFRM	9	SPI Frame Error Interrupt	0x0: No SPI frame error detected 0x1: At least one SPI frame error was detected
SPICRC	8	SPI CRC Error Interrupt	0x0: No SPI CRC error detected 0x1: At least one SPI CRC error was detected
CO_POS_4	7	Comparator Output 4 low-to-high transition interrupt	0x0: No positive edge was detected by Comparator 4 0x1: At least one positive edge was detected by Comparator 4
CO_POS_3	6	Comparator Output 3 low-to-high transition interrupt	0x0: No positive edge was detected by Comparator 3 0x1: At least one positive edge was detected by Comparator 3
CO_POS_2	5	Comparator Output 2 low-to-high transition interrupt	0x0: No positive edge was detected by Comparator 2 0x1: At least one positive edge was detected by Comparator 2
CO_POS_1	4	Comparator Output 1low-to-high transition interrupt	0x0: No positive edge was detected by Comparator 1 0x1: At least one positive edge was detected by Comparator 1
CO_NEG_4	3	Comparator Output 4 high-to-low transition interrupt	0x0: No negative edge was detected by Comparator 4 0x1: At least one negative edge was detected by Comparator 4
CO_NEG_3	2	Comparator Output 3 high-to-low transition interrupt	0x0: No negative edge was detected by Comparator 3 0x1: At least one negative edge was detected by Comparator 3
CO_NEG_2	1	Comparator Output 2 high-to-low transition interrupt	0x0: No negative edge was detected by Comparator 2 0x1: At least one negative edge was detected by Comparator 2
CO_NEG_1	0	Comparator Output 1 high-to-low transition interrupt	0x0: No negative edge was detected by Comparator 1 0x1: At least one negative edge was detected by Comparator 1

INTERRUPT ENABLE (0x13)

Interrupt Enable Register

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	EEOC	EFADC	EFLD	ESPIFRM	ESPICRC
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	ECO_POS_4	ECO_POS_3	ECO_POS_2	ECO_POS_1	ECO_NEG_4	ECO_NEG_3	ECO_NEG_2	ECO_NEG_1

Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EEOC	12	Enable End of ADC Conversion Interrupt	0x0: EOC Interrupt Disabled 0x1: FADC Interrupt
EFADC	11	Enable ADC Fault Interrupt	0x0: FADC Interrupt Disabled 0x1: FADC Interrupt Enabled
EFLD	10	Enable Loss Data Fault Interrupt	0x0: EFLD Interrupt Disabled 0x1: EFLD Interrupt Enabled
ESPIFRM	9	Enable SPI Frame Fault Interrupt	0x0: SPIFRM Interrupt Disabled 0x1: SPIFRM Interrupt Enabled
ESPICRC	8	Enable SPI CRC Fault Interrupt	0x0: SPICRC Interrupt Disabled 0x1: SPICRC Interrupt Enabled
ECO_POS_4	7	Enable COUT4 Positive Transition Interrupt	0x0: Disable CO_POS4 Interrupt 0x1: Enable CO_POS4 Interrupt
ECO_POS_3	6	Enable COUT3 Positive Transition Interrupt	0x0: Disable CO_POS3 Interrupt 0x1: Enable CO_POS3 Interrupt
ECO_POS_2	5	Enable COUT2 Positive Transition Interrupt	0x0: Disable CO_POS2 Interrupt 0x1: Enable CO_POS2 Interrupt
ECO_POS_1	4	Enable COUT1 Positive Transition Interrupt	0x0: Disable CO_POS1 Interrupt 0x1: Enable CO_POS1 Interrupt
ECO_NEG_4	3	Enable COUT4 Negative Transition Interrupt	0x0: Disable CO_NEG4 Interrupt 0x1: Enable CO_NEG4 Interrupt
ECO_NEG_3	2	Enable COUT3 Negative Transition Interrupt	0x0: Disable CO_NEG3 Interrupt 0x1: Enable CO_NEG3 Interrupt
ECO_NEG_2	1	Enable COUT2 Negative Transition Interrupt	0x0: Disable CO_NEG2 Interrupt 0x1: Enable CO_NEG2 Interrupt
ECO_NEG_1	0	Enable COUT1 Negative Transition Interrupt	0x0: Disable CO_NEG1 Interrupt 0x1: Enable CO_NEG1 Interrupt

CONTROL (0x14)

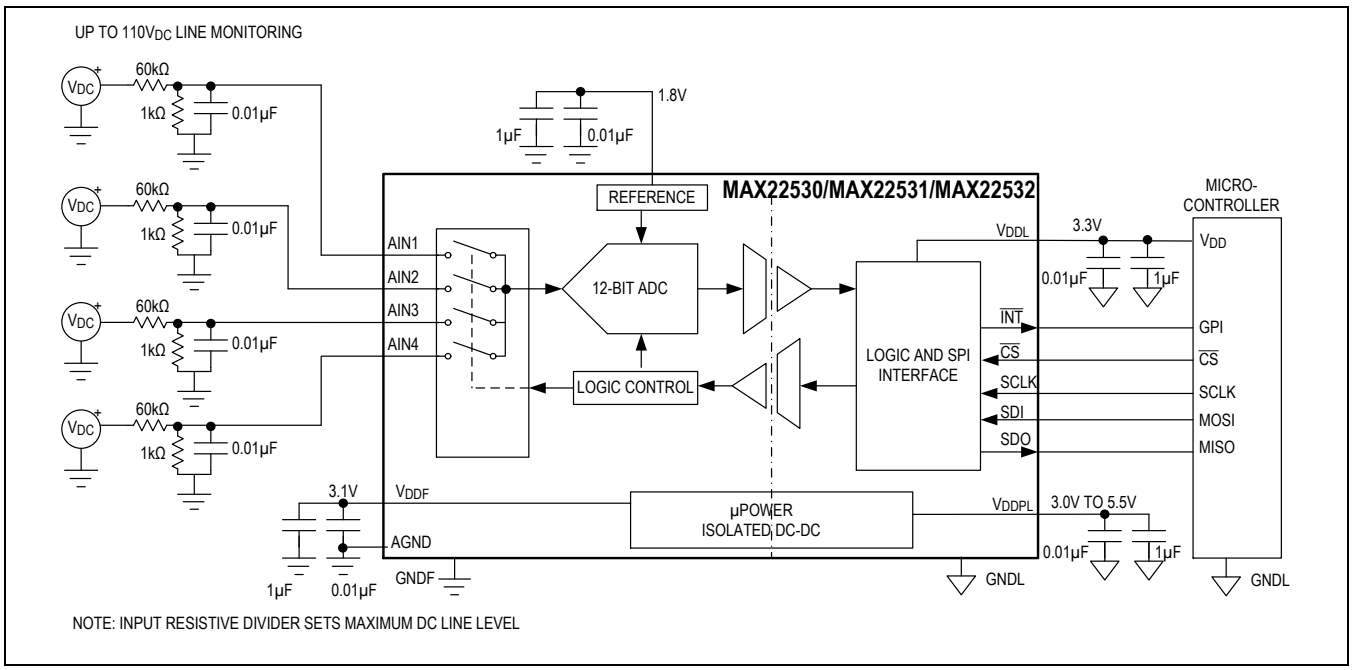
Control Register

BIT	15	14	13	12	11	10	9	8
Field	ENCRC	ECOM	–	–	–	–	–	–
Reset	0b0	0b0	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	FLT_CLR_4	FLT_CLR_3	FLT_CLR_2	FLT_CLR_1	DISPWR	CLRPOR	SRES	REST
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

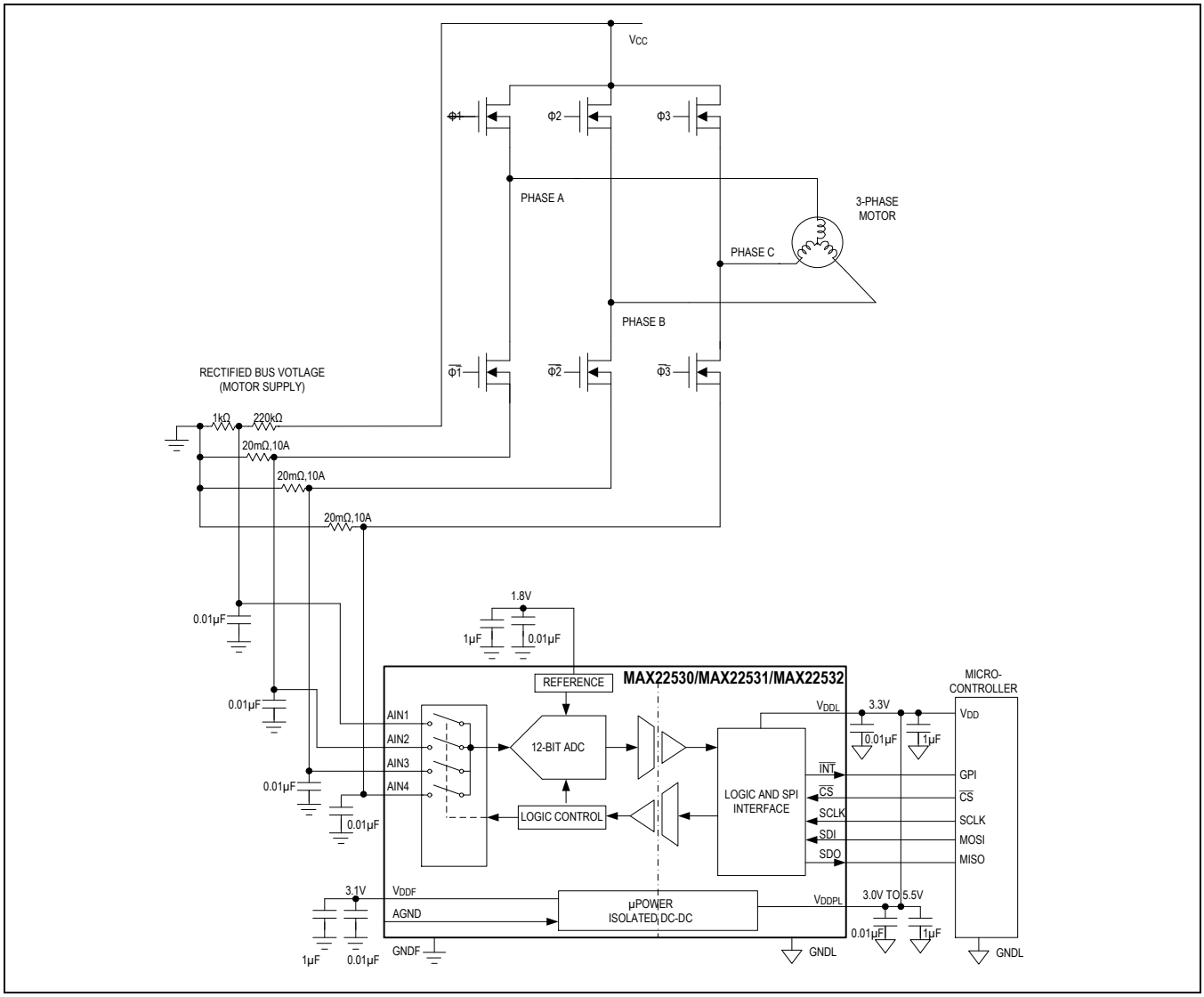
BITFIELD	BITS	DESCRIPTION	DECODE
ENCRC	15	Enable SPI CRC	0x0: CRC not used (24-bit SPI transactions) 0x1: CRC used (32-bit SPI transactions)
ECOM	14	Enable Common High and Low Thresholds for all Channels	0x0: Each threshold needs to be individually programmed 0x1: All comparators use COUTHI1 and COUTLO1 as threshold values
FLT_CLR_4	7	Clear ADC4 Moving Average Filter	0x0: Normal operation 0x1: Clear ADC4 filter
FLT_CLR_3	6	Clear ADC3 Moving Average Filter	0x0: Normal operation 0x1: Clear ADC3 filter
FLT_CLR_2	5	Clear ADC2 Moving Average Filter	0x0: Normal operation 0x1: Clear ADC2 filter
FLT_CLR_1	4	Clear ADC1 Moving Average Filter	0x0: Normal operation 0x1: Clear ADC1 filter
DISPWR	3	Disable Field Power VDDF	0x0: Normal Operation, Enable Field Power VDDF 0x1: Disable Field Power VDDF
CLRPOR	2	Clear POR bit	0x0: No action 0x1: Clear POR bit in PROD_ID Register
SRES	1	Soft Reset (Reset Logic Core & Registers)	0x0: Normal Operation 0x1: Soft Reset Enabled (Self-Clearing)
REST	0	Hard Reset (including field supply power off)	0x0: Normal Operation 0x1: Hard Reset (Self-Clearing)

Typical Application Circuits

High-Voltage DC Monitoring



3-Phase Motor Low Side Monitoring



Ordering Information

PART NUMBER	ISOLATION RATING (V_{RMS})	# OF COUT PINS	PIN-PACKAGE
MAX22530AWE+	5000	0	16-pin WSOIC
MAX22531AAP+	3500	2	20-pin SSOP
MAX22532AAI+*	3500	4	28-pin SSOP

**Future product–contact Maxim for availability.*

+ Denotes lead (Pb)-free/RoHS compliance.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/21	Release for Market Intro	—
1	9/21	Updated *General Description* section, *Safety Regulatory Approvals* section, Insulation Characteristics table, and *Ordering Information* table; added *Digital Isolation* section	1, 7, 8, 21, 36

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