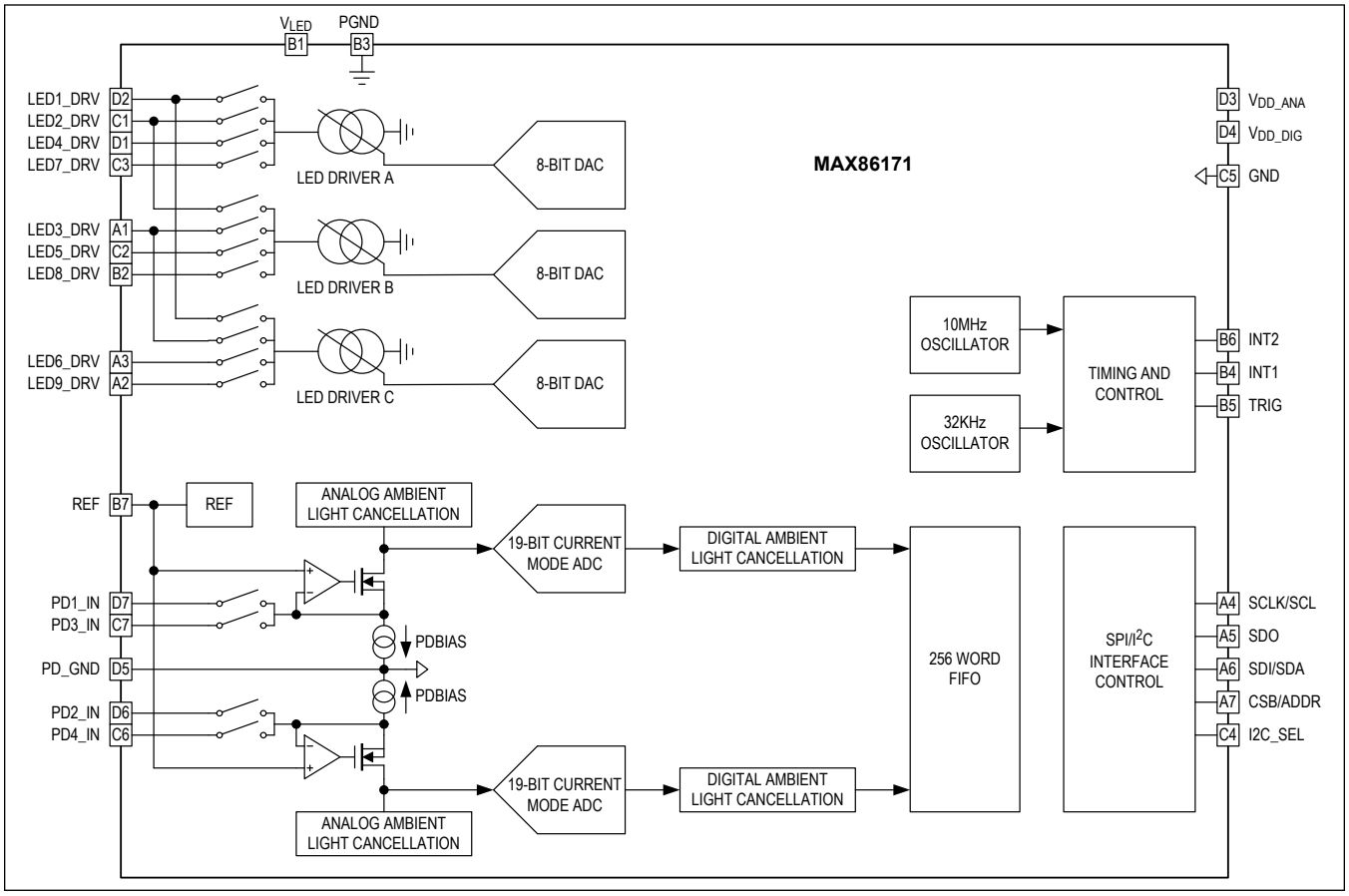
Simplified Block Diagram



Absolute Maximum Ratings

V_{DD_ANA}, V_{DD_DIG} to GND ..... -0.3V to +2.2V
V_{LED} to PGND..... -0.3V to +6.0V
PGND to GND ..... -0.3V to +0.3V
PDx_IN to GND ..... -0.3V to +2.2V
PD_GND to GND..... -0.3V to +0.3V
VREF to GND ..... -0.3V to +2.2V
LEDx_DRV to PGND.....-0.3V to V_{LED} + 0.3V
SDO to GND..... -0.3V to V_{DD} + 0.3V
SDI/SDA, SCLK/SCL, CSB/ADDR, I2C_SEL, INT1, INT2, TRIG to GND..... -0.3V to +6.0V
Output Short-Circuit Duration.....Continuous
Continuous Input Current Into Any Pin (except LEDx_DRV Pins).....±50mA
Continuous Power Dissipation (WLP) (derate 27.24mW/°C above +70°C).....357mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-40°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28-BUMP WLP

Package Code	N281A2+1
Outline Number	21-100259
Land Pattern Number	Refer to *Application Note 1891*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	58.01°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16µA, FR_CLK_SEL = 0, FR_CLK_DIV = 32 (F_{FRAME} = 1kfps), MEASx_TINT = 14.6µs, MEASx_LED_SETLNG = 6µs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
READOUT CHANNEL						
ADC Resolution				19.5		Bits
ADC INL	INL_{RX}	MEASx_TINT = 117.1µs		±10		LSB
		MEASx_TINT = 14.6µs		±40		
ADC DNL	DNL_{RX}	MEASx_TINT = 117.1µs		±3		LSB
		MEASx_TINT = 14.6µs		±10		
ADC Full-Scale Input Current	I_{FS}	MEASx_PPGy_ADC_RGE = 0x0		4.0		µA
		MEASx_PPGy_ADC_RGE = 0x1		8.0		
		MEASx_PPGy_ADC_RGE = 0x2		16.0		
		MEASx_PPGy_ADC_RGE = 0x3		32.0		

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16µA, FR_CLK_SEL = 0, FR_CLK_DIV = 32 (F_{FRAME} = 1kfps), MEASx_TINT = 14.6µs, MEASx_LED_SETLNG = 6µs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Average V_{DD} Supply Current	I_{DD}	One Meas/Frame, MEASx_TINT = 14.6µs, MEASx_LED_RGE = 128mA, MEASx_DRVy_PA = 0x7F, FR_CLK_SEL = 1, PPG1_PWRDN = 0, PPG2_PWRDN = 1	FR_CLK_DIV = 64, Frame Rate = 512fps		120	160	µA
			FR_CLK_DIV = 512, Frame Rate = 64fps		24		
			FR_CLK_DIV = 4096, Frame Rate = 8fps		5		
		Four Meas/Frame, MEASx_TINT = 14.6µs, MEASx_LED_RGE = 128mA, MEASx_DRVy_PA = 0x7F, FR_CLK_SEL = 1, PPG1_PWRDN = 0, PPG2_PWRDN = 1	FR_CLK_DIV = 64, Frame Rate = 512fps		373	448	
			FR_CLK_DIV = 512, Frame Rate = 64fps		48.5		
			FR_CLK_DIV = 4096, Frame Rate = 8fps		8.2		
		One Meas/Frame, MEASx_TINT = 14.6µs, MEASx_LED_REG = 128mA, MEASx_DRVy_PA = 0x7F, FR_CLK_SEL = 1, PPG1_PWRDN = 0, PPG2_PWRDN = 0	FR_CLK_DIV = 64, Frame Rate = 512fps		170	210	
			FR_CLK_DIV = 512, Frame Rate = 64fps		28		
			FR_CLK_DIV = 4096, Frame Rate = 8fps		5.5		
		Four Meas/Frame, MEASx_TINT = 14.6µs, MEASx_LED_RGE = 128mA, MEASx_DRVy_PA = 0x7F, FR_CLK_SEL = 1, PPG1_PWRDN = 0, PPG2_PWRDN = 0	FR_CLK_DIV = 64, Frame Rate = 512fps		532	672	
			FR_CLK_DIV = 512, Frame Rate = 64fps		71		
			FR_CLK_DIV = 4096, Frame Rate = 8fps		9.7		

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16µA, FR_CLK_SEL = 0, FR_CLK_DIV = 32 (F_{FRAME} = 1kfps), MEASx_TINT = 14.6µs, MEASx_LED_SETLNG = 6µs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Average V_{LED} Supply Current	I_{LED}	One LED/Frame, MEASx_LED_RGE = 128mA, MEASx_DRVy_PA = 0x7F, MEASx_TINT = 14.6µs, MEASx_LED_SETLNG = 1, FR_CLK_SEL = 1, PPG1_PWRDN = 0, PPG2_PWRDN = 1	FR_CLK_DIV = 64, Frame Rate = 512fps		870		µA
			FR_CLK_DIV = 512, Frame Rate = 64fps		85		
			FR_CLK_DIV = 4096, Frame Rate = 8fps		10.6		
V_{DD} Current in Shutdown		T_A = +25°C			0.85	3	µA
V_{LED} Current in Shutdown		T_A = +25°C				0.5	µA
DIGITAL I/O CHARACTERISTICS							
Input Voltage Low	V_{IL}	I2C_SEL, CSB/ADDR, SDI/SDA, SCLK/SCL, TRIG				0.4	V
Input Voltage High	V_{IH}	I2C_SEL, CSB/ADDR, SDI/SDA, SCLK/SCL, TRIG		1.4			V
Input Hysteresis	V_{HYS}	I2C_SEL, CSB/ADDR, SDI/SDA, SCLK/SCL, TRIG			430		mV
Input Capacitance	C_{IN}	I2C_SEL, CSB/ADDR, SDI/SDA, SCLK/SCL, TRIG			10		pF
Input Leakage Current	I_{IN}	I2C_SEL, CSB/ADDR, SDI/SDA, SCLK/SCL, TRIG, T_A = +25°C, V_{IN} = 0V or 1.8V		-1	+0.01	+1	µA
Output-Low Voltage	V_{OL}	SDO, INT1, INT2, SDI/SDA (in I^2C mode), I_{SINK} = 4mA				0.4	V
Output-High Voltage	V_{OH}	SDO, INT1, INT2, I_{SOURCE} = 4mA		V_{DD} - 0.4			V
Open-Drain Output-Low Voltage	V_{OL_OD}	INT1_OCFG = INT2_OCFG = 0x0, I_{SINK} = 4mA				0.4	V
SPI TIMING CHARACTERISTICS (Note 4)							
SCLK Frequency	f_{SCLK}					25	MHz
SCLK Period	t_{CP}			40			ns
SCLK Pulse-Width High	t_{CH}			18			ns
SCLK Pulse-Width Low	t_{CL}			18			ns
CSB Fall-to-SCLK Rise Setup Time	t_{CSS0}	Applies to 1st SCLK rising edge after CSB goes low		20			ns
CSB Fall-to-SCLK Rise Hold Time	t_{CSH0}	Applies to inactive rising edge preceding 1st rising edge		5			ns

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16µA, FR_CLK_SEL = 0, FR_CLK_DIV = 32 (F_{FRAME} = 1kfps), MEASx_TINT = 14.6µs, MEASx_LED_SETLNG = 6µs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Last SCLK Rise to CSB Rise	t_{CSH1}	Applies to last SCLK rising edge in a transaction	20			ns
Last SCLK Rise to Next CSB Fall	t_{CSF}	Applies to last SCLK rising edge to next CSB falling edge (new transaction)	60			ns
CSB Pulse-Width High	t_{CSPW}		40			ns
SDI to SCLK Rise Setup Time	t_{DS}		5			ns
SDI to SCLK Rise Hold Time	t_{DH}		5			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 30pF			15	ns
CSB Fall to SDO Enabled	t_{DOE}	C_{LOAD} = 0pF	10			ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable Time			5	ns
I²C TIMING CHARACTERISTICS (Note 4)						
I²C Write Address		ADDR = 0		C8		HEX
		ADDR = 1		CA		
I²C Read Address		ADDR = 0		C9		HEX
		ADDR = 1		CB		
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free-Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time START and Repeat START Condition	t_{HD_STA}		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	t_{SU_STA}		0.6			µs
Data Hold Time	t_{HD_DAT}		0		900	ns
Data Setup Time	t_{SU_DAT}		100			ns
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs
Pulse-Width of Suppressed Spike	t_{SP}		0		50	ns
Bus Capacitance	CB				400	pF
SDA and SCL Receiving Rise Time	t_R		20 + 0.1CB		300	ns
SDA and SCL Receiving Fall Time	t_F		20 + 0.1CB		300	ns

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16µA, FR_CLK_SEL = 0, FR_CLK_DIV = 32 (F_{FRAME} = 1kfps), MEASx_TINT = 14.6µs, MEASx_LED_SETLNG = 6µs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Transmitting Fall Time	t_{TF}		20 + 0.1CB		300	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated's bench or proprietary automated test equipment (ATE) characterization.

Note 2: Definitions of terms:
1. Frame = All measurements made during a particular wake-up interval.
2. Measurement = Ambient light corrected output.

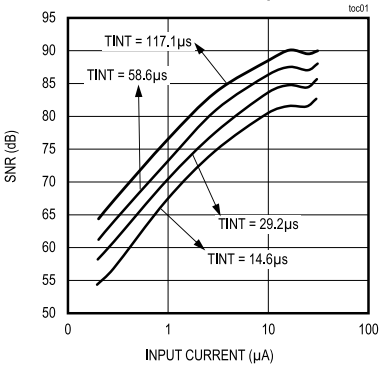
Note 3: All other register settings assumed to be PORb defaults, unless otherwise noted.

Note 4: For design guidance only. Not production tested.

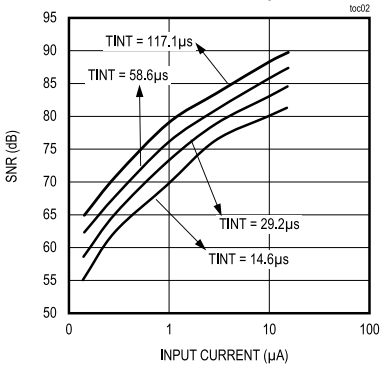
Typical Operating Characteristics

(V_{DD} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, unless otherwise noted.)

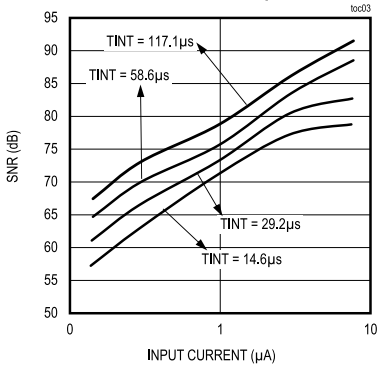
SNR vs. INPUT CURRENT
ADC RANGE = 32µA



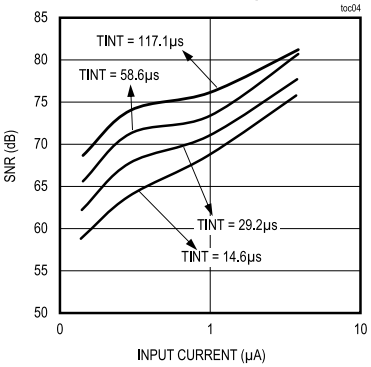
SNR vs. INPUT CURRENT
ADC RANGE = 16µA



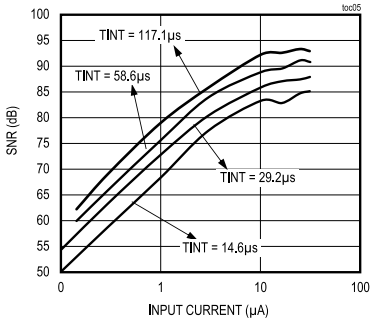
SNR vs. INPUT CURRENT
ADC RANGE = 8µA



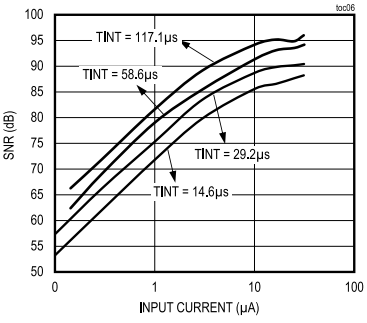
SNR vs. INPUT CURRENT
ADC RANGE = 4µA



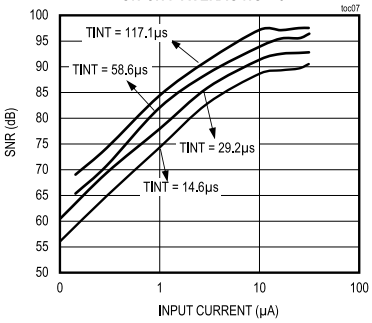
SNR vs. INPUT CURRENT
ADC RANGE = 32µA
ON-CHIP AVERAGING = 2



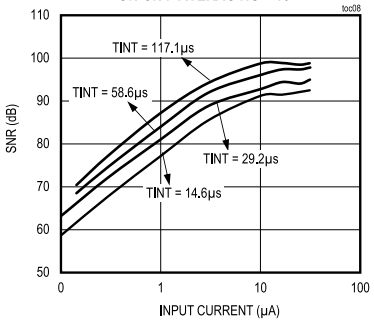
SNR vs. INPUT CURRENT
ADC RANGE = 32µA
ON-CHIP AVERAGING = 4



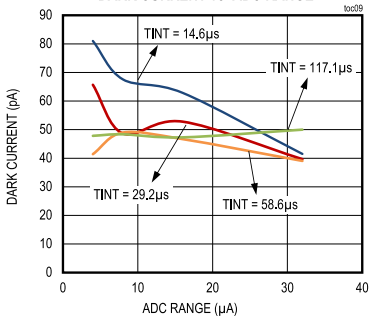
SNR vs. INPUT CURRENT
ADC RANGE = 32µA
ON-CHIP AVERAGING = 8



SNR vs. INPUT CURRENT
ADC RANGE = 32µA
ON-CHIP AVERAGING = 16



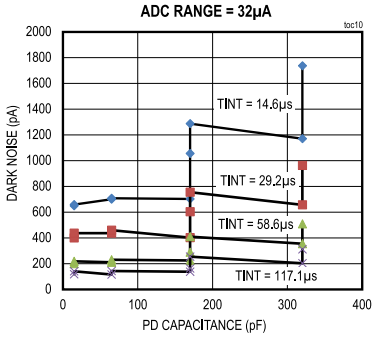
DARK CURRENT vs. ADC RANGE



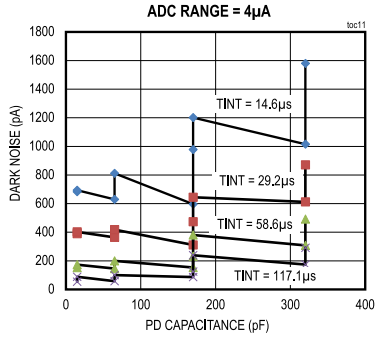
Typical Operating Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, unless otherwise noted.)

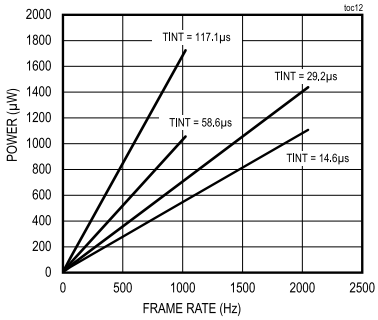
INPUT REFERRED NOISE vs. PD CAPACITANCE
ADC RANGE = 32µA



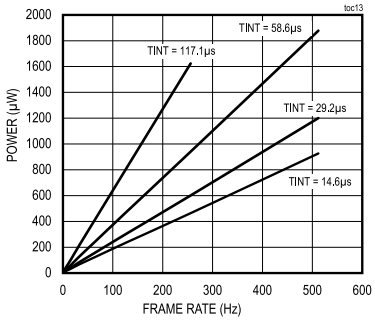
INPUT REFERRED NOISE vs. PD CAPACITANCE
ADC RANGE = 4µA



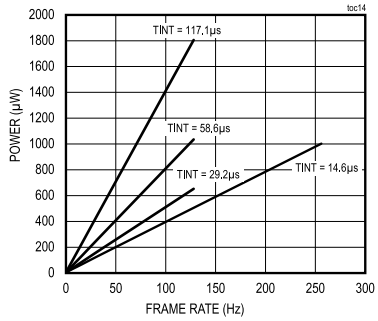
AFE POWER DISSIPATION
1 MEASUREMENT/FRAME



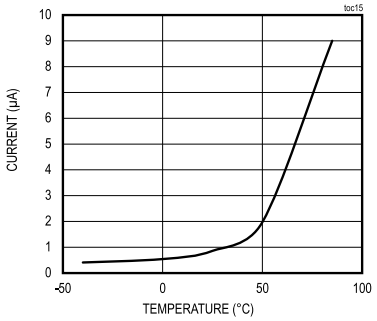
AFE POWER DISSIPATION
4 MEASUREMENTS/FRAME



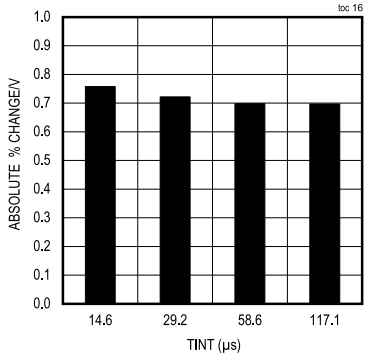
AFE POWER DISSIPATION
9 MEASUREMENTS/FRAME



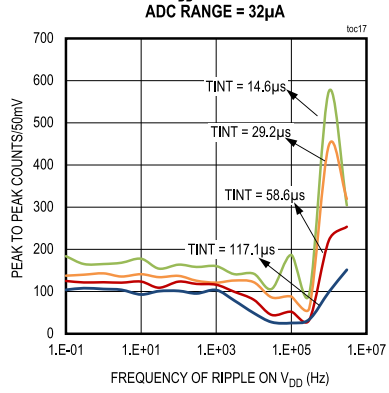
AVERAGE V_{DD} SHUTDOWN CURRENT



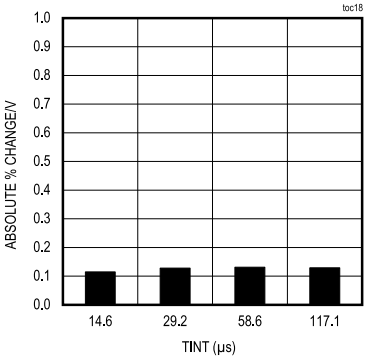
V_{DD} DC PSRR
PD CURRENT = 31µA



V_{DD} AC PSRR
ADC RANGE = 32µA

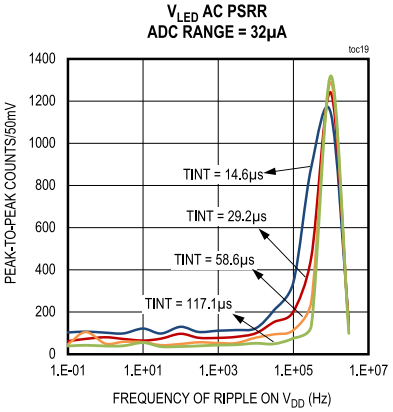


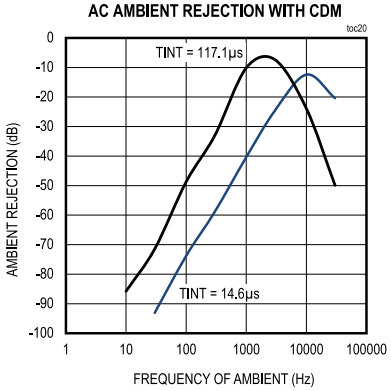
V_{LED} DC PSRR
PD CURRENT = 31µA

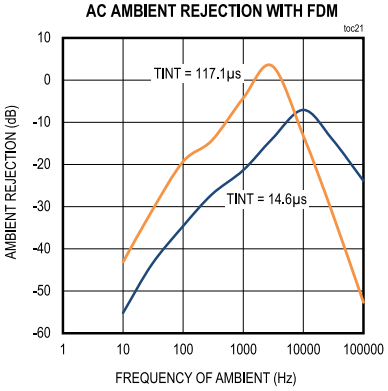


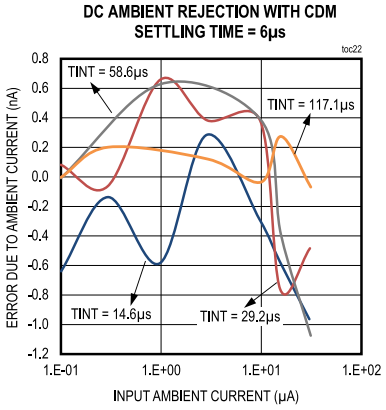
Typical Operating Characteristics (continued)

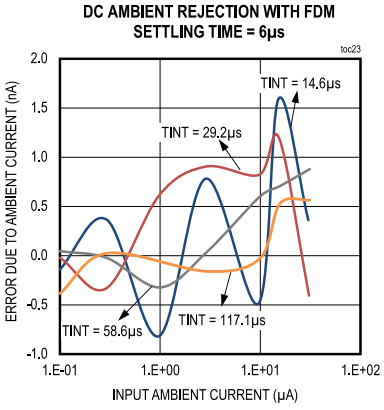
(V_{DD} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, unless otherwise noted.)





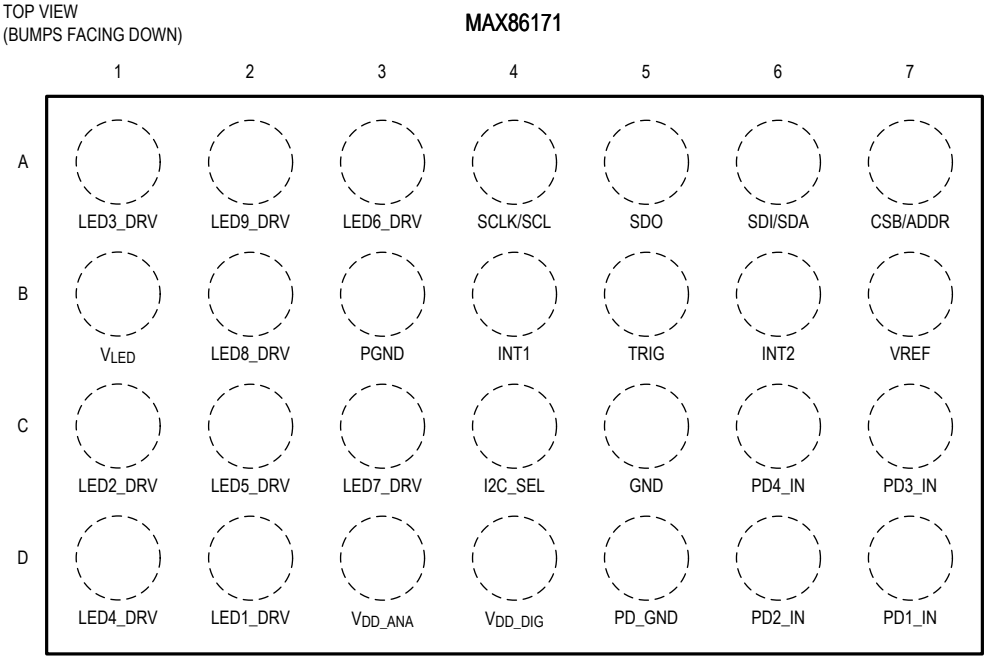






Pin Configuration

MAX86171



WLP
(7x4, 0.35mm Pitch)

Pin Description

PIN	NAME	FUNCTION
POWER		
D3	V_{DD_ANA}	Analog Power Supply. Connect to an externally regulated supply. Bypass to GND with a 0.1µF and 10µF capacitor as close to the bump as possible.
D4	V_{DD_DIG}	Digital Power Supply. Connect to an externally regulated supply. Bypass to GND with a 0.1µF and 10µF capacitor as close to the bump as possible.
C5	GND	Main Power Supply Return. Connect to PCB Ground. Refer to the *PCB Layout Guidelines Section* for more information.
B1	V_{LED}	LED Power Supply Input. In a configuration with more than one LED supply, connect V_{LED} to the highest LED supply voltage. Bypass with a 10µF capacitor to PGND.
B3	PGND	LED Power Return. Connect to PCB Ground. Refer to the *PCB Layout Guidelines Section* for more information.
CONTROL INTERFACE		
A4	SCLK/SCL	SPI Clock/I^2C Clock
A5	SDO	SPI Data Output. Tie to GND or V_{DD} when this pin is not used.
A6	SDI/SDA	SPI Data Input/I^2C Data
A7	CSB/ADDR	SPI Chip Select Input/I^2C Device Address Selector.
C4	I2C_SEL	Input to Select I^2C or SPI Mode. When I2C_SEL is active (high) the interface operates in I^2C mode. When I2C_SEL is inactive (low) the interface operates in SPI mode.

Pin Description (continued)

PIN	NAME	FUNCTION
B5	TRIG	External Clock or Start of Conversion Trigger Input. Tie to GND or V_{DD} when this pin is not used.
B6	INT2	Interrupt 2 Output. When not used, this pin can be left unconnected.
B4	INT1	Interrupt 1 Output. When not used, this pin can be left unconnected.
OPTICAL PINS		
D7	PD1_IN	Photodiode Cathode Input. PPG1_PDSEL = 0. When not used, this pin can be left unconnected.
D6	PD2_IN	Photodiode Cathode Input. PPG2_PDSEL = 0. When not used, this pin can be left unconnected.
C7	PD3_IN	Photodiode Cathode Input. PPG1_PDSEL = 1. When not used, this pin can be left unconnected.
C6	PD4_IN	Photodiode Cathode Input. PPG2_PDSEL = 1. When not used, this pin can be left unconnected.
D5	PD_GND	Photodiode Anode. Star connect to PCB Ground near the MAX86171. Use the PD_GND node to shield the PDx_IN nodes.
D2	LED1_DRV	LED Output Pin 1. Driven from LED driver A and C. Connect the LED cathode to LED1_DRV and its anode to the V_{LED} supply. When not used, this pin can be left unconnected.
C1	LED2_DRV	LED Output Pin 2. Driven from LED driver A and B. Connect the LED cathode to LED2_DRV and its anode to the V_{LED} supply. When not used, this pin can be left unconnected.
A1	LED3_DRV	LED Output Pin 3. Driven from LED driver B and C. Connect the LED cathode to LED3_DRV and its anode to the V_{LED} supply. When not used, this pin can be left unconnected.
D1	LED4_DRV	LED Output Pin 4. Driven from LED driver A. Connect the LED cathode to LED4_DRV and its anode to the V_{LED} supply. When not used, this pin can be left unconnected.
C2	LED5_DRV	LED Output Pin 5. Driven from LED driver B. Connect the LED cathode to LED5_DRV and its anode to the V_{LED} supply. When not used, this pin can be left unconnected.
A3	LED6_DRV	LED Output Pin 6. Driven from LED driver C. Connect the LED cathode to LED6_DRV and its anode to the V_{LED} supply. When not used, this pin can be left unconnected.
C3	LED7_DRV	LED Output Pin 7. Driven from LED driver A. Connect the LED cathode to LED7_DRV and its anode to the V_{LED} supply. When not used, this pin can be left unconnected.
B2	LED8_DRV	LED Output Pin 8. Driven from LED driver B. Connect the LED cathode to LED8_DRV and its anode to the V_{LED} supply. When not used, this pin can be left unconnected.
A2	LED9_DRV	LED Output Pin 9. Driven from LED driver C. Connect the LED cathode to LED9_DRV and its anode to the V_{LED} supply. When not used, this pin can be left unconnected.
REFERENCE		
B7	VREF	Internal Reference Decoupling Point. Bypass with a 1µF capacitor to PCB Ground.

Detailed Description

The MAX86171 is a complete integrated optical data-acquisition system, ideal for various applications including optical pulse-oximetry and heart-rate detection applications. It is designed for the demanding requirements of mobile and wearable devices and requires minimal external hardware components for integration into a wearable device. It includes high-resolution optical readout signal processing channels with robust ambient light cancellation and high current LED driver DACs to form a complete optical readout signal chain.

The MAX86171 is fully adjustable through software registers and the digital output data is stored in a 256-word FIFO. The FIFO allows the MAX86171 to be connected to a microcontroller or processor on a shared bus, I^2C, or SPI depending on hardware selection on the I2C_SEL pin. It operates in fully autonomous mode for low-power battery applications. For wearables with compact optical architectures, refer to MAX86170A and MAX86170B that can support 6/4 LEDs and 4/2 PDs.

The MAX86171 incorporates dual optical readout channels that operate simultaneously. The MAX86171 has three LED drivers. With the built-in MUX and control logic on the chip, the MAX86171 can support up to Nine LEDs and Four PDs. It is well suited for a wide variety of optical sensing applications.

The MAX86171 operates on a 1.8V main supply voltage, with a separate 3.1V to 5.5V LED driver power supply. This device has flexible exposure, timing, and shutdown configurations as well as control of individual blocks so that an optimized measurement can be made at minimum power levels.

Optical Transmitter Overview

The MAX86171 has three independent precision LED current drivers that are muxed to Nine LED driver pins. Three LED current DACs modulate LED pulses for a variety of optical measurements. The three LED current DACs have an 8-bit dynamic range with four programmable full-scale range settings of 32mA, 64mA, 96mA, and 128mA. The three current drivers, DRVA, DRVB, and DRVC, is connected to four of the LED driver pins through a mux according to Table 1. The MEASx Selects registers define how each LED driver is connected for that particular measurement. Thus, the configuration of the LED drivers can be uniquely set for each measurement. Each measurement can drive one, two, or all three LED drivers.

Table 1. LED DRIVER AND LED MUX CONFIGURATION

MEASx_DRVA		MEASx_DRVB		MEASx_DRVC	
Code	**LEDx_DRV Pin**	**Code**	**LEDx_DRV Pin**	**Code**	**LEDx_DRV Pin**
00	LED1_DRV	00	LED2_DRV	00	LED1_DRV
01	LED2_DRV	01	LED3_DRV	01	LED3_DRV
10	LED4_DRV	10	LED5_DRV	10	LED6_DRV
11	LED7_DRV	11	LED8_DRV	11	LED9_DRV

This configuration of LED driver and LED mux is highly flexible, allowing for any of the Nine LED driver pins to sink up to 128mA. Additionally LED1_DRV, LED2_DRV, and LED3_DRV can combine two LED drivers to get a total of 256mA per pin in a given measurement. Table 2 also lists which of the three LED drivers can be connected to which of the Nine LED driver pins.

Table 2. LED DRIVERS TO LED_DRV PIN MAPPING

	LED1_DRV	**LED2_DRV**	**LED3_DRV**	**LED4_DRV**	**LED5_DRV**	**LED6_DRV**	**LED7_DRV**	**LED8_DRV**	**LED9_DRV**
LED Driver A	x	x		x			x		
LED Driver B		x	x		x			x	
LED Driver C	x		x			x			x

Table 2. LED DRIVERS TO LED_DRV PIN MAPPING (continued)

	LED1_DRV	LED2_DRV	LED3_DRV	LED4_DRV	LED5_DRV	LED6_DRV	LED7_DRV	LED8_DRV	LED9_DRV
Total Possible Driver	2	2	2	1	1	1	1	1	1
Total Possible Max Current (mA)	256	256	256	128	128	128	128	128	128

The three LED current DAC/Mux combinations are low-dropout current sources allowing for low-noise, power-supply independent LED currents to be sourced at the lowest supply voltage possible; thus, minimizing LED power consumption. The four full-scale range settings are provided to allow for a trade-off between LED driver noise, V_{LED} power supply rejection, and dropout voltage on the pins. Table 3 illustrates this trade-off.

Table 3. LED DRIVER FULL-SCALE RANGE TRADE-OFF

FULL-SCALE RANGE (mA)	LED DAC RESOLUTION LED CURRENT FOR 1 LSB (mV)	RECOMMENDED MINIMUM V_{LEDx_DRV} (mV)	PEAK LOOP-BACK SNR (dB)
32	0.125	300	84
64	0.250	500	88
96	0.375	700	90
128	0.500	900	91

Optical Receiver Overview

The optical path in MAX86171 is composed of a front-end photodiode biasing circuit with an analog ambient light cancellation (ALC) sample and hold circuit that nulls the ambient light photodiode current at the input of the ADC. This front-end biasing circuit is followed by a current integrating, continuous-time sigma-delta ADC with a proprietary discrete time filter. This discrete time filter uses multiple dark and exposure optical samples to generate an accurate 20-bit effective exposure output signal with excellent low- and high-frequency ambient light rejection.

This combination of analog circuits and back-end digital filtering helps reduce shifts due to ambient light variations. An exposure signal varies less than 0.5nA, on a homogenous photodiode with ambient light variations from 0µA to over 30µA, or over 95dB of DC rejection, all but eliminating issues in high-intensity outdoor lighting conditions. This level of ambient light cancellation is maintained under indoor lighting conditions with over 70dB of rejection at line (mains) rate, 100Hz and 120Hz. In addition back-end filtering also suppresses the high rate of modulation of newer compact fluorescent and LED lighting as well.

The MAX86171 incorporates dual optical-signal paths and has Four PD input pins. Configured by MEASx_PPGy_PDSEL (x = 1...9, y = 1, 2) in each measurement, the on-chip mux switches two of four PDs to these two independent optical signal paths so that two PDs are able to operate simultaneously. Refer to Figure 1.

Each optical signal path supports four full-scale range settings of 4µA, 8µA, 16µA, and 32µA set in the MEASx_PPGy_ADC_RGE (x = 1 to 9, y = 1, 2) field. Also supported are four options of integration times, which effectively modulate the optical channel bandwidth, allowing for a trade-off between light energy consumed and PPG signal quality. Each optical signal path also incorporates a 2-bit offset DAC for extending the optical dynamic range. This is especially useful under certain conditions that occur when attempting to limit the exposure LED current level (red shift in SpO_2 for example). The optical paths also support multiple photodiode and LED settling times in order to support flexible multiparameter measurements for different types of photodiode/LED wavelength combinations.

Most significantly, each MAX86171 signal path supports up to nine unique combinations of the above configurations to be defined and easily enabled and disabled as needed; the goal is to allow a single optical AFE to support multiple optical measurements in a compact, energy efficient design.

The MAX86171 supports both internally timed frame rates and externally triggered frames. The internally timed frame

rate uses an on-chip generated 32768Hz/32000Hz clock from a low-power oscillator paired with a programmable divider. Frame rates of 32768/N or 32000/N where N = 11 to 32786 are directly programmable. The on-chip oscillator can also be fine tuned (register 0x15) to support thermal compensation. In addition, the MAX86171 allows for externally defined frame rates with either an external frame trigger input or an external 32768Hz/32000Hz clock input and the on-chip divider.

The MAX86171 operates in a dynamic power-down mode, always powering down between frames; thus, minimizing power consumption. For more details on the power consumption at various frame rates, refer to the *Electrical Characteristics* table.

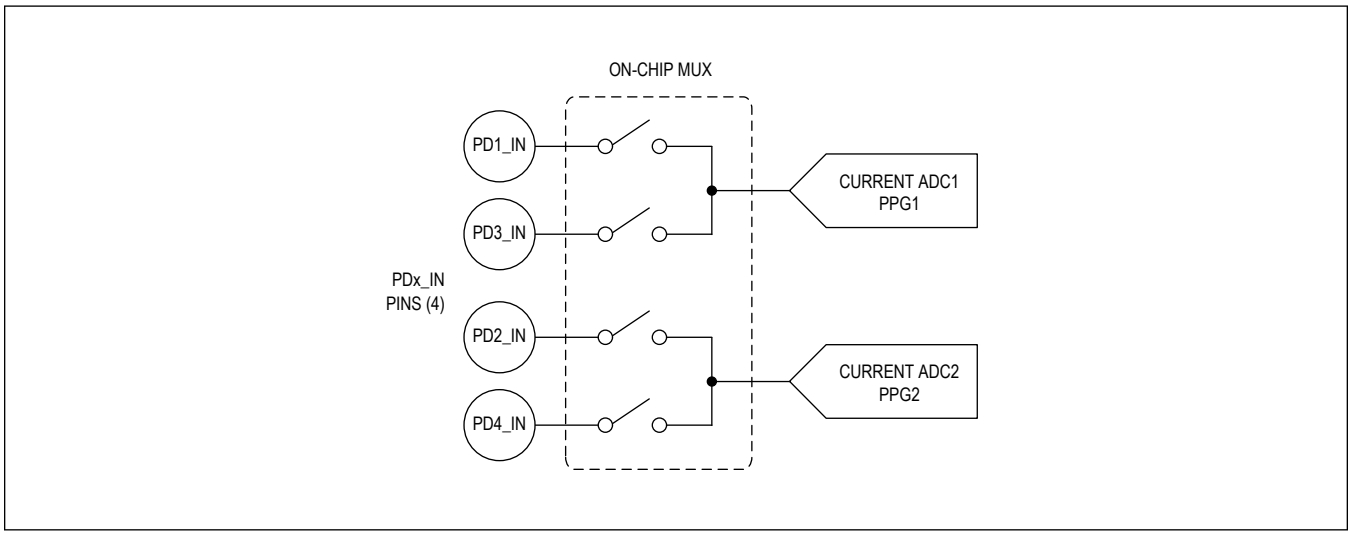


Figure 1. On-Chip Mux for the PDx_IN Pins

Synchronization Modes

The MAX86171 supports three modes of frame rate controls. These are internally timed frame rates through an internal oscillator and divider, externally timed frame rates through an external frame trigger input, and externally timed frame rates through an external frame timing clock and the internal frame clock divider.

SYNC_MODE = 0x0 Internal Frame Oscillator and Divider Mode

SYNC_MODE = 0x0 is the free running mode of operation. In this mode, the MAX86171 uses the internal frame rate oscillator (f_{FRAME_CLK}) and the internal user programmable divider (FR_CLK_DIV) to set the time between measurement instances or the frame rate. The FR_CLK_DIV register can be set to any value between 11 and 32768; thus, allowing a large variety of frame rates to be programmed. In addition, the internal oscillator (f_{FRAME_CLK}) can be set to one of two primary values, 32000Hz with the FR_CLK_SEL bit = 0 or 32768Hz with the FR_CLK_SEL bit = 1. This feature allows additional flexibility in the user-defined frame rate.

The MAX86171 also offers a fine adjust feature (FR_CLK_FINE_TUNE), which can be used in combination with a highly stable crystal-based real-time clock (RTC) oscillator in the host microcontroller to trim out the drift of the on-chip f_{FRAME_CLK} oscillator. By counting the time between MAX86171 generated interrupts using the microcontroller based RTC, it is possible to compute the error in the f_{FRAME_CLK} oscillator and trim that error to within ±0.2% of the microcontroller based RTC.

SYNC_MODE = 0x1 External Frame Trigger Input Mode

SYNC_MODE = 0x1 enables the TRIG input pin to be a start for frame sync signal. On either the falling edge (TRIG_ICFG = 0) or the rising edge (TRIG_ICFG = 1) of the TRIG input, the MAX86171 begins a measurement frame. This frame includes powering up and then executing each enabled measurement from MEAS1 to MEAS9.

SYNC_MODE = 0x2 External Frame Clock Input

SYNC_MODE = 0x2 enables the TRIG input to be an external frame clock input. This input clock effectively replaces

the MAX86171 internal frame clock (f_{FRAME_CLK}) for the purpose of setting the time between start of frame wake-up periods. The MAX86171 uses the FR_CLK_DIV register value to divide this external clock input in order to generate the start of frame wake-up period. However, the stability of frame rate is driven entirely by the external frame clock input.

This mode is useful when the microcontroller can output a 32kHz crystal-based clock. This mode can also be used to lock other sensors together through this same oscillator.

Photodiode Biasing

The MAX86171 provides three photodiode biasing options to support a large range of photodiode capacitance. Each photodiode input can have a separate bias setting; thus, allowing for different photodiodes to be accomodated. The PDx_BIAS values adjust the PDx_IN bias point impedance to ensure that the Photodiode settles rapidly enough to support the signal timing.

Table 4. Recommended PD BIAS Values Based on Photodiode Capacitance

PDx_BIAS[1:0]	PHOTODIODE CAPACITANCE (pF)
00	x
01	0 to 125
10	125 to 250
11	250 to 500

x = Do not use

The PDx_BIAS value impacts the dark current noise of the MAX86171. The relationship between PDx_BIAS and noise with increasing Photodiode capacitance is illustrated in TOC10 and TOC11 in the *Typical Operating Characteristics* section. Because of the increased noise with PDx_BIAS setting, the lowest recommended PDx_BIAS value should be used for a given Photodiode capacitance.

Measurement Configuration and Timing

The MAX86171 optical controller is capable of being configured to make a variety of measurements.

The controller can be configured to pulse one, two or three LED drivers sequentially to make measurements at multiple wavelengths as is done in pulse oximetry measurements or simultaneously to drive multiple LEDs as is done with heart rate measurements on the wrist.

Each LED exposure is ambient light compensated. The controller is also configurable to measure the direct ambient level for every exposure. The direct ambient measurement can be used to adjust the LED-drive level to compensate for increased noise levels when high interfering ambient signals are present.

Frame: Frame is a collection of measurements that can have a minimum of 1 measurement and a maximum of 9 measurements.

Frame Rate: This is similar to sampling rate of a system. Frame rate defines how frequently a frame is repeated.

The optical timing diagrams in Figure 2, Figure 3, Figure 4, Figure 5, and Figure 6 illustrate several possible measurement configurations.

Measurement Configuration

A measurement is essentially one optical sample from one or more LEDs in a single channel configuration and two optical samples in a dual channel configuration. MAX86171 supports nine individual measurements, each of which can be configured independently. Each measurement can be configured in the MEASx registers. These registers help set up a varied set of parameters as outlined by the list below.

These parameters can be configured on a per measurement basis:

- Connections of each of the three LED Drivers to one of the Nine LEDx_DRV pins
- Connection of each of two channels to one of two possible PDs on either channel
- LED driver range and drive currents
- LED settling time
- PD settling time

- Number of averages of each measurement
- Ambient rejection scheme (CDM or FDM)
- Decimation filter selection (COI or SINC3)
- ADC integration time
- ADC range for each channel
- DAC offset for each channel

One Measurement: CDM, No Averaging

The optical timing diagram in Figure 2 represents one measurement with only one LED driver active in central difference method (CDM) mode. No averaging is used.

As seen in Figure 2 only MEASn_DRVA is pulsing during the exposure time.

This timing mode would be used when heart rate is being measured with a single LED. In this mode, three conversions (CDM1, CDM2, and CDM3) occur. The two ambient samples, CDM1 and CDM3, are used for ambient light cancellation. The exposure sample CDM2 will appear in the FIFO as a single optical-sampled value after ambient cancellation.

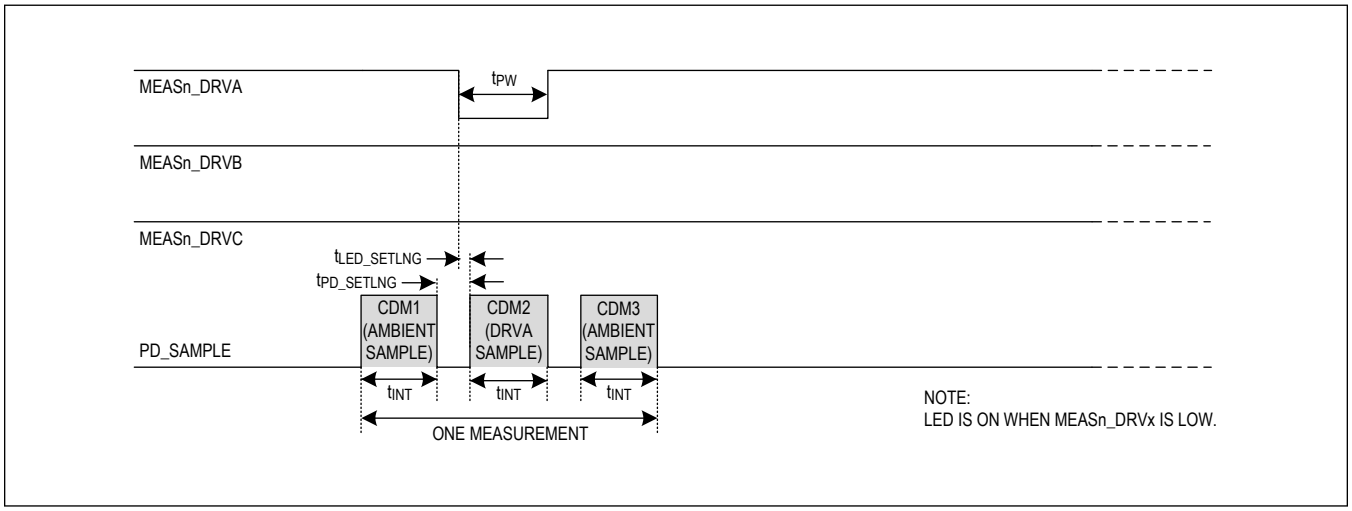


Figure 2. Measurement with CDM

One Measurement with FDM

The optical timing diagram in Figure 3 represents DRVB pulsing with forward difference method (FDM) mode enabled. In this mode, two conversions (FDM1 and FDM2) occur. The ambient sample FDM1 is only used for ambient cancellation. The exposure sample FDM2 appears in the FIFO as a single optical sampled value after ambient cancellation.

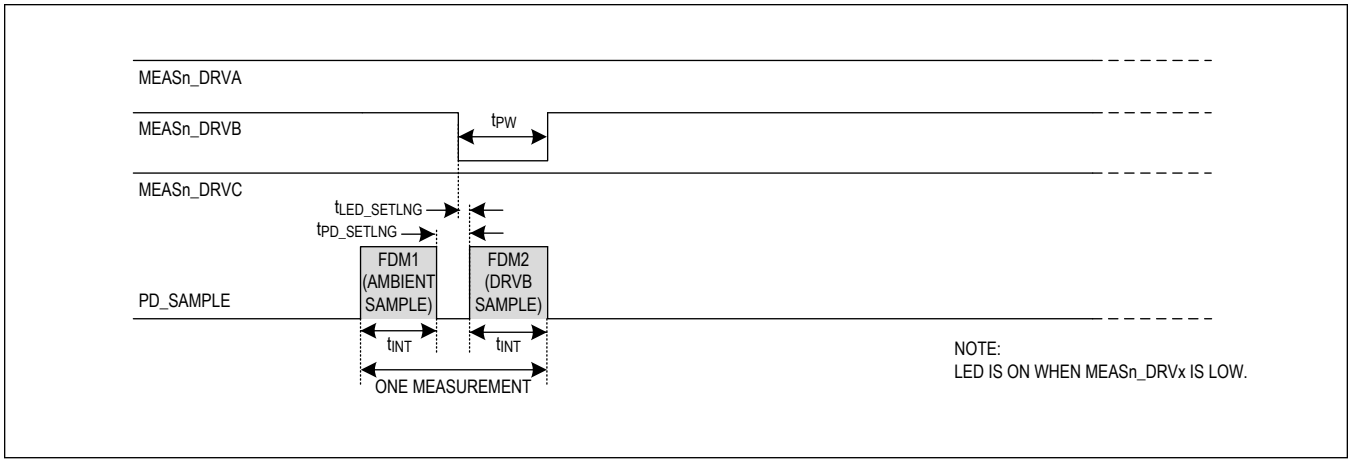


Figure 3. Measurement with FDM

Frame

A frame is a combination of measurements as configured by MEASx_EN (x = 1 to 9). Each frame contains one to nine measurements depending on the register configuration. The frame rate defines how many frames per second (fps). The frame rate is defined by FR_CLK_DIV (register 0x16 and 0x17) or the active edge of TRIG input depending on SYNC_MODE[1:0].

Measurements can be enabled in any order. For example, it is valid to enable MEAS1, MEAS2, and MEAS5 while MEAS3 and MEAS4 are skipped. But if a measurement of direct ambient is configured, then this measurement must be configured as the last measurement in the frame.

Frame with One Measurement Only

Figure 4 represents the timing diagram for one measurement in each frame. This measurement only has one LED driver pulsing.

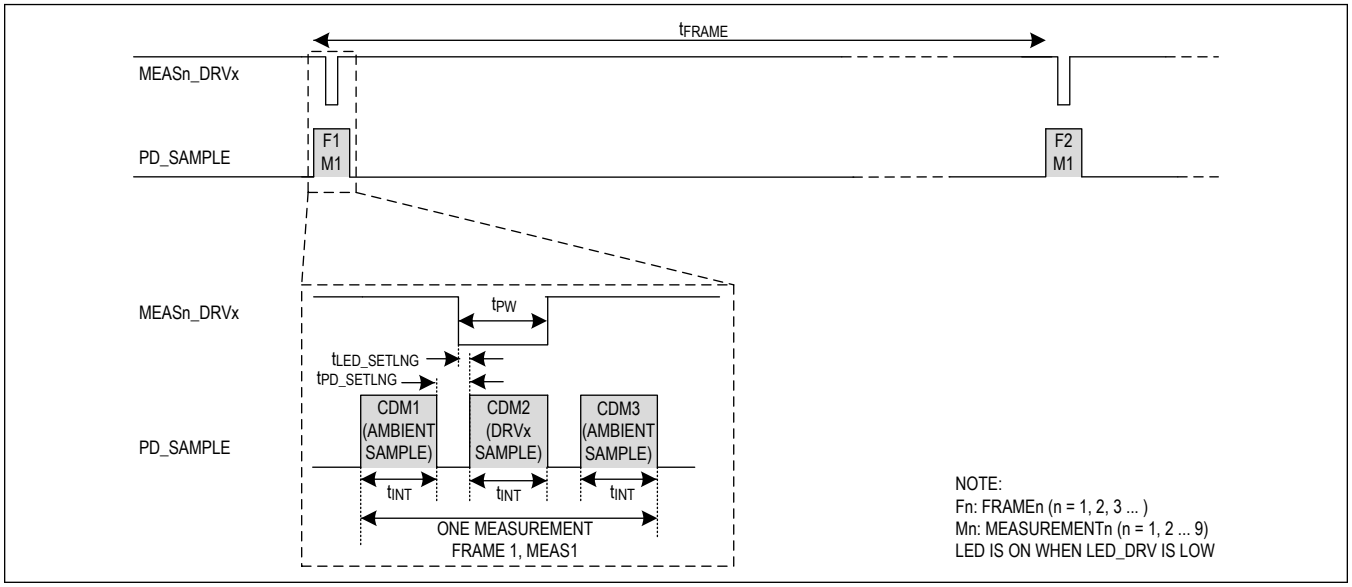


Figure 4. Frame with One Measurement

Frame with All Nine Measurements Enabled

Figure 5 illustrates timing for nine measurements in each frame. MEAS3 is configured as CDM and one of MEAS3_DRVx (x = A, B, C) is sinking current.

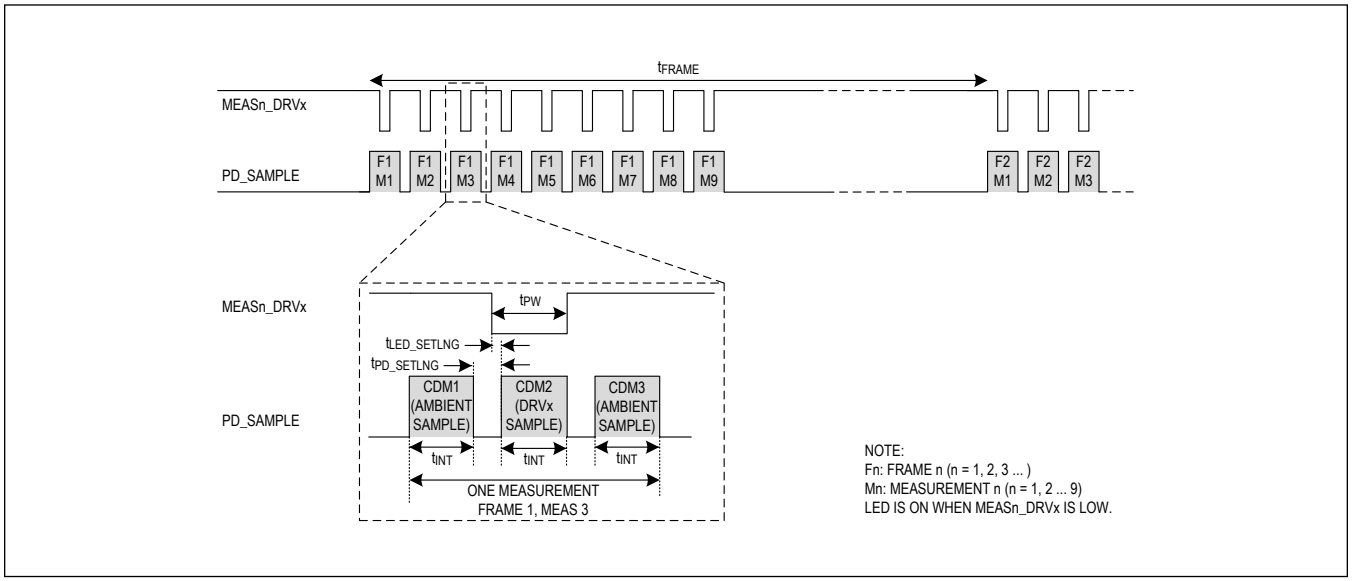


Figure 5. Frame with Nine Measurements

Frame with Measurement Averaging

Figure 6 illustrates timing for nine measurements in each frame with MEAS3 configured as CDM and on-chip average of 2. The result of MEAS3 measurement in each frame only has one FIFO data pushed into FIFO. This FIFO data is the averaged data of N1 and N2 where N1 = N1CDM2 - (N1CDM1 + N1CMD3) / 2 and N2 = N2CDM2 - (N1CDM3 + N2CDM3) / 2. The averaging factor is configured by MEASn_AVER (n = 1 to 9).

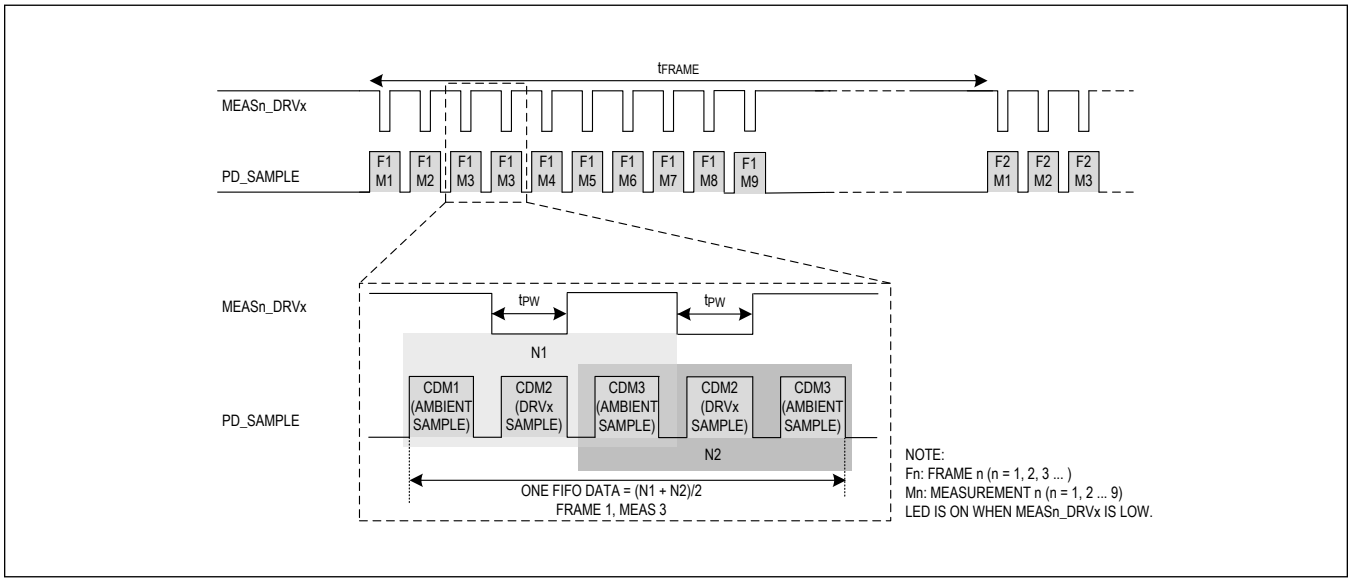


Figure 6. Measurement Averaging

FIFO Description

The FIFO depth is 256 samples and is designed to support various data types. Each sample width is 3 bytes, which includes a 4-bit tag. The tag embedded in the FIFO_DATA[23:0] is used to identify the source of each sample data. The description of each tag is shown in Figure 6.

Measurement Sequence Control (address 0x0C to address 0x0D)

The data format in the FIFO as well as the sequencing of exposures are controlled by the MEAS1_EN through MEAS9_EN bits in the System Configuration 1 and System Configuration 2 registers. There are up to nine measurements available in a frame. The ADC conversion sequence cycles through the enabled measurements shown in Table 5, starting from MEAS1 to MEAS9.

Table 5. MEASUREMENT SEQUENCE CONTROL REGISTERS

ADDRESS	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0
0x0C	System Configuration 1	MEAS9_EN							
0x0D	System Configuration 2	MEAS8_EN	MEAS7_EN	MEAS6_EN	MEAS5_EN	MEAS4_EN	MEAS3_EN	MEAS2_EN	MEAS1_EN

Each of the nine measurements is configured in the MEAS1 setup to MEAS9 Setup registers (See Register Map for details).

Table 6 shows the format of the FIFO data. Optical data, whether ambient corrected LED exposure or direct ambient sampled data, is left justified. Bits F23:F20 of the FIFO word contain the tag that identifies the data. F19:F0 of the FIFO word contain the data which is in 2's complement form. F19 is the sign bit and F18:F0 is the 19 bit sample that was pushed to FIFO after conversion.

Table 6. FIFO DATA FORMAT

FIFO DATA FORMAT (FIFO_DATA[23:16])							
TAG(TAG[3:0])				ADC VALUE(FIFO_DATA[19:16]			
F23	F22	F21	F20	F19	F18	F17	F16
T3	T2	T1	T0	O19	O18	O17	O16
FIFO DATA FORMAT (FIFO_DATA[15:8])							
ADC VALUE (FIFO_DATA[15:8])							
F15	F14	F13	F12	F11	F10	F9	F8
O15	O14	O13	O12	O11	O10	O9	O8
FIFO DATA FROMAT (FIFO_DATA[7:0])							
ADC VALUE (FIFO_DATA[7:0]							
F7	F6	F5	F4	F3	F2	F1	F0
O7	O6	O5	O4	O3	O2	O1	O0

There is no separate tag to identify the measurements for the two optical channels, and for the photodiodes selected for each optical channel. They are distinguished by their relative positions in the FIFO, and the Photodiodes selected for a given measurement. When there is a configuration change, the conversions for the current frame is aborted and a new frame starts with the new configuration. But part of the frame corresponding to the old configuration might have already been saved in the FIFO. So it is important to flush the FIFO after any configuration change. Otherwise, data alignment for the two optical channels might be lost. After the FIFO flush, ignore the data until you get Tag 1 (or the first enabled measurement).

When COLLECT_RAW_DATA is set to 0, computed data is collected in the FIFO. When COLLECT_RAW_DATA is set to 1, raw data for the ambient current and for LED ON current are collected in the FIFO.

Tags 1 to 9 are used when:

1. Computed data (for 2^{MEASx_AVER} pulses) is pushed to the FIFO

2. Raw MEASx data is pushed to the FIFO.

Raw Dark data has a separate tag, and is common to all measurements.

When more than one of the ALC_OVF, EXP_OVF and picket fence event (see the *Picket Fence Detect-and-Replace Function* section) are detected the following priority is used for tag selection:

1. Picket Fence Tag
2. ALC_OVF Tag
3. EXP_OVF Tag
4. MEASx Tag

When COLLECT_RAW_DATA is set to 1, Picket Fence Detection is disabled. An attempt to read an empty FIFO returns the INVALID_DATA tag. The FIFO tags and corresponding data types are explained in Table 7.

Table 7. TAGS AND DATA TYPES

TAG[3:0]	DATA TYPE	COMMENTS
0x0	Reserved	
0x1	PPG MEAS1 DATA	Measurement 1 ADC data
0x2	PPG MEAS2 DATA	Measurement 2 ADC data
0x3	PPG MEAS3 DATA	Measurement 3 ADC data
0x4	PPG MEAS4 DATA	Measurement 4 ADC data
0x5	PPG MEAS5 DATA	Measurement 5 ADC data
0x6	PPG MEAS6 DATA	Measurement 6 ADC data
0x7	PPG MEAS7 DATA	Measurement 7 ADC data
0x8	PPG MEAS8 DATA	Measurement 8 ADC data
0x9	PPG MEAS9 DATA	Measurement 9 ADC data
0xA	PPG DARK DATA	Dark data when Raw data is captured in the FIFO
0xB	PPG ALC_OVF DATA	ALC Overflow was detected. Location of data implies which Measurement and for which PD.
0xC	PPG EXP_OVF DATA	Exposure Overflow was detected. Location of data implies which Measurement and for which PD.
0xD	PPG_PF DATA	Picket Fence event was detected. This occurs only if picket fence is enabled in PPGn_PF_MEAS_SEL[3:0] register. Location of data implies which Measurement and for which PD.
0xE	INVALID DATA	This tag indicates that there was an attempt to read an empty FIFO.
0xF	Reserved	

There are seven registers that control how the FIFO is configured and read out. Details of these registers are in Table 8.

Table 8. FIFO CONFIGURATION REGISTERS

ADDRESS	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0
0X04	FIFO Write Pointer	FIFO_WR_PTR[7:0]							
0X05	FIFO Read Pointer	FIFO_RD_PTR[7:0]							
0X06	FIFO Counter 1	FIFO_DATA_COUNT[8]	OVF_COUNTER[6:0]						
0X07	FIFO Counter 2	FIFO_DATA_COUNT[7:0]							

Table 8. FIFO CONFIGURATION REGISTERS (continued)

ADDRESS	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0
0X08	FIFO Data Register	FIFO_DATA[7:0]							
0X09	FIFO Configuration 1	FIFO_A_FULL[7:0]							
0X0A	FIFO Configuration 2	RAW_DATA	-		FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	

Write Pointer (address 0x04)

FIFO_WR_PTR[7:0] points to the FIFO location where the next data will be written. This pointer advances for each data item pushed on to the FIFO by the internal conversion process. The write pointer is an 8 bit counter and wraps around to count 0x00 on the next data after count 0xFF.

Read Pointer (address 0x05)

FIFO_RD_PTR[7:0] points to the location from where the next data from the FIFO is read through the serial interface. This advances each time a data item is read from the FIFO. The read pointer can be both read and written to. This allows a data item to be reread from the FIFO if it has not already been overwritten. The read pointer is updated from an 8 bit counter and wraps around to count 0x00 from count 0xFF.

Overflow Counter (address 0x06)

OVF_COUNTER[6:0] logs the number of data items lost if the FIFO is not read in a timely fashion. This counter saturates at count value 0x7F. When a complete data item is popped from the FIFO (when the read pointer advances), the OVF_COUNTER is reset to zero. This counter is essentially a debug tool. It should be read immediately before reading the FIFO in order to check if an overflow condition has occurred. See FIFO_RO for more details.

FIFO Data Counter (address 0x06 B7 and address 0x07)

FIFO_DATA_COUNT[8:0] is a read-only register which holds the number of items available in the FIFO for the host to read. This increments when a new item is pushed to the FIFO, and decrements when the host reads an item from the FIFO.

FIFO Data (address 0x08)

FIFO_DATA[7:0] is a read-only register used to retrieve data from the FIFO. It is important to burst read the data from the FIFO. Each data item is three bytes. So burst reading three bytes at the FIFO_DATA register through the serial interface advances the FIFO_RD_PTR[7:0]. The format and data type of the data stored in the FIFO is determined by the tag associated with the data. Readout from the FIFO follows a progression defined by measurements enabled by MEAS1_EN to MEAS9_EN bits in the System Configuration 1 (register 0x0C) and System Configuration 2 (register 0x0D) registers, starting from MEAS1_EN. As mentioned earlier, the data from the two optical channels for a given measurement share the same tag, but can be distinguished by their relative position in the FIFO. The configuration is best illustrated by a few examples.

Assume it is desired to perform an SpO2 measurement and also monitor the ambient level on the photodiode to adjust the IR and red LED intensity using dual optical channels with photodiodes 1 and 2 selected. To perform this measurement, configure the following registers.

Table 9. SYSTEM CONFIGURATION

SYSTEM CONFIGURATION	
MEAS1_EN = 1'b1	(IR LED exposure)
MEAS2_EN = 1'b1	(RED LED exposure)
MEAS3_EN = 1'b1	(DIRECT AMBIENT exposure)
MEAS4_EN = 1'b0	(NONE)

Table 9. SYSTEM CONFIGURATION (continued)

SYSTEM CONFIGURATION	
MEAS5_EN = 1'b0	(NONE)
MEAS6_EN = 1'b0	(NONE)
MEAS7_EN = 1'b0	(NONE)
MEAS8_EN = 1'b0	(NONE)
MEAS9_EN = 1'b0	(NONE)
MEASUREMENT 1 SETUP (IR LED ON LED DRVA ON PIN 1)	
MEAS1_AMB = 1'b0	(Ambient measurement off)
MEAS1_DRVA= 2'b00	(LED Driver A on pin 1 and Current is non-zero)
MEAS1_DRVB= 2'b00	(Don't Care because Current is 0)
MEAS1_DRVC= 2'b00	(Don't Care because Current is 0)
MEAS1_PPG1_ADC_RGE[1:0]	(PPG1 Gain Range Control)
MEAS1_PPG2_ADC_RGE[1:0]	(PPG2 Gain Range Control)
MEAS1_PPG_TINT[1:0]	(LED Pulse Width Control)LED Pulse Amplitude
MEAS1_DRVA_PA[7:0] = 8'h0F	(LED Driver A Current)
MEAS1_DRVB_PA[7:0] = 8'h00	(LED Driver B Current)
MEAS1_DRVC_PA[7:0] = 8'h00	(LED Driver C Current)
MEAS1_PPG1_PDSEL = 1'b0	(Photodiode 1 selected on Optical Channel 1)
MEAS1_PPG2_PDSEL = 1'b0	(Photodiode 2 selected on Optical Channel 2)
MEASUREMENT 2 SETUP (RED LED ON LED DRVB ON PIN 2)	
MEAS2_AMB = 1'b0	(Ambient measurement off)
MEAS2_DRVA= 2'b00	(Don't Care because Current is 0)
MEAS2_DRVB= 2'b00	(LED Driver B on pin 2 and Current is non-zero)
MEAS2_DRVC= 2'b00	(Don't Care because Current is 0)
MEAS2_PPG1_ADC_RGE[1:0]	(PPG1 Gain Range Control)
MEAS2_PPG2_ADC_RGE[1:0]	(PPG2 Gain Range Control)
MEAS2_PPG_TINT[1:0]	(LED Pulse Width Control)LED Pulse Amplitude
MEAS2_DRVA_PA[7:0] = 8'h00	(LED Driver A Current)
MEAS2_DRVB_PA[7:0] = 8'h0A	(LED Driver B Current)
MEAS2_DRVC_PA[7:0] = 8'h00	(LED Driver C Current)
MEAS2_PPG1_PDSEL = 1'b0	(Photodiode 1 selected on Optical Channel 1)
MEAS2_PPG2_PDSEL = 1'b0	(Photodiode 2 selected on Optical Channel 2)
MEASUREMENT 3 SETUP (AMBIENT MEASUREMENT)	
MEAS3_AMB = 1'b1	(Ambient measurement selected)
MEAS3_DRVA= 2'b00	(Don't Care because MEAS3_AMB = 1)
MEAS3_DRVB= 2'b00	(Don't Care because MEAS3_AMB = 1)
MEAS3_DRVC= 2'b00	(Don't Care because MEAS3_AMB = 1)
MEAS3_PPG1_ADC_RGE[1:0]	(PPG1 Gain Range Control)
MEAS3_PPG2_ADC_RGE[1:0]	(PPG2 Gain Range Control)
MEAS3_PPG_TINT[1:0]	(LED Pulse Width Control)
MEAS3_PPG1_PDSEL = 1'b0	(Photodiode 1 selected on Optical Channel 1)
MEAS3_PPG2_PDSEL = 1'b0	(Photodiode 2 selected on Optical Channel 2)

With this configuration the sample sequence and the data format in the FIFO follows the following time/location sequence.

tag 1, PPG1 IR data
tag 1, PPG2 IR data
tag 2, PPG1 RED data
tag 2, PPG2 RED data
tag 3, PPG1 Ambient data
tag 3, PPG2 Ambient data
tag 1, PPG1 IR data
tag 1, PPG2 IR data
tag 2, PPG1 RED data
tag 2, PPG2 RED data
tag 3, PPG1 Ambient data
tag 3, PPG2 Ambient data
.
.
.
tag 1, PPG1 IR data
tag 1, PPG2 IR data
tag 2, PPG1 RED data
tag 2, PPG2 RED data
tag 3, PPG1 Ambient data
tag 3, PPG2 Ambient data

where:

PPGm IR data = Ambient corrected exposure data from IR LED in Optical channel m

PPGm RED data = Ambient corrected exposure data from RED LED in Optical channel m

PPGm Ambient data = Direct ambient sample in Optical channel m

m = 1 for Optical Channel 1, and 2 for Optical Channel 2

For a second example, assume it is desired to pulse IR LED and RED LED simultaneously while also monitoring the ambient level.

Table 10. SYSTEM CONFIGURATION

SYSTEM CONFIGURATION	
MEAS1_EN = 1'b1	(IR LED and RED LED exposure)
MEAS2_EN = 1'b0	(NONE)
MEAS3_EN = 1'b0	(NONE)
MEAS4_EN = 1'b1	(DIRECT AMBIENT exposure)
MEAS5_EN = 1'b0	(NONE)
MEAS6_EN = 1'b0	(NONE)
MEAS7_EN = 1'b0	(NONE)
MEAS8_EN = 1'b0	(NONE)
MEAS9_EN = 1'b0	(NONE)
MEASUREMENT 1 Setup (IR LED ON LED DRVA ON PIN 1, RED LED ON LED DRVB ON PIN 3)	

Table 10. SYSTEM CONFIGURATION (continued)

MEAS1_AMB = 1'b0	(Ambient measurement off)
MEAS1_DRVA= 2'b00	(LED Driver A on pin 1 and Current is non-zero)
MEAS1_DRVB= 2'b01	(LED Driver B on pin 3 and Current is non-zero)
MEAS1_DRVC= 2'b00	(Don't Care because Current is 0)
MEAS1_PPG1_ADC_RGE[1:0]	(PPG1 Gain Range Control)
MEAS1_PPG2_ADC_RGE[1:0]	(PPG2 Gain Range Control)
MEAS1_PPG_TINT[1:0]	(LED Pulse Width Control)LED Pulse Amplitude
MEAS1_DRVA_PA[7:0] = 8'h0B	(LED Driver A Current)
MEAS1_DRVB_PA[7:0] = 8'h0E	(LED Driver B Current)
MEAS1_DRVC_PA[7:0] = 8'h00	(LED Driver C Current)
MEASUREMENT 4 SETUP (AMBIENT MEASUREMENT)	
MEAS4_AMB = 1'b1	(Ambient measurement selected)
MEAS4_DRVA= 2'b00	(Don't Care because MEAS4_AMB = 1)
MEAS4_DRVB= 2'b00	(Don't Care because MEAS4_AMB = 1)
MEAS4_DRVC= 2'b00	(Don't Care because MEAS4_AMB = 1)
MEAS4_PPG1_ADC_RGE[1:0]	(PPG1 Gain Range Control)
MEAS4_PPG2_ADC_RGE[1:0]	(PPG2 Gain Range Control)
MEAS4_PPG_TINT[1:0]	(LED Pulse Width Control)

In this case, the sequencing in the FIFO is,

tag 1, PPG1 IR+RED data
tag 1, PPG2 IR+RED data
tag 4, PPG1 Ambient data
tag 4, PPG2 Ambient data
tag 1, PPG1 IR+RED data
tag 1, PPG2 IR+RED data
tag 4, PPG1 Ambient data
tag 4, PPG2 Ambient data
.
.
.
tag 1, PPG1 IR+RED data
tag 1, PPG2 IR+RED data
tag 4, PPG1 Ambient data
tag 4, PPG2 Ambient data

where:

PPGm IR+RED data = Ambient corrected exposure data from IR and RED for optical channel m

PPGm Ambient data = Direct ambient corrected sample for optical channel m

m = 1 for Optical Channel 1, and 2 for Optical Channel 2

The number of bytes of data for the two Optical Channels in one frame is given by: 2 x 3 x N

where, N is the number of measurements enabled

To calculate the number of data items available in the FIFO the following pseudo-code can be performed:

```
read the OVF_COUNTER register
read the FIFO_DATA_COUNT registers
if OVF_COUNTER == 0 //no overflow occurred
   NUM_AVAILABLE_SAMPLES = FIFO_DATA_COUNT
else
   NUM_AVAILABLE_SAMPLES = 256   // overflow occurred and data has been lost
endif
```

FIFO_A_FULL (address 0x09)

The FIFO_A_FULL[7:0] field in the FIFO Configuration 1 register (0x09) sets the watermark for the FIFO and determines when the A_FULL bit in the Status register (0x00) gets asserted. The A_FULL bit sets when the number of data items in FIFO is equal to 256 minus FIFO_A_FULL[7:0]. The interrupt is routed to the INT1 if A_FULL_EN1 mask bit in the Interrupt 1 Enable 1 register (0x78) is set, and to the INT2 pin if the A_FULL_EN2 mask bit in Interrupt 2 Enable 1 register (0x7C) is set. This condition should prompt the applications processor to read samples from the FIFO immediately. The A_FULL bit is cleared when the status register is read.

The application processor can read both the FIFO_WR_PTR[7:0] and FIFO_RD_PTR[7:0] to calculate the number of data items available in the FIFO, or just read the OVF_COUNTER[6:0] and FIFO_DATA_COUNT[8:0] registers, and read as many data items as it needs to empty the FIFO. Alternatively, if the application always responds much faster than the selected sample rate, it could read 256 minus FIFO_A_FULL[7:0] number of data items every time it gets an A_FULL interrupt and be assured that all data from the FIFO are read.

FIFO_RO (address 0x0A)

The FIFO_RO bit in the FIFO Configuration 2 register (0x0A) determines whether samples get pushed on to the FIFO when it is full. If FIFO_RO is set to 1, push is enabled when FIFO is full, old samples are lost. Both FIFO_WR_PTR and FIFO_RD_PTR increment for each data item pushed to the FIFO after it is full. If FIFO_RO is set to 0, the new sample is dropped and the FIFO is not updated. FIFO_WR_PTR and FIFO_RD_PTR do not increment until a data item is read from the FIFO.

A_FULL_TYPE (address 0x0A)

The A_FULL_TYPE bit defines the behavior of the A_FULL interrupt. If the A_FULL_TYPE bit is set low, the A_FULL interrupt gets asserted when the A_FULL condition is detected and cleared by a status register read, but reasserts for every sample if the A_FULL condition persists. If A_FULL_TYPE bit is set high, the A_FULL interrupt gets asserted only when a new A_FULL condition is detected. The interrupt gets cleared on the Interrupt Status 1 register read, and does not reassert for every sample until a new A_FULL condition is detected.

FIFO_STAT_CLR (address 0x0A)

The FIFO_STAT_CLR bit defines whether the A_FULL interrupt should get cleared by FIFO_DATA[7:0] register read. If FIFO_STAT_CLR is set low, A_FULL and FIFO_DATA_RDY interrupts do not get cleared by the FIFO_DATA register read but get cleared by the status register read. If FIFO_STAT_CLR is set high, A_FULL and FIFO_DATA_RDY interrupts get cleared by a FIFO_DATA register read or a status register read.

FLUSH_FIFO (address 0x0A)

The FIFO Flush bit is used for flushing the FIFO. The FIFO becomes empty and the FIFO_WR_PTR[7:0], FIFO_RD_PTR[7:0], FIFO_DATA_COUNT[8:0] and OVF_COUNTER[6:0] get reset to zero. FLUSH_FIFO is a self-clearing bit.

Ambient Rejection

The MAX86171 implements ambient light cancellation in two steps, a coarse cancellation and a fine cancellation. Each MEASx gets its own ambient light cancellation. The coarse cancellation is in the analog domain. It is enabled by default and can be disabled by setting register bit ALC_DISABLE. The fine cancellation is a digital cancellation scheme and is configured as central difference method (CDM) or forward different method (FDM) (register bit MEASx_FILT_SEL).

ALC is an analog sample and hold which can cancel up to 200µA of DC photodiode current. Any drift or residual from ALC is cancelled by CDM/FDM cancellation.

CDM is comprised of 3 ADC conversions with 2 ambient and 1 exposure conversion. FDM is comprised of 2 ADC conversions with 1 ambient only and 1 exposure conversion.

The ambient and exposure samples are used for digital cancellation of any residual error (from ALC) or drift (in ambient signal). The final computed value is the effective exposure signal which is stored in the FIFO. See Figure 7 for the timing diagram for CDM and Figure 8 shows the timing diagram for FDM.

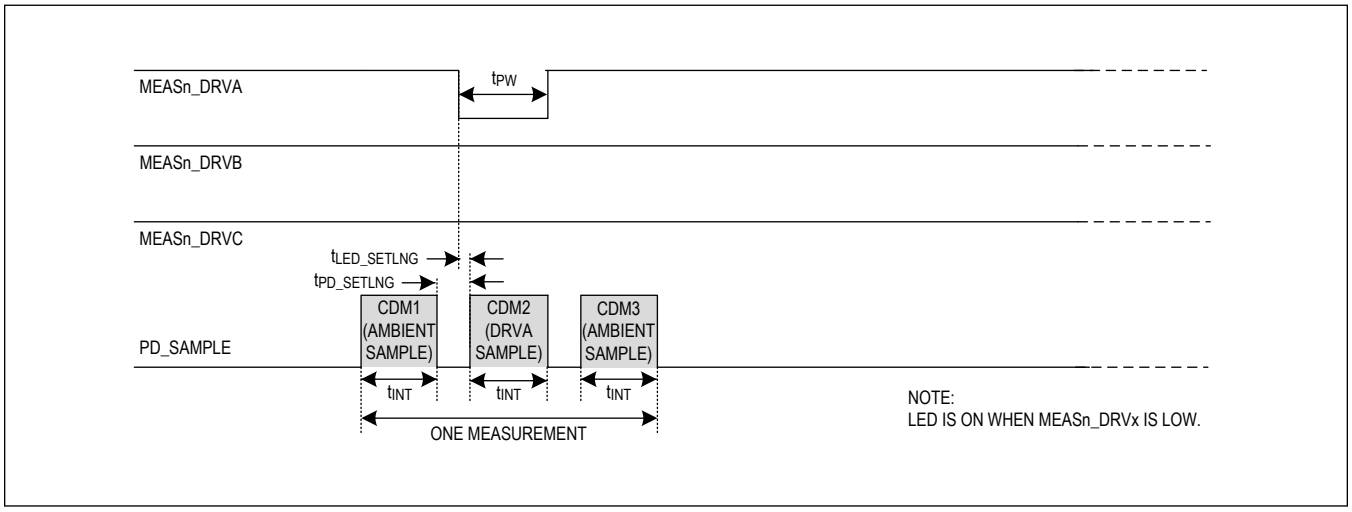


Figure 7. Central Difference Method (CDM)

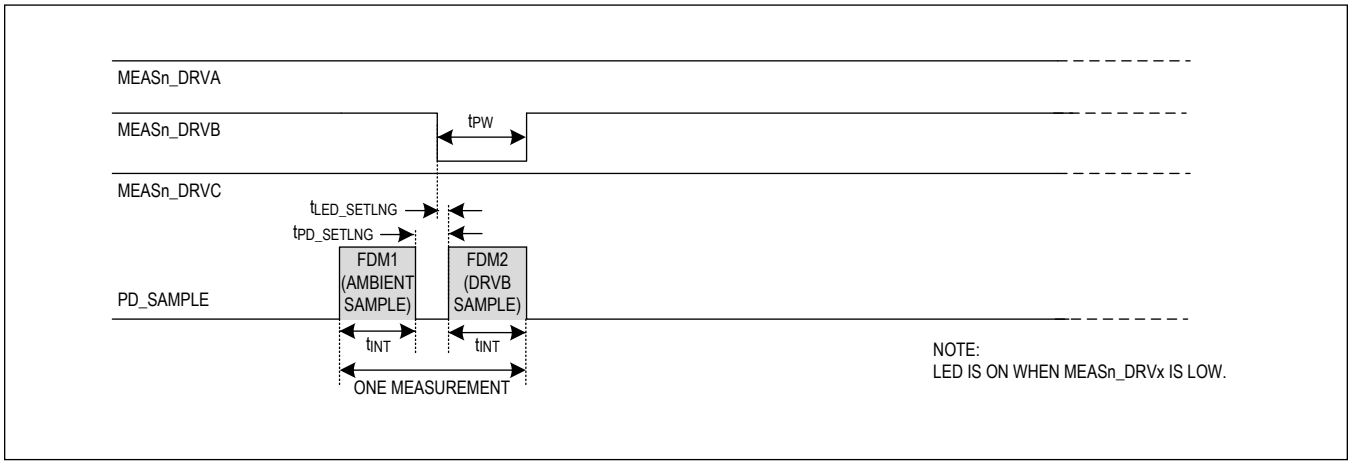


Figure 8. Forward Difference Method (FDM)

Threshold Detect Function

The MAX86171 includes a threshold detect function that significantly reduces energy consumption and extends battery life when the sensor is not in contact with skin. There are two thresholds available in MAX86171, THRESHOLD1 and THRESHOLD2. Both are disabled by default.

The Threshold function is enabled by setting THRESHx_HILO_EN1 (x = 1, 2) in register 0x78 and THRESHx_HILO_EN2(x = 1,2) in register 0x7C. The Threshold detect function can be set up for either PPG1 or PPG2 through THRESH2_PPG_SEL and THRESH1_PPG_SEL (register 0x69). In order to configure the threshold detect function, both an upper limit and a lower limit must be set. These can be configured in the THRESHOLD Interrupts

register block (0x68 to 0x6D).

In addition, two features are available to make the threshold detect function more adaptable for various system and application requirements. These are Time Hysteresis and Level Hysteresis (TIME_HYST[1:0] and LEVEL_HYST[2:0] bits) and are configurable through the THRESHOLD_HYST register (0x69).

When enabled, the THRESHx_HILO interrupt bit (register 0x00) is asserted and threshold mode is activated when the ADC counts of the assigned measurement on the specified PPG channel drops below the lower limit, or exceeds the upper limit (in consideration with LEVEL_HYST and TIME_HYST settings). The LED configuration during the threshold detect active mode is determined by the firmware settings as needed for each application. The LED current, ADC integration time, and frame rate can be reduced significantly; thereby reducing power consumption during situations when there is no reflective returned signal.

Picket Fence Detect-and-Replace Function

Under typical situations, the rate of change of ambient light is such that the ambient signal level during exposure can be accurately predicted and high levels of ambient rejection are obtained. However, it is possible to have situations where the ambient light level changes extremely rapidly, for example when in a car with direct sunlight exposure passes under a bridge and into a dark shadow. In these situations, it is possible for the MAX86171 ambient light correction (ALC) circuit to fail and produce an erroneous estimation of the ambient light during the exposure interval. The MAX86171 has a built-in algorithm called the picket fence function that corrects the final PPG results in case of the ALC circuit failure due to these extreme conditions.

The picket fence function works on the basis that the extreme conditions causing a failure of the ALC are rare events. These events result in a large deviation from the past sample history of a normal PPG signal, which normally would change relatively slowly with respect to the sampling interval. Under these conditions, the picket fence function enables the user to detect sample values that are well outside the normal sample-to-sample deviation and replace those samples with an extrapolated value based on the relatively recent history of samples.

The picket fence function is configured in the Picket Fence Measurement Select Register (address 0x70). Picket Fence can be enabled on any of the 9 measurements at any one time. Also, picket fence can be enabled on one or both PPG channels. The power-on-reset default of MAX86171 has the picket fence function disabled. The function begins with detecting a picket fence event. Detection is done by taking the absolute value of the difference between the present ADC converted value and a predicted point called an estimation error, and comparing this estimation error to a threshold. If the estimation error exceeds the threshold, then the present ADC converted point is considered a picket fence event.

The predicted point referred to above is computed in one of two ways, set by the value in the PF_ORDER (address 0x71[6]) bit. If PF_ORDER = 0 the predicted point is simply the previous ADC converted point. If PF_ORDER = 1 the predicted point is a least square fit extrapolation based on the previous four picket fence outputs, which under normal circumstances is identical to the ADC converted inputs.

The threshold used in detecting a picket fence event is a low pass version of the running estimation error computed above times a multiplier. The multiplier used is set by the THRESHOLD_SIGMA_MULT (address 0x71[1:0]) bits and can be 4, 8, 16, or 32 times the running low-pass filter output of the estimation error.

The low pass filter function is controlled by two parameters, the IIR_TC (address 0x71[5:4]) bits and IIR_INIT_VALUE (address 0x71[3:2]) bits. The IIR_TC bits control the filter's time constant and are adjustable from 8 to 64 samples. The IIR_INIT_VALUE bits control the initial values for the IIR low pass filter when the algorithm is initialized.

Figure 9 below illustrates the function in block diagram form. If the picket fence algorithm is enabled (address 0x70), the input from the ADC, s(n) generates p(n) in a way that is dependent on the value of the PF_ORDER bit. Value s(n) is subtracted from p(n) and turned into a positive number d(n) and fed into the IIR low pass filter producing value lpf(n). The output of the low pass filter lpf(n) is then multiplied by a user constant, THRESHOLD_SIGMA_MULT to produce the picket fence threshold, PFT(n). The value d(n) is then compared to this threshold and if greater than the PFT(n), the point s(n) is replaced with the point p(n).

This scheme essentially produces a threshold that tracks the past returned optical signal with a bandwidth based on the past historical change from sample to sample. Figure 10 below illustrates graphically how the threshold detection scheme works on a real PPG signal. Note that the black trace is the real ADC sample points, the red trace is the output of the low pass filter of the error estimation mirrored around the ADC points, and the blue traces are the threshold values.

The recommended settings for the picket fence algorithm are the default power on reset values for all registers except

the THRESHOLD_SIGMA_MULT bits. Here, it is recommended that the 32x value 0x3 be used so only large excursions are classified as picket fence events. Lower values of THRESHOLD_SIGMA_MULT can cause the algorithm to go off track in case of an extremely noisy waveform.

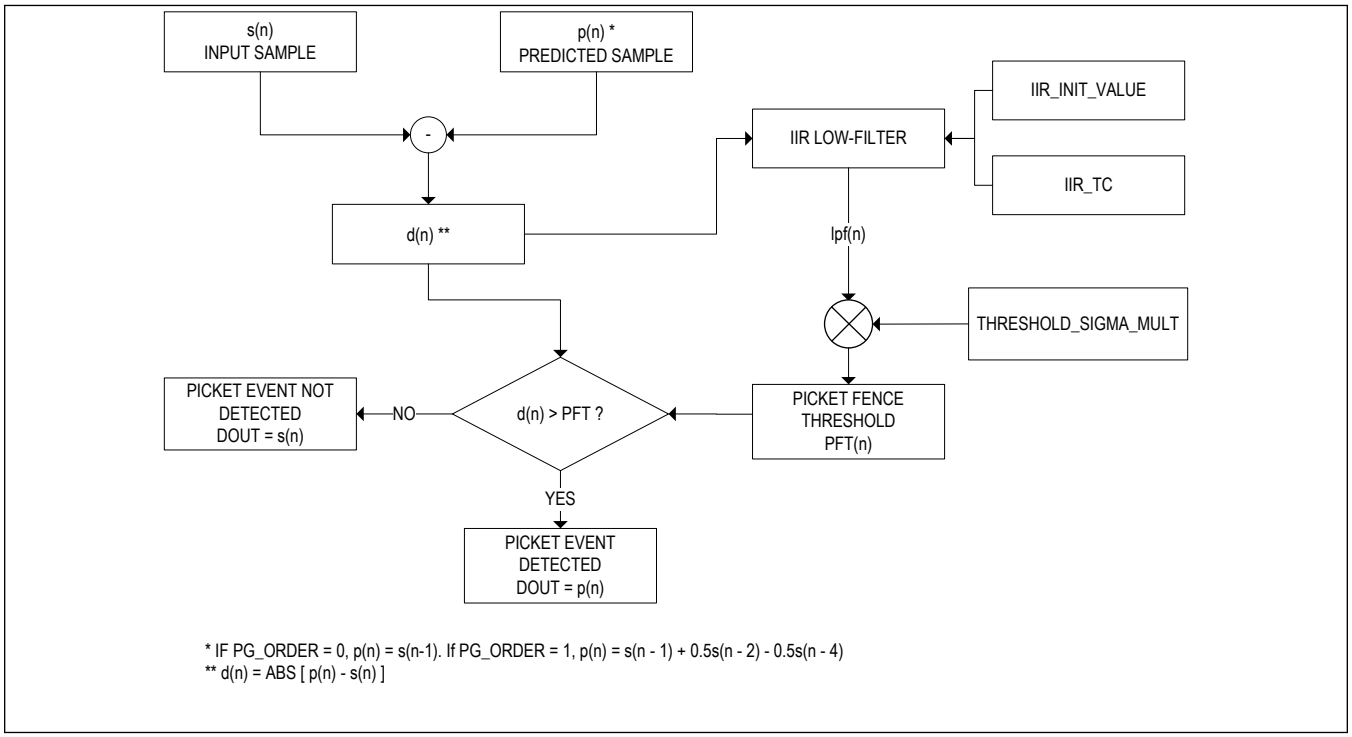


Figure 9. Picket Fence Function Flow

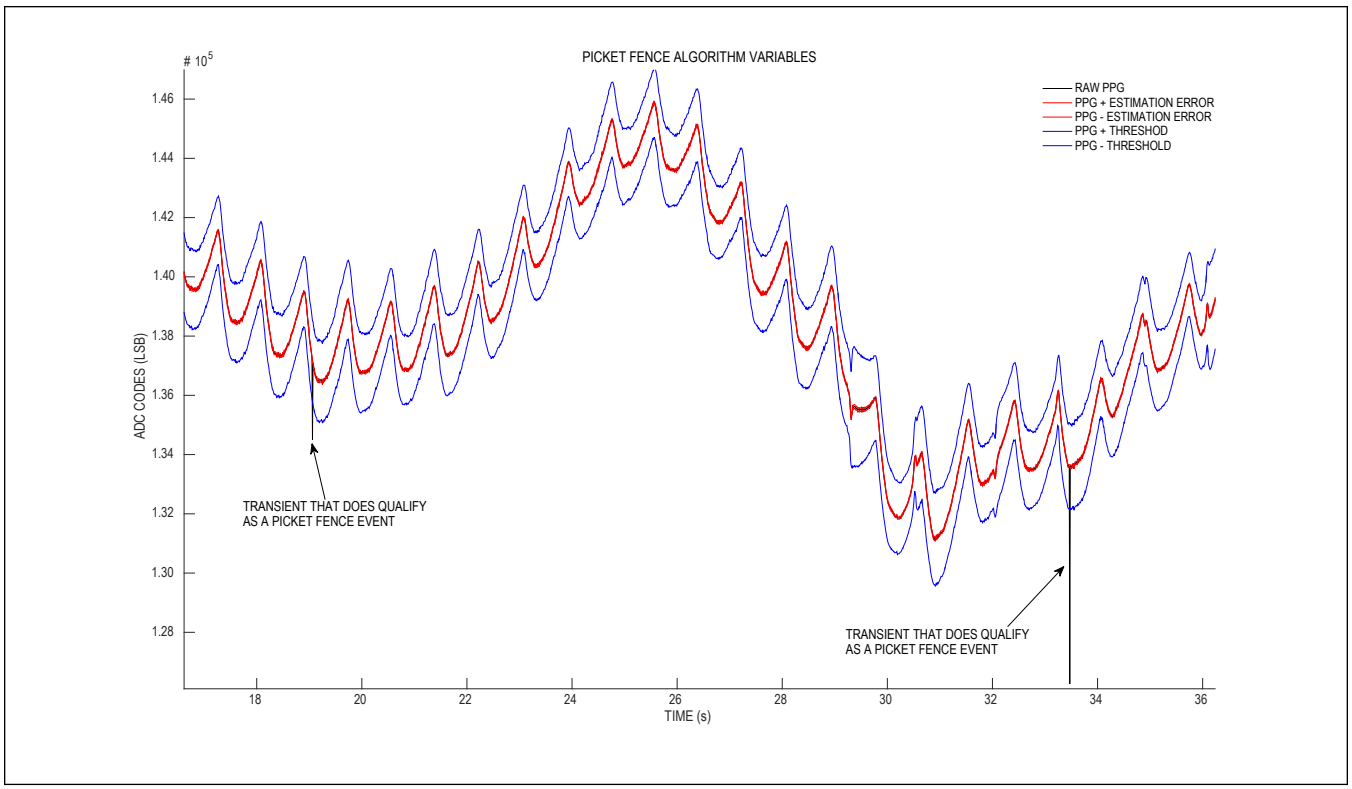


Figure 10. Picket Fences Variables In A PPG Waveform

Digital Interface

The MAX86171 has an I2C and SPI combination interface. The I2C_SEL pin selects between the two interfaces. When I2C_SEL is high, the interface is in the I2C mode and idles looking for a start bit to occur on the SCL and SDA pins, while the SPI interface is held in a reset state. When I2C_SEL is low, the I2C interface is in a reset state, the SPI interface is activated and the SDO pin goes active. In the following sections, both interface timings and protocols are described.

SPI Timing

Detailed SPI Timing

The MAX86171 detailed SPI timing diagram is illustrated in Figure 11. The timings indicated are all specified in the *Electrical Characteristics* section.

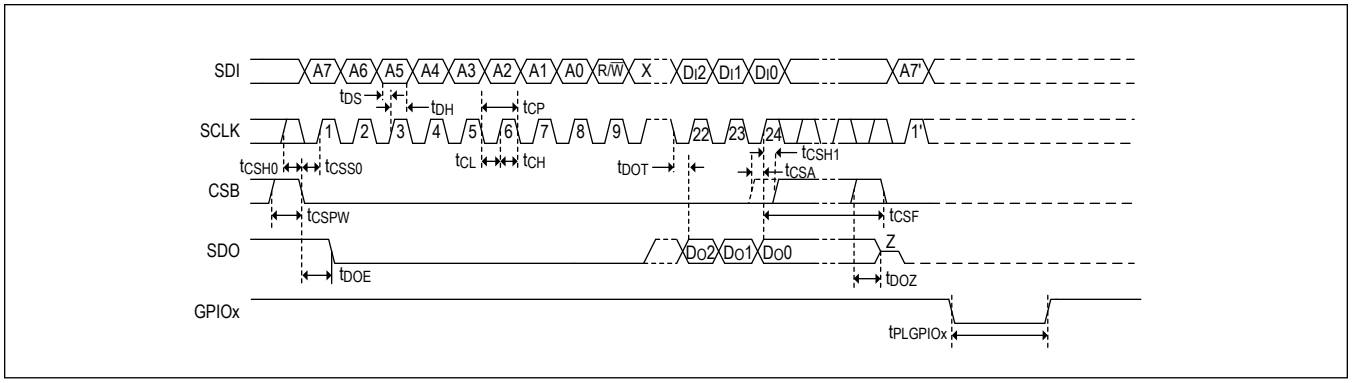


Figure 11. Detailed SPI Timing Diagram

Single-Word SPI Register Read/Write Transaction

The SPI interface on the MAX86171 is SPI/QSPI/Micro-wire/DSP compatible. The operation of the SPI interface is shown in Figure 12. Data is strobed into the MAX86171 on the SCLK rising edge while clocked out on the SCLK falling edge. All single-word SPI read and write operations are done in a three-byte, 24-clock-cycle SPI instruction framed by a CSB low interval. The content of the SPI operation consists of a one-byte register address, A[7:0], followed by a one byte command word which defines the transaction as write or read, followed by a single-byte data word either written to or read from the register location provided in the first byte.

Write mode operations are executed on the 24th SCLK rising edge using the first three bytes of data available. In write mode, any data supplied after the 24th SCLK rising edge is ignored. Subsequent writes require CSB to deassert high and then assert low for the next write command. A rising CSB edge preceding the 24th rising edge of SCLK (Figure 11), results in the transaction being aborted.

Read mode operations access the requested data on the 16th SCLK rising edge, and present the MSB of the requested data on the following SCLK falling edge, allowing the SPI master to latch the data MSB on the 17th SCLK rising edge. Configuration and status registers are available via normal mode read-back sequences. FIFO reads must be done with a burst mode FIFO read (see *SPI FIFO Burst Mode Read Transaction* section). If more than 24 SCLK rising edges are provided in a normal read sequence then the excess edges are ignored and the device reads back zeros.

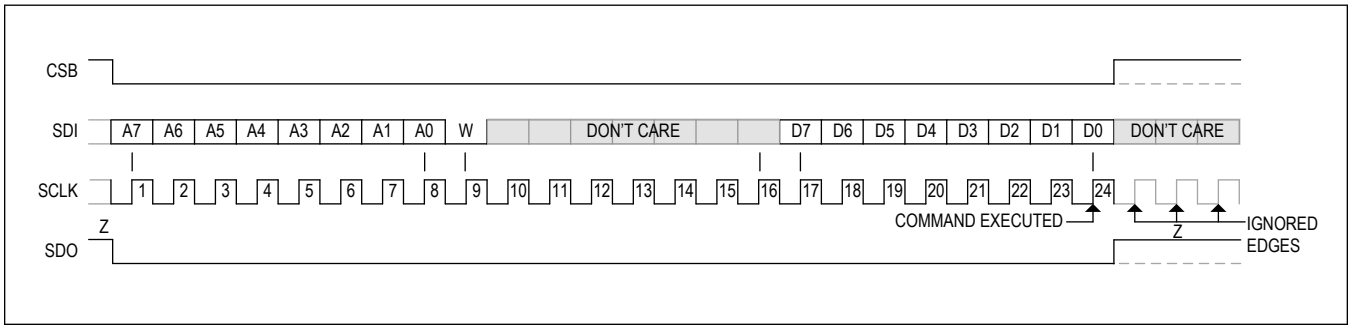


Figure 12. SPI Write Transaction

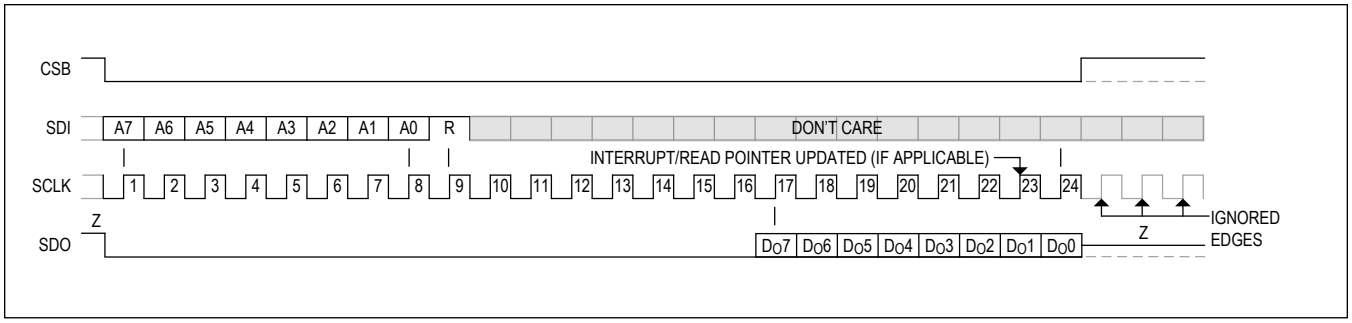


Figure 13. SPI Read Transaction

SPI FIFO Burst Mode Read Transaction

The MAX86171 provides a FIFO burst read mode to increase data transfer efficiency. The first 16 SCLK cycles operate exactly as described for the normal read mode, the first byte being the register address, the second being a read command. The subsequent SCLKs consist of FIFO data, 24 SCLKs per word. All words in the FIFO should be read with a single FIFO burst read command.

Each FIFO sample consists of three bytes per sample ([[FIFO Data Format]]); thus, requires 24 SCLKs per sample to read out. The first byte (SCLK 17 to 24) consists of a tag indicating the data type of the subsequent bits. Following the tag is the MSBs of the subsequent data (MSB, MSB1, MSB2, and MSB3). The next byte (SCLK 25 to 32) consists of data bits MSB4 to MSB11. The final byte of each sample (SCLK 33 to 40) consists of the data LSB bits. The number of words in the FIFO depends on the FIFO configuration. See the FIFO_A_FULL (0x09) section for more details.

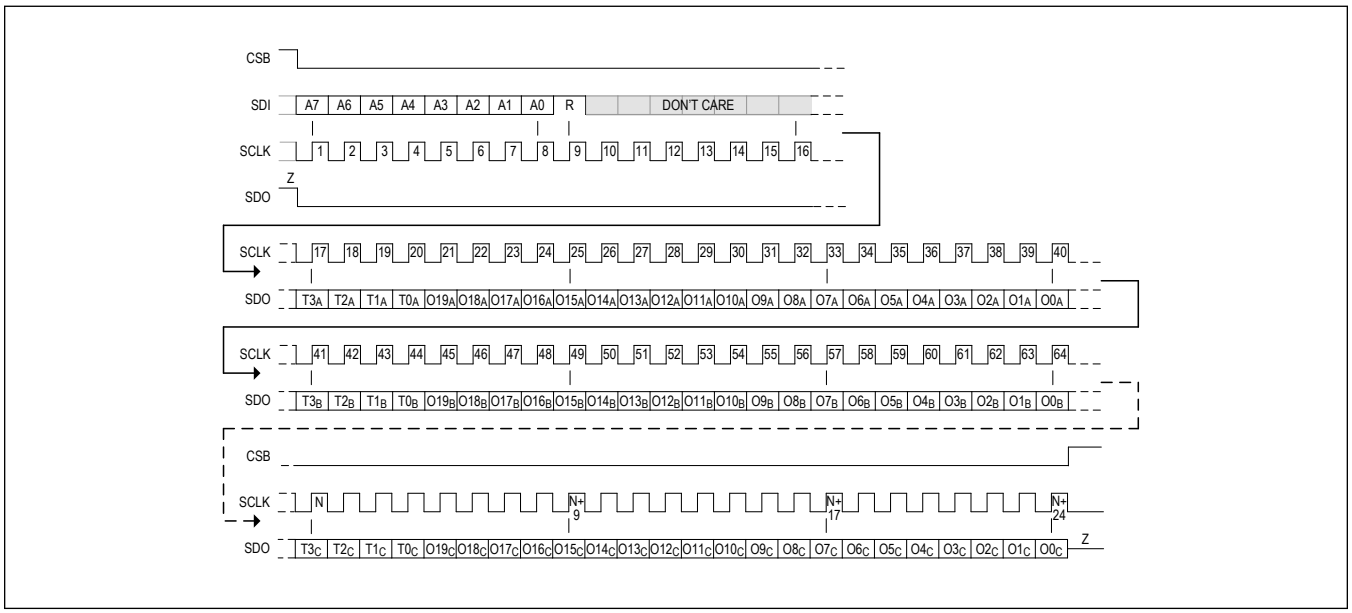


Figure 14. SPI FIFO Burst Mode Read Transaction

I²C/SMBus-Compatible Serial Interface

The I²C interface on the MAX86171 is an I²C/SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX86171 and the master at clock rates up to 400kHz.

Figure 15 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX86171 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a

STOP (P) condition. Each word transmitted to the MAX86171 is eight-bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX86171 transmits the proper slave address followed by a series of nine SCL pulses. The MAX86171 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor is required on SDA. SCL operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX86171 from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Detailed I²C Timing Diagram

The detailed timing diagram of various electrical characteristics is shown in Figure 15.

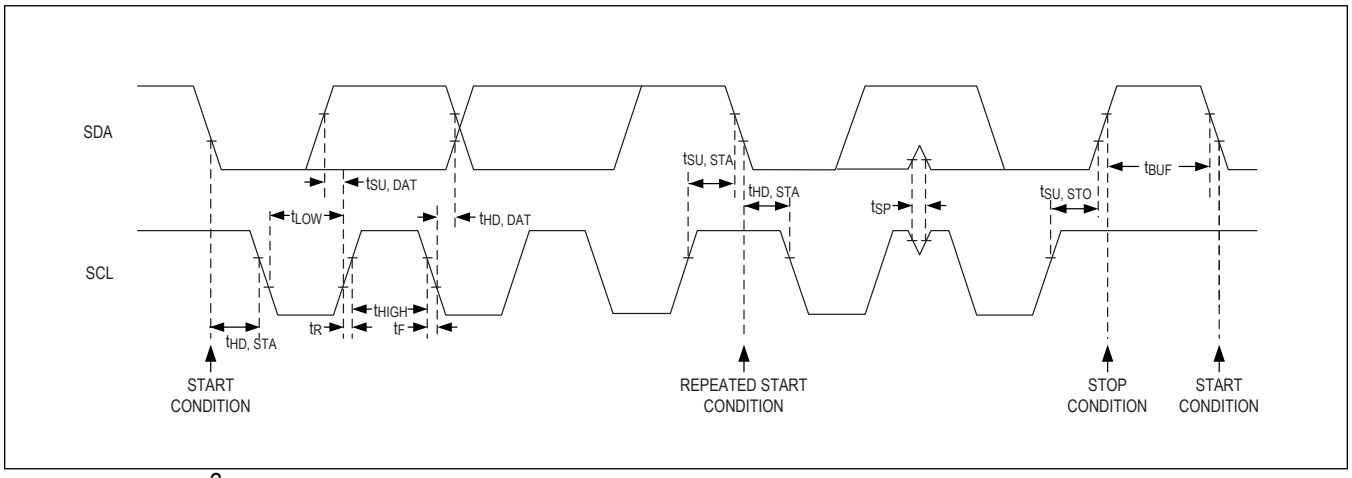


Figure 15. Detailed I²C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 16). A START condition from the master signals the beginning of a transmission to the MAX86171. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

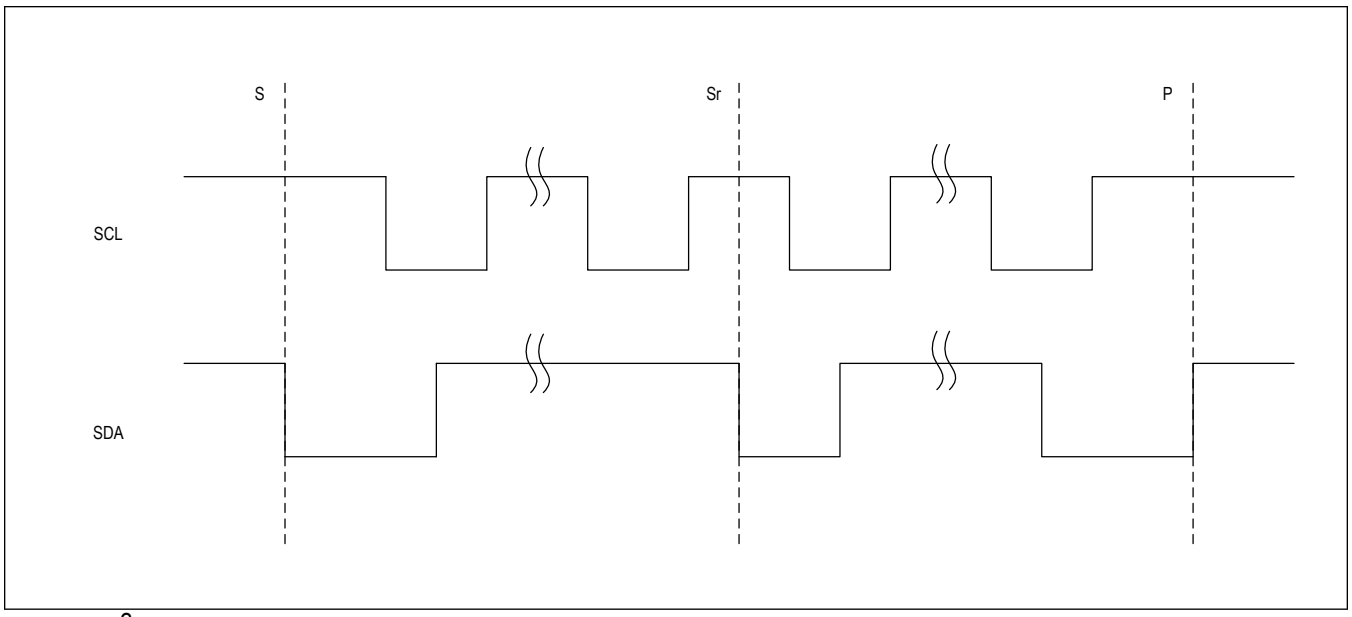


Figure 16. I²C START, STOP, and REPEATED START Conditions

Early STOP Conditions

The MAX86171 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the MAX86171 the seven most significant bits are 0b110010X, where X is determined by the CSB/ADDR pin. For read mode, set the read/write bit to 1. For write mode, set the read/write bit to 0. The address is the first byte of information sent to the IC after the START condition. See Table 11.

Table 11. I²C Slave Address

ADDR PIN	WRITE	READ
High	0xCA	0xCB
Low	0xC8	0xC9

Acknowledge Bit

The acknowledge bit (ACK) is a clocked 9th bit that the MAX86171 uses to handshake receipt of each byte of data when in write mode (Figure 17). The MAX86171 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX86171 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge (NACK) is sent when the master reads the final byte of data from the MAX86171 followed by a STOP condition.

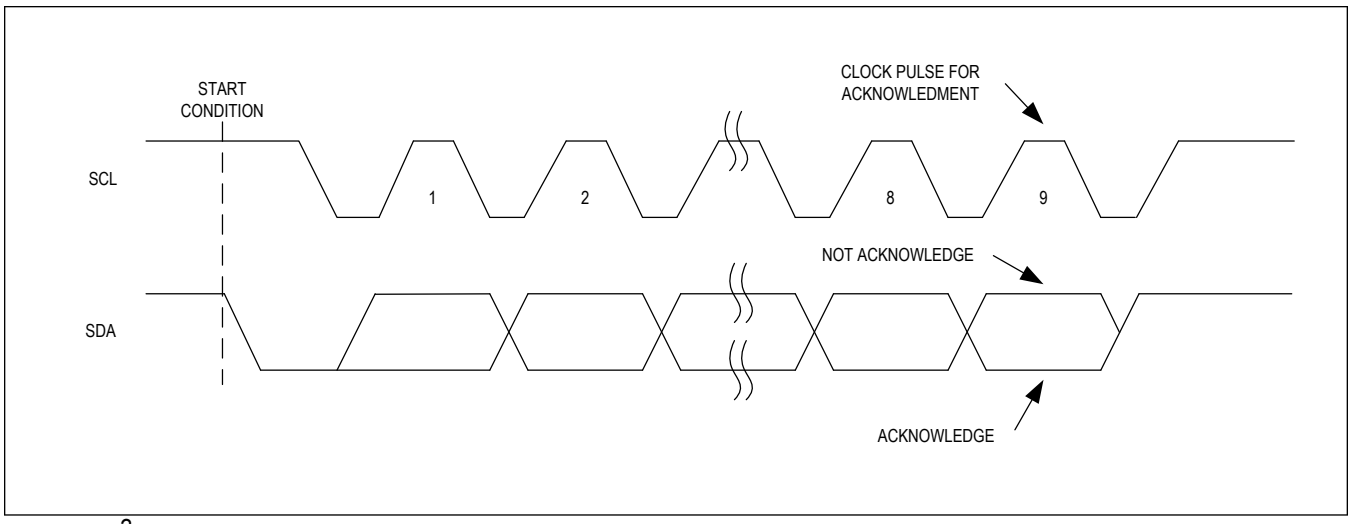


Figure 17. I²C Acknowledge Bit

I²C Write Data Format

A write to the MAX86171 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 18 illustrates the proper frame format for writing one byte of data to the MAX86171. Figure 19 illustrates the frame format for writing n-bytes of data to the MAX86171.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX86171. The MAX86171 acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX86171 internal register address pointer. The pointer tells the MAX86171 where to write the next byte of data. An acknowledge pulse is sent by the MAX86171 upon receipt of the address pointer data.

The third byte sent to the MAX86171 contains the data that is written to the chosen register. An acknowledge pulse from the MAX86171 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. The autoincrement feature is disabled when there is an attempt to write to the FIFO_DATA register.

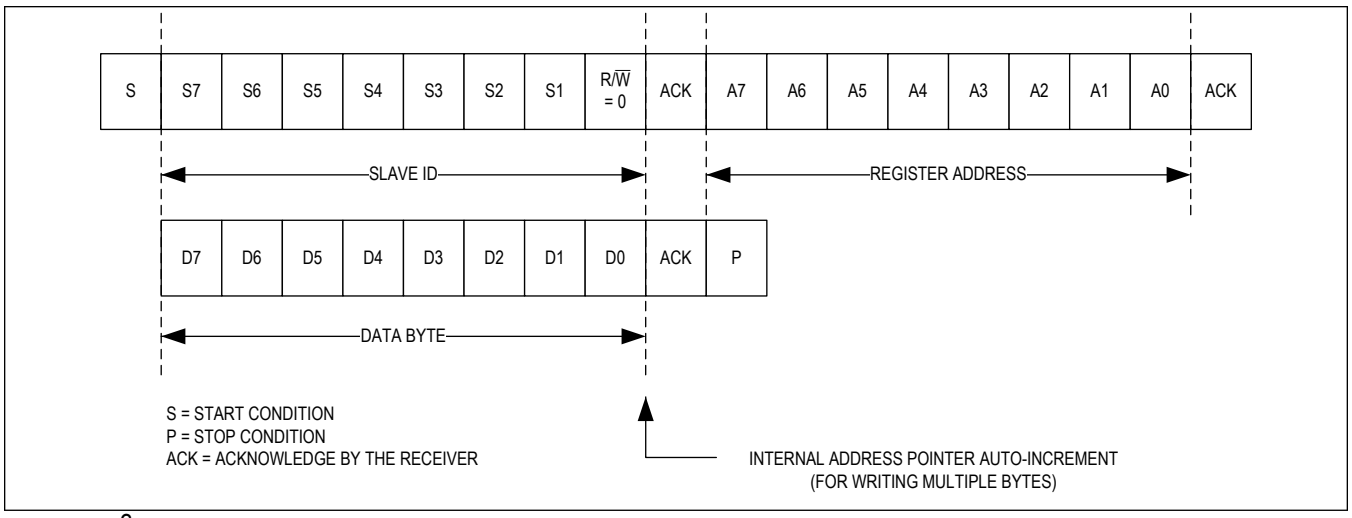


Figure 18. I²C Single Byte Write Transaction

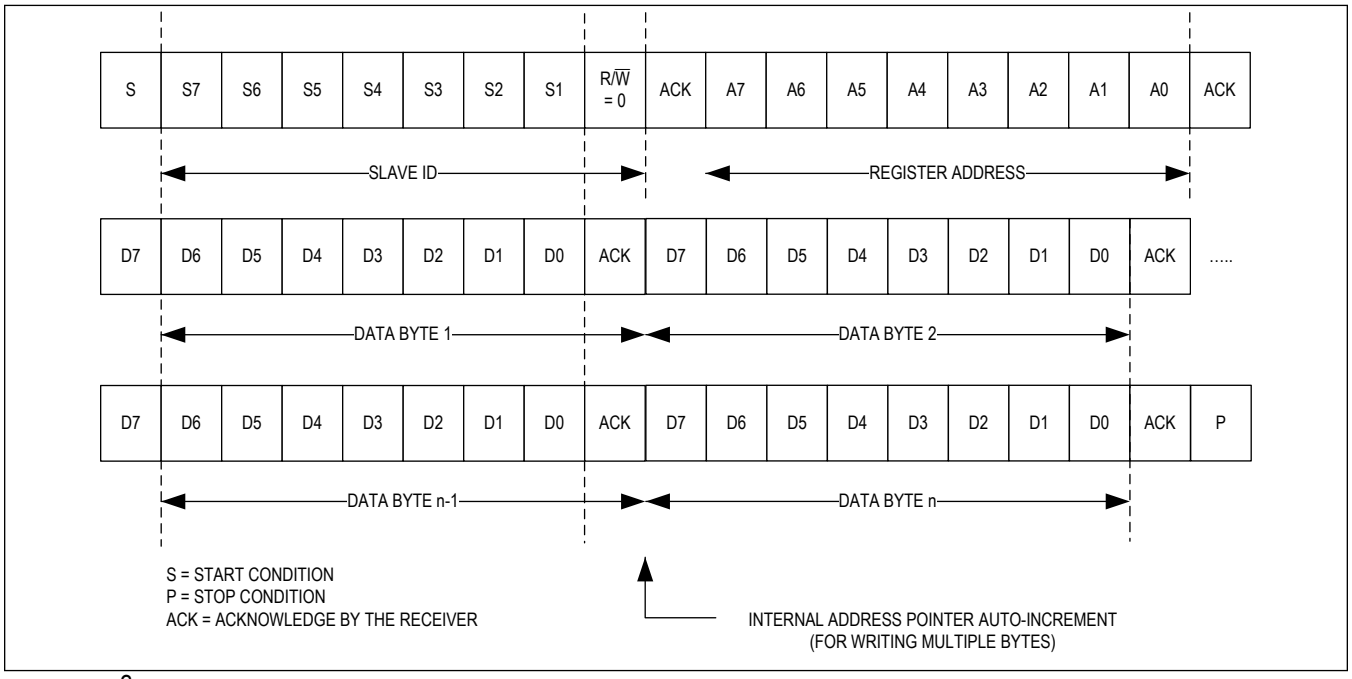


Figure 19. I²C Multi-Byte Write Transaction

I²C Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX86171 acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX86171 is the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. The auto_increment feature is disabled when there is an attempt to read from the FIFO_DATA register. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX86171 slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX86171 then transmits the contents of the specified register. The address pointer auto-increments after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a NACK from the master and then a STOP condition.

Figure 20 illustrates the frame format for reading one byte from the MAX86171. Figure 21 illustrates the frame format for reading multiple bytes from the MAX86171.

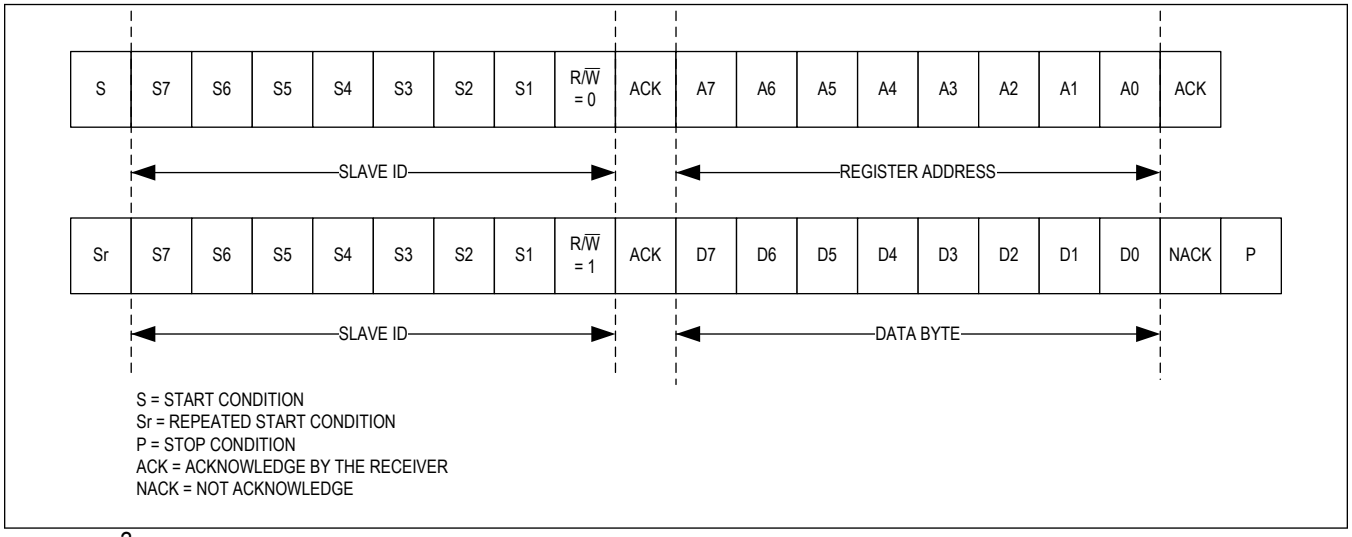


Figure 20. I^2C Single Byte Read Transaction

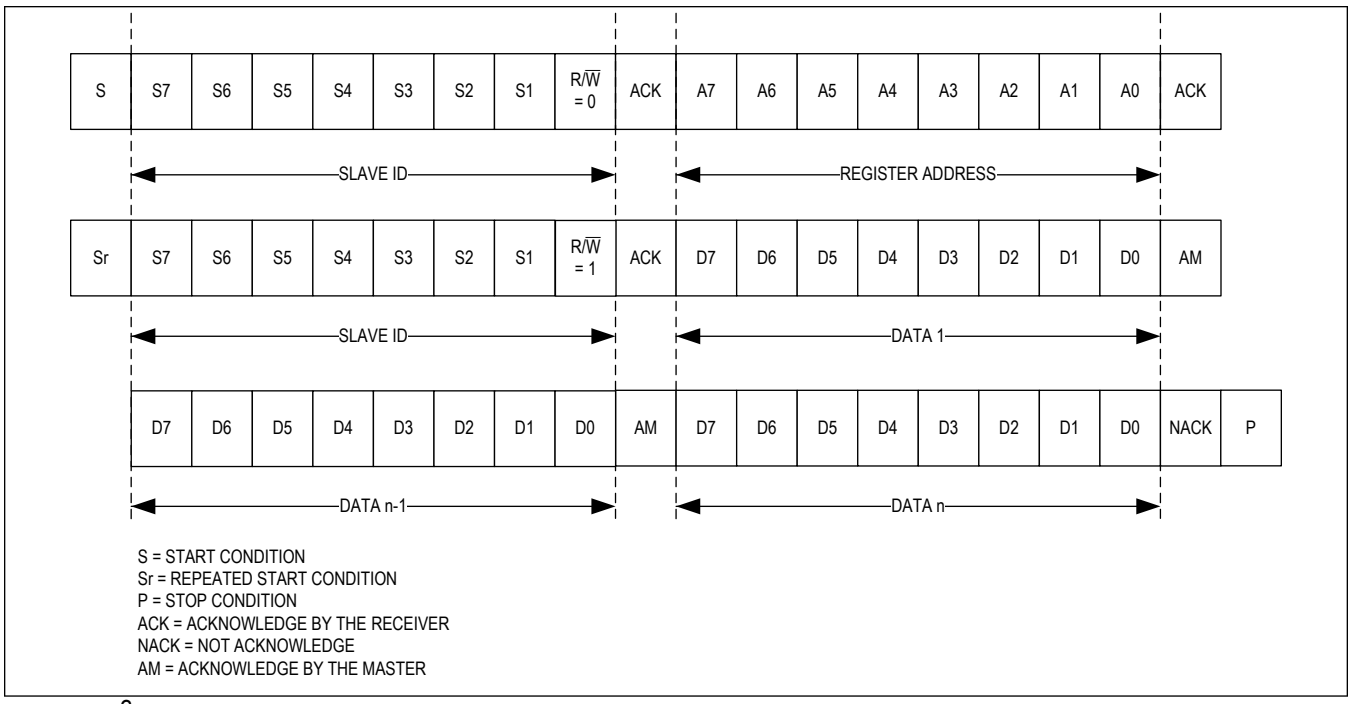


Figure 21. I^2C Multi-Byte Read Transaction

PCB Layout Guidelines

MAX86171 is a high dynamic range analog front-end (AFE) and its performance can be adversely impacted by the physical printed circuit board (PCB) layout. It is important that all bypass recommendation in the pin table be followed. Specifically, it is recommended that the V_{DD_ANA} and V_{DD_DIG} pins be shorted at the PCB. It is also recommended that GND, and PGND be shorted to a single PCB ground plane.

The combined V_{DD_ANA} and V_{DD_DIG} pins should then be decoupled with a 0.1µF and a larger ceramic chip capacitor around 10µF to the PCB Ground plane. In addition, the VREF pin should be decoupled to the PCB Ground plane with a 1.0µF ceramic capacitor. The voltage on the VREF pin is nominally 1.21V, so a 6.3V-rated ceramic capacitor should be adequate for this purpose. It is recommended that all decoupling caps use individual vias to the PCB Ground plane to avoid mutual impedance coupling between decoupled supplies when sharing vias.

The most critical aspect of the PCB layout of MAX86171 is the handling of the PD_IN and PD_GND nodes. Parasitic capacitive coupling to the PD_IN can result in additional noise being injected into the MAX86171 front-end. To minimize external interference coupling to PD_IN, it is recommended that the PD_IN node be fully shielded by the PD_GND node. An example of this recommendation is in Figure 22. The PD_IN node is shielded with a coplanar PD_GND trace. The photodiode cathode should be entirely shielded with the PD_GND shield, which is also the photodiode anode. The PD_GND pin should only be attached to the PCB Ground in only one point.

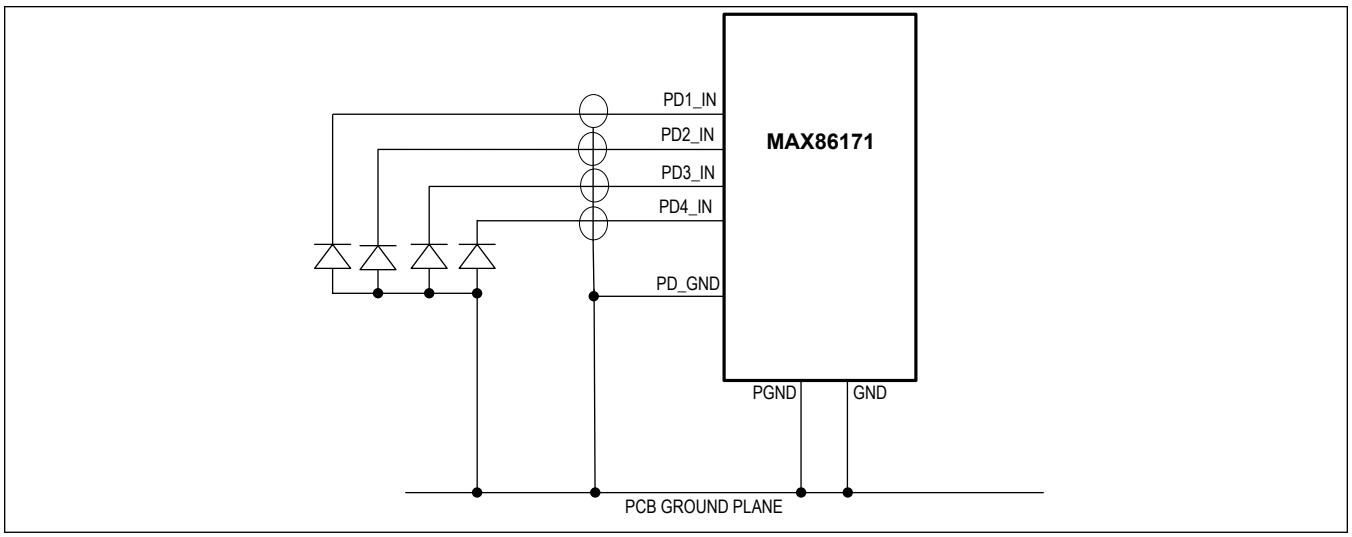


Figure 22. PCB Layout Recommendation

Register Map

User Register Map

ADDRESS	NAME	MSB							LSB
Status									
0x00	Status 1[7:0]	A_FULL	FRAME_RDY	FIFO_DATA_RDY	ALC_OVF	EXP_OVF	THRESH2_HILO	THRESH1_HILO	PWR_RDY
0x01	Status 2[7:0]	LED9_COMPB	VDD_OOR	–	–	–	INVALID_CFG	–	–
0x02	Status 3[7:0]	LED8_COMPB	LED7_COMPB	LED6_COMPB	LED5_COMPB	LED4_COMPB	LED3_COMPB	LED2_COMPB	LED1_COMPB
FIFO									
0x04	FIFO Write Pointer[7:0]	FIFO_WR_PTR[7:0]							
0x05	FIFO Read Pointer[7:0]	FIFO_RD_PTR[7:0]							
0x06	FIFO Counter 1[7:0]	FIFO_DATA_COUNT_MSB	OVF_COUNTER[6:0]						
0x07	FIFO Counter 2[7:0]	FIFO_DATA_COUNT_LSB[7:0]							
0x08	FIFO Data Register[7:0]	FIFO_DATA[7:0]							
0x09	FIFO Configuration 1[7:0]	FIFO_A_FULL[7:0]							
0x0A	FIFO Configuration 2[7:0]	–	–	–	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
System Control									
0x0C	System Configuration 1[7:0]	MEAS9_EN	SW_FORCE_SYNC	SYNC_MODE[1:0]		PPG2_PWRDN	PPG1_PWRDN	SHDN	RESET
0x0D	System Configuration 2[7:0]	MEAS8_EN	MEAS7_EN	MEAS6_EN	MEAS5_EN	MEAS4_EN	MEAS3_EN	MEAS2_EN	MEAS1_EN
0x0E	System Configuration 3[7:0]	–	–	–	ALC_DISABLE	–	–	COLLECT_RAW_DATA	MEAS1_CONFIG_SEL
0x0F	Photodiode Bias[7:0]	PD4_BIAS[1:0]		PD3_BIAS[1:0]		PD2_BIAS[1:0]		PD1_BIAS[1:0]	
0x10	Pin Functional Configuration[7:0]	–	–	–	INT2_FCFG[1:0]		–	–	TRIG_ICFG
0x11	Output Pin Configuration[7:0]	–	–	–	INT2_OCFG[1:0]		INT1_OCFG[1:0]		–
Frame Rate Clock									
0x15	FR Clock Frequency Select[7:0]	–	–	FR_CLK_SEL	FR_CLK_FINE_TUNE[4:0]				
0x16	FR Clock Divider MSB[7:0]	–	FR_CLK_DIV_H[6:0]						
0x17	FR Clock Divider LSB[7:0]	FR_CLK_DIV_L[7:0]							

ADDRESS	NAME	MSB							LSB
MEAS1 Setup									
0x18	MEAS1 Selects[7:0]	–	MEAS1_AMB	MEAS1_DRVC[1:0]		MEAS1_DRVB[1:0]		MEAS1_DRVA[1:0]	
0x19	MEAS1 Configuration 1[7:0]	–	MEAS1_PPG2_PDSEL	MEAS1_PPG1_PDSEL	MEAS1_TINT[1:0]		MEAS1_AVER[2:0]		
0x1A	MEAS1 Configuration 2[7:0]	MEAS1_SINC3_SEL	MEAS1_FILT_SEL	MEAS1_LED_RGE[1:0]		MEAS1_PPG2_ADC_RGE[1:0]		MEAS1_PPG1_ADC_RGE[1:0]	
0x1B	MEAS1 Configuration 3[7:0]	MEAS1_PD_SETLNG[1:0]		MEAS1_LED_SETLNG[1:0]		MEAS1_PPG2_DACOFF[1:0]		MEAS1_PPG1_DACOFF[1:0]	
0x1C	MEAS1 DRVA Current[7:0]	MEAS1_DRVA_PA[7:0]							
0x1D	MEAS1 DRVB Current[7:0]	MEAS1_DRVB_PA[7:0]							
0x1E	MEAS1 DRVC Current[7:0]	MEAS1_DRVC_PA[7:0]							
MEAS2 Setup									
0x20	MEAS2 Selects[7:0]	–	MEAS2_AMB	MEAS2_DRVC[1:0]		MEAS2_DRVB[1:0]		MEAS2_DRVA[1:0]	
0x21	MEAS2 Configuration 1[7:0]	–	MEAS2_PPG2_PDSEL	MEAS2_PPG1_PDSEL	MEAS2_TINT[1:0]		MEAS2_AVER[2:0]		
0x22	MEAS2 Configuration 2[7:0]	MEAS2_SINC3_SEL	MEAS2_FILT_SEL	MEAS2_LED_RGE[1:0]		MEAS2_PPG2_ADC_RGE[1:0]		MEAS2_PPG1_ADC_RGE[1:0]	
0x23	MEAS2 Configuration 3[7:0]	MEAS2_PD_SETLNG[1:0]		MEAS2_LED_SETLNG[1:0]		MEAS2_PPG1_DACOFF[1:0]		MEAS2_PPG1_DACOFF[1:0]	
0x24	MEAS2 DRVA Current[7:0]	MEAS2_DRVA_PA[7:0]							
0x25	MEAS2 DRVB Current[7:0]	MEAS2_DRVB_PA[7:0]							
0x26	MEAS2 DRVC Current[7:0]	MEAS2_DRVC_PA[7:0]							
MEAS3 Setup									
0x28	MEAS3 Selects[7:0]	–	MEAS3_AMB	MEAS3_DRVC[1:0]		MEAS3_DRVB[1:0]		MEAS3_DRVA[1:0]	
0x29	MEAS3 Configuration 1[7:0]	–	MEAS3_PPG2_PDSEL	MEAS3_PPG1_PDSEL	MEAS3_TINT[1:0]		MEAS3_AVER[2:0]		
0x2A	MEAS3 Configuration 2[7:0]	MEAS3_SINC3_SEL	MEAS3_FILT_SEL	MEAS3_LED_RGE[1:0]		MEAS3_PPG2_ADC_RGE[1:0]		MEAS3_PPG1_ADC_RGE[1:0]	
0x2B	MEAS3 Configuration 3[7:0]	MEAS3_PD_SETLNG[1:0]		MEAS3_LED_SETLNG[1:0]		MEAS3_PPG2_DACOFF[1:0]		MEAS3_PPG1_DACOFF[1:0]	
0x2C	MEAS3 DRVA Current[7:0]	MEAS3_DRVA_PA[7:0]							
0x2D	MEAS3 DRVB Current[7:0]	MEAS3_DRVB_PA[7:0]							

ADDRESS	NAME	MSB							LSB
0x2E	MEAS3 DRVC Current[7:0]	MEAS3_DRVC_PA[7:0]							
MEAS4 Setup									
0x30	MEAS4 Selects[7:0]	–	MEAS4_AMB	MEAS4_DRVC[1:0]		MEAS4_DRVB[1:0]		MEAS4_DRVA[1:0]	
0x31	MEAS4 Configuration 1[7:0]	–	MEAS4_PPG2_PDSEL	MEAS4_PPG1_PDSEL	MEAS4_TINT[1:0]		MEAS4_AVER[2:0]		
0x32	MEAS4 Configuration 2[7:0]	MEAS4_SINC3_SEL	MEAS4_FILT_SEL	MEAS4_LED_RGE[1:0]		MEAS4_PPG2_ADC_RGE[1:0]		MEAS4_PPG1_ADC_RGE[1:0]	
0x33	MEAS4 Configuration 3[7:0]	MEAS4_PD_SETLNG[1:0]		MEAS4_LED_SETLNG[1:0]		MEAS4_PPG2_DACOFF[1:0]		MEAS4_PPG1_DACOFF[1:0]	
0x34	MEAS4 DRVA Current[7:0]	MEAS4_DRVA_PA[7:0]							
0x35	MEAS4 DRVB Current[7:0]	MEAS4_DRVB_PA[7:0]							
0x36	MEAS4 DRVC Current[7:0]	MEAS4_DRVC_PA[7:0]							
MEAS5 Setup									
0x38	MEAS5 Selects[7:0]	–	MEAS5_AMB	MEAS5_DRVC[1:0]		MEAS5_DRVB[1:0]		MEAS5_DRVA[1:0]	
0x39	MEAS5 Configuration 1[7:0]	–	MEAS5_PPG2_PDSEL	MEAS5_PPPG1_PDSEL	MEAS5_TINT[1:0]		MEAS5_AVER[2:0]		
0x3A	MEAS5 Configuration 2[7:0]	MEAS5_SINC3_SEL	MEAS5_FILT_SEL	MEAS5_LED_RGE[1:0]		MEAS5_PPG2_ADC_RGE[1:0]		MEAS5_PPG1_ADC_RGE[1:0]	
0x3B	MEAS5 Configuration 3[7:0]	MEAS5_PD_SETLNG[1:0]		MEAS5_LED_SETLNG[1:0]		MEAS5_PPG2_DACOFF[1:0]		MEAS5_PPG1_DACOFF[1:0]	
0x3C	MEAS5 DRVA Current[7:0]	MEAS5_DRVA_PA[7:0]							
0x3D	MEAS5 DRVB Current[7:0]	MEAS5_DRVB_PA[7:0]							
0x3E	MEAS5 DRVC Current[7:0]	MEAS5_DRVC_PA[7:0]							
MEAS6 Setup									
0x40	MEAS6 Selects[7:0]	–	MEAS6_AMB	MEAS6_DRVC[1:0]		MEAS6_DRVB[1:0]		MEAS6_DRVA[1:0]	
0x41	MEAS6 Configuration 1[7:0]	–	MEAS6_PPG2_PDSEL	MEAS6_PPG1_PDSEL	MEAS6_TINT[1:0]		MEAS6_AVER[2:0]		
0x42	MEAS6 Configuration 2[7:0]	MEAS6_SINC3_SEL	MEAS6_FILT_SEL	MEAS6_LED_RGE[1:0]		MEAS6_PPG2_ADC_RGE[1:0]		MEAS6_PPG1_ADC_RGE[1:0]	
0x43	MEAS6 Configuration 3[7:0]	MEAS6_PD_SETLNG[1:0]		MEAS6_LED_SETLNG[1:0]		MEAS6_PPG2_DACOFF[1:0]		MEAS6_PPG1_DACOFF[1:0]	
0x44	MEAS6 DRVA Current[7:0]	MEAS6_DRVA_PA[7:0]							

ADDRESS	NAME	MSB							LSB
0x45	MEAS6 DRVB Current[7:0]	MEAS6_DRVB_PA[7:0]							
0x46	MEAS6 DRVC Current[7:0]	MEAS6_DRVC_PA[7:0]							
MEAS7 Setup									
0x48	MEAS7 Selects[7:0]	–	MEAS7_AMB	MEAS7_DRVC[1:0]		MEAS7_DRVB[1:0]		MEAS7_DRVA[1:0]	
0x49	MEAS7 Configuration 1[7:0]	–	MEAS7_PPG2_PDSEL	MEAS7_PPG1_PDSEL	MEAS7_TINT[1:0]		MEAS7_AVER[2:0]		
0x4A	MEAS7 Configuration 2[7:0]	MEAS7_SINC3_SEL	MEAS7_FILT_SEL	MEAS7_LED_RGE[1:0]		MEAS7_PPG2_ADC_RGE[1:0]		MEAS7_PPG1_ADC_RGE[1:0]	
0x4B	MEAS7 Configuration 3[7:0]	MEAS7_PD_SETLNG[1:0]		MEAS7_LED_SETLNG[1:0]		MEAS7_PPG2_DACOFF[1:0]		MEAS7_PPG1_DACOFF[1:0]	
0x4C	MEAS7 DRVA Current[7:0]	MEAS7_DRVA_PA[7:0]							
0x4D	MEAS7 DRVB Current[7:0]	MEAS7_DRVB_PA[7:0]							
0x4E	MEAS7 DRVC Current[7:0]	MEAS7_DRVC_PA[7:0]							
MEAS8 Setup									
0x50	MEAS8 Selects[7:0]	–	MEAS8_AMB	MEAS8_DRVC[1:0]		MEAS8_DRVB[1:0]		MEAS8_DRVA[1:0]	
0x51	MEAS8 Configuration 1[7:0]	–	MEAS8_PPG2_PDSEL	MEAS8_PPG1_PDSEL	MEAS8_TINT[1:0]		MEAS8_AVER[2:0]		
0x52	MEAS8 Configuration 2[7:0]	MEAS8_SINC3_SEL	MEAS8_FILT_SEL	MEAS8_LED_RGE[1:0]		MEAS8_PPG2_ADC_RGE[1:0]		MEAS8_PPG1_ADC_RGE[1:0]	
0x53	MEAS8 Configuration 3[7:0]	MEAS8_PD_SETLNG[1:0]		MEAS8_LED_SETLNG[1:0]		MEAS8_PPG2_DACOFF[1:0]		MEAS8_PPG1_DACOFF[1:0]	
0x54	MEAS8 DRVA Current[7:0]	MEAS8_DRVA_PA[7:0]							
0x55	MEAS8 DRVB Current[7:0]	MEAS8_DRVB_PA[7:0]							
0x56	MEAS8 DRVC Current[7:0]	MEAS8_DRVC_PA[7:0]							
MEAS9 Setup									
0x58	MEAS9 Selects[7:0]	–	MEAS9_AMB	MEAS9_DRVC[1:0]		MEAS9_DRVB[1:0]		MEAS9_DRVA[1:0]	
0x59	MEAS9 Configuration 1[7:0]	–	MEAS9_PPG2_PDSEL	MEAS9_PPG1_PDSEL	MEAS9_TINT[1:0]		MEAS9_AVER[2:0]		
0x5A	MEAS9 Configuration 2[7:0]	MEAS9_SINC3_SEL	MEAS9_FILT_SEL	MEAS9_LED_RGE[1:0]		MEAS9_PPG2_ADC_RGE[1:0]		MEAS9_PPG1_ADC_RGE[1:0]	
0x5B	MEAS9 Configuration 3[7:0]	MEAS9_PD_SETLNG[1:0]		MEAS9_LED_SETLNG[1:0]		MEAS9_PPG2_DACOFF[1:0]		MEAS9_PPG1_DACOFF[1:0]	

ADDRESS	NAME	MSB							LSB
0x5C	MEAS9 DRVA Current[7:0]	MEAS9_DRVA_PA[7:0]							
0x5D	MEAS9 DRVB Current[7:0]	MEAS9_DRVB_PA[7:0]							
0x5E	MEAS9 DRVC Current[7:0]	MEAS9_DRVC_PA[7:0]							
Threshold Interrupts									
0x68	THRESHOLD MEAS SEL[7:0]	THRESH2_MEAS_SEL[3:0]				THRESH1_MEAS_SEL[3:0]			
0x69	THRESHOLD HYST[7:0]	THRESH2_PPG_SEL	THRESH1_PPG_SEL	–	TIME_HYST[1:0]		LEVEL_HYST[2:0]		
0x6A	PPG HI THRESHOLD1[7:0]	THRESHOLD1_UPPER[7:0]							
0x6B	PPG LO THRESHOLD1[7:0]	THRESHOLD1_LOWER[7:0]							
0x6C	PPG HI THRESHOLD2[7:0]	THRESHOLD2_UPPER[7:0]							
0x6D	PPG LO THRESHOLD2[7:0]	THRESHOLD2_LOWER[7:0]							
Picket Fence									
0x70	Picket Fence Measurement Select[7:0]	PPG2_PF_MEAS_SEL[3:0]				PPG1_PF_MEAS_SEL[3:0]			
0x71	Picket Fence Configuration[7:0]	–	PF_ORDER	IIR_TC[1:0]		IIR_INIT_VALUE[1:0]		THRESHOLD_SIGMA_MULT[1:0]	
Interrupt Enables									
0x78	Interrupt1 Enable 1[7:0]	A_FULL_EN1	FRAME_RDY_EN1	FIFO_DATA_RDY_EN1	ALC_OVF_EN1	EXP_OVF_EN1	THRESH2_HILO_EN1	THRESH1_HILO_EN1	LED_TX_EN1
0x79	Interrupt1 Enable 2[7:0]	LED9_COMPB_EN1	VDD_OOR_EN1	–	–	–	INVALID_CFG_EN1	–	–
0x7A	Interrupt1 Enable 3[7:0]	LED8_COMPB_EN1	LED7_COMPB_EN1	LED6_COMPB_EN1	LED5_COMPB_EN1	LED4_COMPB_EN1	LED3_COMPB_EN1	LED2_COMPB_EN1	LED1_COMPB_EN1
0x7C	Interrupt2 Enable 1[7:0]	A_FULL_EN2	FRAME_RDY_EN2	FIFO_DATA_RDY_EN2	ALC_OVF_EN2	EXP_OVF_EN2	THRESH2_HILO_EN2	THRESH1_HILO_EN2	LED_TX_EN2
0x7D	Interrupt2 Enable 2[7:0]	LED9_COMPB_EN2	VDD_OOR_EN2	–	–	–	INVALID_CFG_EN2	–	–
0x7E	Interrupt2 Enable 3[7:0]	LED8_COMPB_EN2	LED7_COMPB_EN2	LED6_COMPB_EN2	LED5_COMPB_EN2	LED4_COMPB_EN2	LED3_COMPB_EN2	LED2_COMPB_EN2	LED1_COMPB_EN2
Part ID									
0xFF	Part ID[7:0]	PART_ID[7:0]							

Register Details

Status 1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL	FRAME_RDY	FIFO_DATA_RDY	ALC_OVF	EXP_OVF	THRESH2_HILO	THRESH1_HILO	PWR_RDY
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

A_FULL

The A_FULL bit is set to 1 when the FIFO has reached the threshold programmed in the FIFO_A_FULL register. This is a read-only bit. This bit is cleared when the Status 1 Register is read. It is also cleared when the FIFO Data Register (0x08) is read if FIFO_STAT_CLR = 1.

VALUE	ENUMERATION	DECODE
0	NORMAL	Normal Operation
1	ASSERTED	Indicates that the FIFO buffer has reached the threshold set by FIFO_A_FULL[7:0].

FRAME_RDY

A frame consists of FIFO data for all the PPG ADC conversions for the sequence programmed in the MEASn (n = 1 to 9) enable registers. FRAME_RDY bit is set to 1 when a full frame conversion has completed. This is a read-only bit and is cleared by reading the Status 1 Register (0x00). It is also cleared by reading the FIFO Data Register if FIFO_STAT_CLR = 1.

VALUE	ENUMERATION	DECODE
0	NORMAL	Normal Operation
1	ASSERTED	This interrupt triggers when a complete sample is available in the FIFO.

FIFO_DATA_RDY

The FIFO_DATA_RDY bit is set to 1 when new data is available in the FIFO. This is a read-only bit and is cleared by reading the Status 1 register (0x00). It is also cleared by reading the FIFO Data Register if FIFO_STAT_CLR = 1

VALUE	ENUMERATION	DECODE
0	NORMAL	Normal Operation
1	ASSERTED	There is new data in the FIFO

ALC_OVF

The ALC_OVF bit is set to 1 when a dark current measurement is either underranged or overranged for any of the assigned measurements. This is a read-only bit, and is cleared by reading the Status 1 register (0x00). A measurement is overranged if it is positive full-scale (0x7FFFF, 524287), and underranged if it is less than negative full-scale/4 (< 0xE0000, -131072).

VALUE	ENUMERATION	DECODE
0	NORMAL	Normal Operation
1	ASSERTED	This interrupt triggers when the ambient light cancellation function of the photodiode has reached its maximum limit due to overflow, and therefore, ambient light is affecting the output of the ADC.

EXP_OVF

The EXP_OVF bit is set to 1 when an exposure current measurement is either underranged or overranged. It is also set

to 1 if a photodiode forward bias is detected. This is a read-only bit, and is cleared by reading the Status 1 register (0x00). A measurement is overranged if it is positive full-scale (0x7FFFF, 524287), and underrange if it is less than negative full-scale/4 (< 0xE0000, -131072).

VALUE	ENUMERATION	DECODE
0	NORMAL	Normal Operation
1	ASSERTED	This interrupt triggers when the exposure signal has reached its maximum limit due to overflow.

THRESH2_HILO

The THRESH2_HILO bit is set to 1 when the THRESH2_MEAS instance as defined qualifies as above THRESHOLD2_UPPER or below THRESHOLD2_LOWER. This is a read-only bit and is cleared by reading the Status 1 register (0x00).

See the Threshold Detect Function section for a complete explanation of how the two threshold instances operate.

VALUE	ENUMERATION	DECODE
0	NORMAL	ADC reading is below the defined THRESHOLD2_UPPER level AND above THRESHOLD2_LOWER level.
1	ASSERTED	ADC reading is above the defined THRESHOLD2_UPPER level OR below THRESHOLD2_LOWER level.

THRESH1_HILO

The THRESH1_HILO bit is set to 1 when the THRESH1_MEAS instance as defined qualifies as above THRESHOLD1_UPPER or below THRESHOLD1_LOWER. This is a read-only bit and is cleared by reading the Status 1 register (0x00).

See the Threshold Detect Function section for a complete explanation of how the two threshold instances operate.

VALUE	ENUMERATION	DECODE
0	NORMAL	ADC reading is below the defined THRESHOLD1_UPPER level AND above THRESHOLD1_LOWER level.
1	ASSERTED	ADC reading is above the defined THRESHOLD1_UPPER level OR below THRESHOLD1_LOWER level.

PWR_RDY

The PWR_RDY bit is set to 1 when V_{DD} goes below the undervoltage lockout (UVLO) threshold, which is approximately 1.3V. If this condition occurs, all registers within the MAX86171 are reset to their PORb state. This bit is not triggered by a soft-reset. This is a read-only bit and is cleared when the Status 1 register is read, or by setting the SHDN bit to 1.

PWR_RDY is a non-maskable interrupt. So it gets asserted on both INT1 and INT2.

VALUE	ENUMERATION	DECODE
0	NORMAL	Normal Operation
1	ASSERTED	Indicates that V_{DD_DIG} or V_{DD_ANA} went below the UVLO threshold.

Status 2 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	LED9_COMPB	VDD_OOR	–	–	–	INVALID_CFG	–	–
Reset	0b0	0b0	–	–	–	0b0	–	–
Access Type	Read Only	Read Only	–	–	–	Read Only	–	–

LED9_COMPB

LEDx (x = 1 to 9) is not compliant. If the LEDx_DRV pin voltage drops below the compliance voltage threshold at the end of each exposure interval, the LEDx_COMPB status bit is asserted. LEDx_COMPB is a read-only bit. It is cleared when the corresponding status register is read.

VALUE	ENUMERATION	DECODE
0	NORMAL	LED9_DRV pin has sufficient voltage for the driver
1	ASSERTED	LEDx_DRV pin voltage is below compliance. Power supply rejection on LEDx is degraded and LEDx current is inaccurate.

VDD_OOR

VDD_OOR bit is set to 1 when VDD_DIG is out of range 1.65V < V_{DD_DIG} < 2.05V. The detection circuitry has a 10ms time delay and continues to trigger as long as the V_{DD_DIG} is out of range. VDD_OOR is a read-only bit and is cleared when the Status 2 register is read.

VALUE	ENUMERATION	DECODE
0	NORMAL	Normal Operation
1	ASSERTED	Indicates that V_{DD_DIG} is greater than 2.05V or less than 1.65V.

INVALID_CFG

INVALID_CFG is set to 1 when the Frame Rate programmed using the clock dividers FR_CLK_DIV_H[6:0] and FR_CLK_DIV_L[7:0] is too fast to accommodate the measurement sequences enabled in a frame. This is a read-only bit and it gets cleared when the Status 2 register is read.

VALUE	ENUMERATION	DECODE
0	NORMAL	Configuration timing is valid.
1	ASSERTED	Configuration timing is not valid.

Status 3 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	LED8_COMPB	LED7_COMPB	LED6_COMPB	LED5_COMPB	LED4_COMPB	LED3_COMPB	LED2_COMPB	LED1_COMPB
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

LED8_COMPB

See LED9_COMPB for details.

LED7_COMPB

See LED9_COMPB for details.

LED6_COMPB

See LED9_COMPB for details.

LED5_COMPB

See LED9_COMPB for details.

LED4_COMPB

See LED9_COMPB for details.

LED3_COMPB

See LED9_COMPB for details.

LED2_COMPB

See LED9_COMPB for details.

LED1_COMPB

See LED9_COMPB for details.

FIFO Write Pointer (0x04)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_WR_PTR[7:0]							
Reset	0x0							
Access Type	Read Only							

FIFO_WR_PTR

FIFO_WR_PTR[7:0] points to the location where the next sample will be written. This pointer advances for each sample pushed on to the circular FIFO.

Refer to the FIFO Description section for details.

FIFO Read Pointer (0x05)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_RD_PTR[7:0]							
Reset	0x0							
Access Type	Write, Read, Dual							

FIFO_RD_PTR

FIFO_RD_PTR[7:0] points to the location from where the processor gets the next sample from the FIFO using the serial interface. This advances each time a sample is popped from the circular FIFO. The processor can also write to this pointer after reading the samples. This allows rereading (or retrying) samples from the FIFO. However, writing to FIFO_RD_PTR[7:0] can have adverse effects if it results in the FIFO being almost full.

Refer to the FIFO Description section for details.

FIFO Counter 1 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT_MSB	OVF_COUNTER[6:0]						
Reset	0x0	0x0						
Access Type	Read Only	Read Only						

FIFO_DATA_COUNT_MSB

FIFO_DATA_COUNT_MSB is a read-only register that holds the most significant bit of the number of data items

available in the FIFO for the host to read. The lower 8 bits are in the FIFO_DATA_COUNT_LSB[7:0] register.

The 9-bit FIFO_DATA_COUNT[8:0] register is comprised of FIFO_DATA_COUNT_MSB and FIFO_DATA_COUNT_LSB[7:0] registers. FIFO_DATA_COUNT[8:0] increments when a new data item is pushed to the FIFO, and decrements when the host reads a data item from the FIFO.

Refer to the FIFO Description section for details.

OVF_COUNTER

When FIFO is full any new samples result in new or old samples getting lost depending on FIFO_RO. OVF_COUNTER[6:0] counts the number of samples lost. It saturates at 0x7F. This is a read-only register.

Refer to the FIFO Description section for details.

FIFO Counter 2 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

FIFO_DATA_COUNT_LSB

FIFO_DATA_COUNT_LSB[7:0] is a read-only register that holds the lower 8 bits of the number of data items available in the FIFO for the host to read.

See the FIFO_DATA_COUNT_MSB register description for details.

FIFO Data Register (0x08)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA[7:0]							
Reset	0x0							
Access Type	Read Only							

FIFO_DATA

FIFO_DATA[7:0] is a read-only register and is used to get data from the FIFO.

Refer to the FIFO Description section for details.

FIFO Configuration 1 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_A_FULL[7:0]							
Reset	0x7F							
Access Type	Write, Read							

FIFO_A_FULL

FIFO_A_FULL[7:0] indicates how many new samples can be written to the FIFO before the interrupt is asserted. For example, if set to 0x0F, the interrupt triggers when there are 15 empty spaces left (241 entries).

Refer to the FIFO Description section for details.

FIFO_A_FULL[7:0]	FREE SPACE BEFORE INTERRUPT	# OF SAMPLES IN FIFO
0	0	256
1	1	255
2	2	254
3	3	253
----	----	----
254	254	2
255	255	1

FIFO Configuration 2 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
Reset	–	–	–	0b0	0b1	0b0	0b0	–
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	–

FLUSH_FIFO

When FLUSH_FIFO bit is set to ‘1’, the FIFO gets flushed, FIFO_WR_PTR[7:0] and FIFO_RD_PTR[7:0] are reset to zero and FIFO_DATA_COUNT[8:0] becomes 0. The contents of the FIFO are lost. FIFO_FLUSH is a self-clearing bit.

Refer to the FIFO Description section for details.

FIFO_STAT_CLR

When FIFO_STAT_CLR is set to 0, A-FULL, FRAME_RDY and FIFO_DATA_RDY bits and the corresponding interrupts get cleared when Status 1 register is read. When FIFO_STAT_CLR is set to 1, A-FULL, FRAME_RDY and FIFO_DATA_RDY bits and the corresponding interrupts get cleared when the Status 1 register is read or when FIFO_DATA[7:0] register is read.

Refer to the FIFO Description section for details.

VALUE	ENUMERATION	DECODE
0	RD_DATA_NOCLR	A_FULL, FRAME_RDY and FIFO_DATA_RDY status and interrupts do not get cleared by FIFO_DATA[7:0] register read. They get cleared by a status register read.
1	RD_DATA_CLR	A_FULL, FRAME_RDY and FIFO_DATA_RDY status and interrupts get cleared by FIFO_DATA[7:0] register read or status register read (Default)

A_FULL_TYPE

A_FULL_TYPE defines the behavior of the A_FULL interrupt. When A_FULL_TYPE is set to 0, A_FULL is asserted everytime the FIFO Almost Full condition is detected. When A_FULL_TYPE is set to 1, A_FULL is asserted only for any new A_FULL condition.

Refer to the FIFO Description section for details.

VALUE	ENUMERATION	DECODE
0	AFULL_RPT	A_FULL interrupt gets asserted when the A_FULL condition is detected. It is cleared by status register read, but reasserts for every sample if the A_FULL condition persists.
1	AFULL_ONCE	A_FULL interrupt gets asserted only when the A_FULL condition is detected. The interrupt gets cleared on status register read, and does not reassert for every sample until a new A_FULL condition is detected.

FIFO_RO

The FIFO_RO bit controls the behavior of the FIFO when the FIFO becomes completely filled with data. Push to FIFO is enabled when FIFO is full if FIFO_RO = 1 and old samples are lost. Both FIFO_WR_PTR and FIFO_RD_PTR increment for each sample after the FIFO is full. Push to FIFO is disabled when FIFO is full if FIFO_RO = 0 and new samples are lost. FIFO_WR_PTR and FIFO_RD_PTR do not increment until a sample is read from the FIFO.

Refer to the FIFO Description section for details.

VALUE	ENUMERATION	DECODE
0	STOP	The FIFO stops on full.
1	PUSH	The FIFO automatically rolls over on full.

System Configuration 1 (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_EN	SW_FORCE_SYNC	SYNC_MODE[1:0]		PPG2_PWRDN	PPG1_PWRDN	SHDN	RESET
Reset	0b0	0b0	0x0		0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

MEAS9_EN

Set MEASn_EN (n = 1 to 9) to 0 to disable measurement programmed in MEASn_SETUP registers in the measurement sequence. Set MEASn_EN to 1 to enable measurement programmed in MEASn_SETUP registers in the measurement sequence. The sequence consists of all the enabled measurements starting from MEAS1_EN to MEAS9_EN.

MEASn_EN (n = 1 to 9)	ENUMERATION	DECODE
0	DISABLE	Disable Measurement n
1	ENABLE	Enable Measurement n

SW_FORCE_SYNC

Writing a 1 to this bit aborts the current Frame and starts a new Frame. This is a self-clearing bit.

SYNC_MODE

SYNC_MODE[1:0] bits are used for programming the frame synchronization modes as described in the table below.

Modes of operation:

SYNC_MODE[1:0]	OPERATING MODES	TRIG INPUT	DESCRIPTION
0, 3	Internal Frame Sync	Not Used	The device is in free-running mode. Frame-sync pulses are generated internally using the internal 32kHz/32.768kHz frame clock and the frame rate divider set by FR_CLK_DIV. The ADC Sync signals are generated internally using the 10MHz ADC clock.
1	External Frame Sync	Frame Sync	The device is in one-shot mode. A frame cycle begins upon receipt of an active edge on the TRIG input. A frame cycle consists of a power-up cycle and the execution of each enabled measurement. The ADC Sync signals are generated internally using the10MHz ADC clock. The internal 32kHz/32.768kHz frame clock is disabled.

2	External Clock	EXT_CLK, External Frame Rate Clock	The internal 32kHz/32.768kHz frame clock is disabled and the internal frame clock is driven by the TRIG pin. Frame-sync pulses are generated internally using the external TRIG input 32kHz/32.768kHz frame clock and the frame rate divider set by FR_CLK_DIV. The ADC Sync signals are generated internally using the 10MHz ADC clock. Start of sampling process can be controlled by an SPI software sync command, which zeros out the frame rate divider and restarts the frame counting process.The device then advances with the external TRIG input clock. Subsequent software Sync commands abort the current frame and restart a new Frame.

PPG2_PWRDN

When PPG2_PWRDN is set 0, the optical channel 2 is enabled. When PPG2_PWRDN is set to 1, this channel is powered down to save power.

PPG2_PD	ENUMERATION	DECODE
0	ON	Optical Channel 2 is enabled.
1	OFF	Optical Channel 2 is powered down.

PPG1_PWRDN

When PPG1_PWRDN is set 0, the optical channel 1 is enabled. When PPG1_PWRDN is set to 1, this channel is powered down to save power.

PPG1_PD	ENUMERATION	DECODE
0	ON	Optical Channel 1 is enabled
1	OFF	Optical Channel 1 is powered down

SHDN

The part can be put into a power-save mode by setting SHDN bit to 1. While in power-save mode, all configuration registers retain their values and write/read operations function as normal. All interrupts are cleared to zero in this mode. Set SHDN to 0 to put the part in normal mode.

VALUE	ENUMERATION	DECODE
0	NORMAL	The part is in normal operation. No action is taken.
1	SHUTDOWN	The part can be put into power-save mode by writing a ‘1’ to this bit. While in this mode all configuration registers remain accessible and retain their data. ADC conversion data contained in the registers are previous values. Writeable registers also remain accessible in shutdown. All interrupts are cleared. In this mode, the oscillator is shut down and the part draws minimum current. If this bit is asserted during an active conversion then the conversion is aborted.

RESET

When the RESET bit is set to 1, the MAX86171 undergoes a forced power-on-reset sequence. All configuration, threshold, and data registers are reset to their power-on state. This bit then automatically becomes ‘0’ after the reset sequence is completed.

VALUE	ENUMERATION	DECODE
0	NORMAL	The part is in normal operation. No action is taken.
1	RESET	The MAX86171 undergoes a forced power-on-reset sequence. All configuration, threshold, and data registers are reset to their power-on state. This bit then automatically becomes ‘0’ after the reset sequence is completed.

System Configuration 2 (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_EN	MEAS7_EN	MEAS6_EN	MEAS5_EN	MEAS4_EN	MEAS3_EN	MEAS2_EN	MEAS1_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

MEAS8_EN

See MEAS9_EN for details.

MEAS7_EN

See MEAS9_EN for details.

MEAS6_EN

See MEAS9_EN for details.

MEAS5_EN

See MEAS9_EN for details.

MEAS4_EN

See MEAS9_EN for details.

MEAS3_EN

See MEAS9_EN for details.

MEAS2_EN

See MEAS9_EN for details.

MEAS1_EN

See MEAS9_EN for details.

System Configuration 3 (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ALC_DISABLE	–	–	COLLECT_RAW_DATA	MEAS1_CONFIG_SEL
Reset	–	–	–	0b0	–	–	0b0	0b0
Access Type	–	–	–	Write, Read	–	–	Write, Read	Write, Read

ALC_DISABLE

The ALC_DISABLE bit inhibits the front-end analog ambient light cancellation circuit. This bit does not alter the backend ambient subtraction.

VALUE	DECODE
0	Front-end ambient light cancelation is enabled.
1	Front-end ambient light cancelation is disabled.

COLLECT_RAW_DATA

Each measurement consists of an interleaved of N+1 DARK conversions and N exposure conversions, where N = 2^{SMP_AVE}. If COLLECT_RAW_DATA = 0, the weighted average of all ambient corrected exposures is computed and the results pushed to the FIFO. When COLLECT_RAW_DATA = 1, the weighted average is not computed and each raw conversion is pushed to the FIFO. This mode inhibits the back-end ambient cancellation as well as the weighted averaging. This allows for the use of a customized ambient rejection algorithm in a host microcontroller.

When COLLECT_RAW_DATA = 1, Picket Fence detect is disabled.

COLLECT_RAW_DATA	ENUMERATION	DECODE
0	COMPUTED	Capture computed data for each burst in the FIFO.
1	RAW	Capture raw data for each DARK and LED conversion in the FIFO.

MEAS1_CONFIG_SEL

When the MEAS1_CONFIG_SEL bit is set to 0, all enabled measurements use the unique configuration defined in each MEASn setup.

When the MEAS1_CONFIG_SEL bit is set to 1, all enabled measurements use the following configuration settings defined in MEAS1 setup. This allows for a reduced setup configuration.

MEAS1_FILT_SEL

MEAS1_TINT

MEAS1_AVER

MEAS1_PD_SETLNG

MEAS1_LED_SETLNG

MEAS1_PPG1_PDSEL

MEAS1_PPG2_PDSEL

MEAS1_LED_RGE

MEAS1_PPG1_ADC_RGE

MEAS1_PPG2_ADC_RGE

VALUE	ENUMERATION	DECODE
0	SPECIFIC_CFG	Use measurement specific configuration defined in each measurement register.
1	MEAS1_CFG	Use MEAS1 configuration for all enabled measurements.

Photodiode Bias (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	PD4_BIAS[1:0]		PD3_BIAS[1:0]		PD2_BIAS[1:0]		PD1_BIAS[1:0]	
Reset	0x1		0x1		0x1		0x1	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

PD4_BIAS

See the Photodiode Biasing section for more information.

PDx_BIAS[1:0] (x = 1 TO 4)	PHOTODIODE CAPACITANCE
0	Not recommended
1	0pF to 125pF (POR default)
2	125pF to 250pF

PDx_BIAS[1:0] (x = 1 TO 4)	PHOTODIODE CAPACITANCE
3	250pF to 500pF

PD3_BIAS

See PD4_BIAS[1:0] for details.

PD2_BIAS

See PD4_BIAS[1:0] for details.

PD1_BIAS

See PD4_BIAS[1:0] for details.

Pin Functional Configuration (0x10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	INT2_FCFG[1:0]		–	–	TRIG_ICFG
Reset	–	–	–	0x0		–	–	0b0
Access Type	–	–	–	Write, Read		–	–	Write, Read

INT2_FCFG

The INT2_FCFG[1:0] bit sets the functional configuration of the INT2 pin. This interrupt can be configured to be disabled, cleared on status byte read or to self-clear after two optional prescribed times.

VALUE	DECODE
0	Disabled
1	INT2 is enabled and is cleared upon reading of any status register or FIFO
2	INT2 is enabled and is self-clearing after 30.5µs
3	INT2 is enabled and is self-clearing after 244µs

TRIG_ICFG

The TRIG_ICFG bit sets the input active edge of the TRIG pin. Active edge is the edge for which the TRIG input responds.

VALUE	DECODE
0	TRIG active edge is falling (PORb default).
1	TRIG active edge is rising.

Output Pin Configuration (0x11)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	INT2_OCFG[1:0]		INT1_OCFG[1:0]		–
Reset	–	–	–	0x0		0x0		–
Access Type	–	–	–	Write, Read		Write, Read		–

INT2_OCFG

See INT1_OCFG[1:0] for details.

INT1_OCFG

INTx_OCFG[1:0] (x = 1, 2) selects the output drive type for the INTx pin, as shown in the table below.

VALUE	DECODE
0	Open drain, V_{DD} compliant, active-low output (PORb default).
1	Active drive to VDD_DIG and GND, the active level is high-output.
2	Active drive to VDD_DIG and GND, the active level is low-output.
3	Not defined

FR Clock Frequency Select (0x15)

BIT	7	6	5	4	3	2	1	0
Field	–	–	FR_CLK_SEL	FR_CLK_FINE_TUNE[4:0]				
Reset	–	–	0b1	0x0				
Access Type	–	–	Write, Read	Write, Read				

FR_CLK_SEL

When FR_CLK_SEL is set to 0, the internal frame-rate primary clock is trimmed to 32.0kHz. When FR_CLK_SEL is set to 1, the internal frame rate primary clock is trimmed to 32.768kHz. The measurement frame rate is the primary clock rate divided by the program divider ratio (FR_CLK_DIV).

FR_CLK_SEL	ENUMERATION	DECODE
0	CLK32000Hz	The internal frame-rate primary clock is 32000Hz.
1	CLK32768Hz	The internal frame-rate primary clock is 32768Hz.

FR_CLK_FINE_TUNE

FR_CLK_FINE_TUNE4:0] is used to fine-tune the internal 32kHz/32.768kHz frame rate clock. This register can be used to compensate the internal oscillator for thermal drift. This can be accomplished by measuring the time between interrupts using a microcontroller crystal based real-time oscillator as a reference and computing the error in the time between interrupts. FR_CLK_FINE_TUNE[4:0] is a 2s complement code with a resolution of 0.2%/LSB. The total range is +3.0% to -3.2% around the factory trimmed value. See the FR_CLK_FINE_TUNE table for the shift in internal primary frame-rate clock vs. trim code.

FR_CLK_FINE_TUNE[4:0]	SHIFT IN OSC FREQUENCY (%)
0x10	-3.2
0x11	-3.0
0x12	-2.8
0x13	-2.6
0x14	-2.4
0x15	-2.2
0x16	-2.0
0x17	-1.8
0x18	-1.6
0x19	-1.4
0x1A	-1.2
0x1B	-1.0
0x1C	-0.8

0x1D	-0.6
0x1E	-0.4
0x1F	-0.2
0x00	0.0
0x01	0.2
0x02	0.4
0x03	0.6
0x04	0.8
0x05	1.0
0x06	1.2
0x07	1.4
0x08	1.6
0x09	1.8
0x0A	2.0
0x0B	2.2
0x0C	2.4
0x0D	2.6
0x0E	2.8
0x0F	3.0

FR Clock Divider MSB (0x16)

BIT	7	6	5	4	3	2	1	0
Field	–	FR_CLK_DIV_H[6:0]						
Reset	–	0x01						
Access Type	–	Write, Read						

FR_CLK_DIV_H

FR_CLK_DIV_H[6:0] is the upper 7 bits of the 15-bit FR_CLK_DIV[14:0] clock divider, which defines the frame rate at which every enabled measurement is made.

The FR_CLK_DIV[14:0] should be programmed such that all the conversions selected in the MEASn_EN (n = 1 to 9) bits in the System Configuration 1 and 2 registers can be completed within the frame period. In the event that the number of enabled measurements as well as the integration time and number of averages of each enabled measurement results in a frame measurement time that is longer than the primary frame clock period divided by FR_CLK_DIV, a timing error occurs. This timing error sets the INVALID_CFG bit in the Status register 2.

The time for each measurement to complete is given by:

$t_{MEASUREMENT} = t_{INIT1} + t_{MEAS1} + t_{MEAS2} + t_{MEAS3} + ... + t_{MEAS9}$

where:

if the MEASn_SINC3 = 1 or MEASn_FILT = 0, then:

$t_{MEASn} = [t_{INIT} + MEASn_TINT \times (2 \times MEASn_AVER+1) + 2 \times MEASn_AVER \times MEASn_PD_SETLNG] \times MEASn_EN$

if MEASn_SINC3 = 0 and MEASn_FILT = 1 then:

$t_{MEASn} = [t_{INIT} + 2 \times MEASn_TINT + MEASn_PD_SETLNG] \times MEASn_EN$

$t_{INIT1} = 7 \times t_{CLOCK}$

$t_{INIT} = 3 \times t_{CLOCK}$

MEASn_TINT = Integration time defined in measurement n = 1 to 9

MEASn_EN = 1 if the measurement is enabled and 0 if it is not for measurement n = 1 to 9

MEASn_AVER = Number of averages defined in measurement n = 1 to 9

MEASn_PD_SETLNG = Photodiode settling time defined in measurement n = 1 to 9

t_{CLOCK} = Frame clock period, which can be 1/32768 sec or 1/32000 sec depending on the FR_CLK_SEL bit

In SYNC_MODE = 0 and 2 a valid measurement requires:

$t_{MEASUREMENT} < FR_CLK_DIV/F_{Primary_Frame_Clock}$

where:

$F_{Primary_Frame_Clock}$ = Either the internal primary frame clock (SYNC_MODE = 0) or the external frame clock inputed through the TRIG input (SYNC_MODE = 2)

In SYNC_MODE = 1 a valid measurement requires:

$t_{MEASUREMENT} < t_{TRIG_PERIOD}$

where:

t_{TRIG_PERIOD} = Period of the TRIG input signal

FR Clock Divider LSB (0x17)

BIT	7	6	5	4	3	2	1	0
Field	FR_CLK_DIV_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

FR_CLK_DIV_L

FR_CLK_DIV_L[7:0] is the lower byte of the 15-bit FR_CLK_DIV[14:0] clock divider that defines the frame rate.

See FR_CLK_DIV_H for more details.

MEAS1 Selects (0x18)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS1_AMB	MEAS1_DRVC[1:0]		MEAS1_DRVB[1:0]		MEAS1_DRVA[1:0]	
Reset	–	0b0	0x1		0x0		0x0	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS1_AMB

Set MEASn_AMB (n = 1 to 9) to 1 to enable a direct ambient measurement. Set MEASn_AMB to 0 to allow normal exposure measurements to be made. When MEASn_AMB is set to 1, MEASn_DRVA[1:0], MEASn_DRVB[1:0], and MEASn_DRVC[1:0] are ignored.

When a MEASn_AMB is set to 1, it should always be the last enabled measurement in the frame.

MEASn_AMB (n = 1 to 9)	DECODE
0	Enable normal exposure measurements for MEASn.
1	Enable direct ambient conversion for MEASn.

MEAS1_DRVC

Program MEASn_DRVC (n = 1 to 9) measurement to select the LEDx_DRV pin (x = 1, 3, 6, 9) for LED Driver C as shown in the table below.

MEASn_DRVC[1:0] (n = 1 to 9)	DECODE
0	LED Driver C drives pin 1
1	LED Driver C drives pin 3
2	LED Driver C drives pin 6
3	LED Driver C drives pin 9

MEAS1_DRVB

Program MEASn_DRVB (n = 1 to 9) measurement to select the LEDx_DRV pin (x = 2, 3, 5, 8) for LED Driver B as shown in the table below.

MEASn_DRVB[1:0] (n = 1 to 9)	DECODE
0	LED Driver B drives pin 2
1	LED Driver B drives pin 3
2	LED Driver B drives pin 5
3	LED Driver B drives pin 8

MEAS1_DRVA

Program MEASn_DRVA (n = 1 to 9) measurement to select the LEDx_DRV pin (x = 1, 2, 4, 7) for LED Driver A as shown in the table below.

MEASn_DRVA[1:0] (n = 1 to 9)	DECODE
0	LED Driver A drives pin 1
1	LED Driver A drives pin 2
2	LED Driver A drives pin 4
3	LED Driver A drives pin 7

MEAS1 Configuration 1 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS1_PPG2_PDSEL	MEAS1_PPG1_PDSEL	MEAS1_TINT[1:0]		MEAS1_AVER[2:0]		
Reset	–	0b0	0b0	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS1_PPG2_PDSEL

MEASn_PPG2_PDSEL (n = 1 to 9) selects which PDx_IN (x = 2, 4) is connected to optical channel 2 for measurement n. Set MEASn_PPG2_PDSEL to 0 to select PD2_IN and 1 to select PD4_IN as input to optical channel 2 as shown below.

MEASn_PPG2_PDSEL (n = 1 to 9)	DECODE
0	Select PD2_IN as input to optical channel 2 for measurement n.
1	Select PD4_IN as input to optical channel 2 for measurement n.

MEAS1_PPG1_PDSEL

MEASn_PPG1_PDSEL (n = 1 to 9) selects which PDx_IN (x = 1, 3) is connected to optical channel 1 for measurement n. Set MEASn_PPG1_PDSEL to 0 to select PD1_IN and 1 to select PD3_IN as input to optical channel 1 as shown below.

MEASn_PPG1_PDSEL (n = 1 to 9)	DECODE
0	Select PD1_IN as input to PPG1 for measurement n.
1	Select PD3_IN as input to PPG1 for measurement n.

MEAS1_TINT

MEASn_TINT[1:0] (n = 1 to 9) bits set the integration time of PPG ADC as shown in the table below.

MEASn_TINT[1:0] (n = 1 to 9)	INTEGRATION TIME (µs)
00	14.6
01	29.2
10	58.6
11	117.1

MEAS1_AVER

MEASn_AVER[2:0] (n = 1 to 9) sets the number of exposures that are averaged in order to improve the exposure SNR and improve ambient light cancelation. MEASn_AVER works only with MEASn_FILT_SEL = 0 or when COLLECT_RAW_DATA = 1. When MEASn_FILT_SEL = 0, $(2 \times 2^{MEASn_AVER} + 1)$ ADC conversions of interleaved dark and exposure measurements are made and a weighted computed average loaded into the FIFO.

MEASn_AVER[2:0] (n = 1 to 9)	NUMBER OF LED PULSES
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

MEAS1 Configuration 2 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_SINC3_SEL	MEAS1_FILT_SEL	MEAS1_LED_RGE[1:0]		MEAS1_PPG2_ADC_RGE[1:0]		MEAS1_PPG1_ADC_RGE[1:0]	
Reset	0b0	0b0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS1_SINC3_SEL

MEASx_SINC3_SEL (x = 1 to 9) enables the SINC3 decimation filter for the delta-sigma ADC for measurement x. This filter provides improved high-frequency roll-off, which also improves high-frequency ambient light rejection and V_{LED} power-supply rejection. MAX86171 by default, uses a third order cascade of integrators (COI3) decimation filter. This

filter provides excellent quantization, but only a 20dB/dec roll-off at higher frequencies. The SINC3 filter is only available on the longest integration time, MEASx_TINT = 0x3 (117.1µs). However, the SINC3 filter provides a 60dB/dec roll-off at out of band frequencies; thus, providing improved ambient and V_{LED} rejection.

Set MEASx_SINC3 low to use the COI3 decimation filter.

Set MEASx_SINC3 high to select the SINC3 decimation filter, which is only used if the MEASx_TINT = 0x3 (integration time set to 117.1µs) for this measurement.

VALUE	DECODE
0x0	SINC3 filter is not used.
0x1	SINC3 decimation filter is used only if MEASx_TINT = 0x3 (115.2µs)

MEAS1_FILT_SEL

MEASn_FILT_SEL (n = 1 to 9) sets the backend ambient light rejection method to be used. Set MEASn_FILT_SEL to 0 to use the central difference method where ambient light estimation is made from dark measurements before and after the exposure measurement. Set MEASn_FILT_SEL to 1 to use the forward difference method where the ambient light is estimated by a dark measurement before the exposure measurement.

When MEASn_FILT_SEL is set to 0, (2 x 2^{MEASn_AVER} + 1) ADC conversions of interleaved dark and exposure measurements are made and a weighted computed average loaded into the FIFO. When MEASn_FILT_SEL is set to 1, only one dark and exposure ADC conversion is made, regardless of the value of MEASn_AVER.

VALUE	DECODE
0	Ambient light correction is done using the central difference method.
1	Ambient light correction is done using the forward difference method.

MEAS1_LED_RGE

MEASn_LED_RGE (n = 1 to 9) sets the range of all three LED current drivers DRVA, DRVB, DRVC for the nth measurement.

MEASn_LED_RGE[1:0]	LED FULL-SCALE RANGE (mA)
00	32
01	64
10	96
11	128

MEAS1_PPG2_ADC_RGE

MEASn_PPGx_ADC_RGE[1:0] (n = 1 to 9, x = 1, 2) bits set the ADC positive full-scale range of the optical channel x in measurement n, as shown in the table below.

MEASn_PPGX_ADC_RGE[1:0] (N = 1 TO 9, X = 1, 2)	LSB (pA)	FULL SCALE (µA)
00	7.6	4.0
01	15.3	8.0
10	30.5	16.0
11	61.0	32.0

MEAS1_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS1 Configuration 3 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PD_SETLNG[1:0]		MEAS1_LED_SETLNG[1:0]		MEAS1_PPG2_DACOFF[1:0]		MEAS1_PPG1_DACOFF[1:0]	
Reset	0x1		0x1		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS1_PD_SETLNG

MEASn_PD_SETLNG[1:0] sets the time between dark and exposure samples as shown in the table below. This time can be used to allow for longer photodiode settling.

MEASn_PD_SETLNG[1:0] (n = 1 to 9)	TIME BETWEEN SAMPLES (µs)
0	6.1
1	12.1 (Default)
2	18.1
3	24.1

MEAS1_LED_SETLNG

Program MEASn_LED_SETLNG[1:0] to select the delay from the rising edge of LED to start of the exposure ADC integration. This allows for the LED current to settle before the start of ADC integration. LED settling time must always be less than the PD settling time for the same measurement.

MEASn_LED_SETLNG[1:0] (n = 1 to 9)	SETTLING TIME (µs)
00	6.0
01	12.0 (default)
10	18.0
11	24.0

MEAS1_PPG2_DACOFF

MEASn_PPGx_DACOFF[1:0] sets the value of the offset DAC during the exposure interval. This allow for a larger convertible exposure range by sourcing some of the exposure current from the offset DAC. Set MEASn_PPGx_DACOFF[1:0] to select the desired offset current as shown in the table below.

MEASN_PPGX_DACOFF[1:0] (N = 1 TO 9, X = 1, 2)	INJECTED OFFSET CURRENT (µA)
0	Offset DAC current is 0
1	Offset DAC current is 8
2	Offset DAC current is 16
3	Offset DAC current is 24

MEAS1_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS1 DRVA Current (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS1_DRVA_PA

MEASn_DRVx_PA[7:0] (n = 1 to 9, x = A, B, C) sets the LED drive current on each of the three LED drivers DRVA, DRVB, and DRVC for the measurement. Each of the three LED drivers is routed to the LEDy_DRV (y = 1 to 9) as set by the MEASn_DRVA, MEASn_DRVB, and MEASn_DRVC multiplexer setting. The full-scale range of all three LED drivers is set by the MEASn_LED_RGE[1:0] bits.

Set MEASn_DRVx_PA[7:0] (n = 1 to 9, x = A, B, C) code to set the desired current according to the table below. If MEASn_DRVx_PA[7:0] is set to 0x00, LED Driver x is disabled for measurement n.

MEASn_LED_RGE[1:0] (n = 1 to 9)	00	01	10	11
MEASn_DRVx_PA[7:0] (n = 1 to 9, x = A, B, C)	LED CURRENT (mA)	LED CURRENT (mA)	LED CURRENT (mA)	LED CURRENT (mA)
0	0.000	0.000	0.000	0.000
1	0.125	0.250	0.375	0.500
10	0.250	0.500	0.750	1.000
11	0.375	0.750	1.125	1.500
.....				
11111100	31.500	63.000	94.500	126.000
11111101	31.625	63.250	94.875	126.500
11111110	31.750	63.500	95.250	127.000
11111111	31.875	63.750	95.625	127.500
LSB	0.125	0.250	0.375	0.500

MEAS1 DRVB Current (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS1_DRVB_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS1 DRVC Current (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_DRVC_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS1_DRVC_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS2 Selects (0x20)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS2_AMB	MEAS2_DRVC[1:0]		MEAS2_DRVB[1:0]		MEAS2_DRVA[1:0]	
Reset	–	0b0	0x0		0x0		0x0	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS2_AMB

See MEAS1_AMB for details.

MEAS2_DRVC

See MEAS1_DRVC[1:0] for details.

MEAS2_DRVB

See MEAS1_DRVB[1:0] for details.

MEAS2_DRVA

See MEAS1_DRVA[1:0] for details.

MEAS2 Configuration 1 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS2_PPG2_PDSEL	MEAS2_PPG1_PDSEL	MEAS2_TINT[1:0]		MEAS2_AVER[2:0]		
Reset	–	0b0	0b0	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS2_PPG2_PDSEL

See MEAS1_PPG2_PDSEL for details.

MEAS2_PPG1_PDSEL

See MEAS1_PPG1_PDSEL for details.

MEAS2_TINT

See MEAS1_TINT for details.

MEAS2_AVER

See MEAS1_AVER[2:0] for details.

MEAS2 Configuration 2 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_SINC3_SEL	MEAS2_FILT_SEL	MEAS2_LED_RGE[1:0]		MEAS2_PPG2_ADC_RGE[1:0]		MEAS2_PPG1_ADC_RGE[1:0]	
Reset	0b0	0b0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS2_SINC3_SEL

See MEAS1_SINC3_SEL for details.

MEAS2_FILT_SEL

See MEAS1_FILT_SEL for details.

MEAS2_LED_RGE

See MEAS1_LED_RGE[1:0] for details.

MEAS2_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS2_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS2 Configuration 3 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PD_SETLNG[1:0]		MEAS2_LED_SETLNG[1:0]		MEAS2_PPG1_DACOFF[1:0]		MEAS2_PPG1_DACOFF[1:0]	
Reset	0x1		0x1		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS2_PD_SETLNG

See MEAS1_PD_SETLNG[1:0] for details.

MEAS2_LED_SETLNG

See MEAS1_LED_SETLNG[1:0] for details.

MEAS2_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS2_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS2 DRVA Current (0x24)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS2_DRVA_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS2 DRVB Current (0x25)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS2_DRVB_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS2 DRVC Current (0x26)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_DRVC_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS2_DRVC_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS3 Selects (0x28)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS3_AMB	MEAS3_DRVC[1:0]		MEAS3_DRVB[1:0]		MEAS3_DRVA[1:0]	
Reset	–	0b0	0x1		0x0		0x0	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS3_AMB

See MEAS1_AMB for details.

MEAS3_DRVC

See MEAS1_DRVC[1:0] for details.

MEAS3_DRVB

See MEAS1_DRVB[1:0] for details.

MEAS3_DRVA

See MEAS1_DRVA[1:0] for details.

MEAS3 Configuration 1 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS3_PPG2_PDSEL	MEAS3_PPG1_PDSEL	MEAS3_TINT[1:0]		MEAS3_AVER[2:0]		
Reset	–	0b0	0b0	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS3_PPG2_PDSEL

See MEAS1_PPG2_PDSEL for details.

MEAS3_PPG1_PDSEL

See MEAS1_PPG1_PDSEL for details.

MEAS3_TINT

See MEAS1_TINT for details.

MEAS3_AVER

See MEAS1_AVER[2:0] for details.

MEAS3 Configuration 2 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_SINC3_SEL	MEAS3_FILT_SEL	MEAS3_LED_RGE[1:0]		MEAS3_PPG2_ADC_RGE[1:0]		MEAS3_PPG1_ADC_RGE[1:0]	
Reset	0b0	0b0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS3_SINC3_SEL

See MEAS1_SINC3_SEL for details.

MEAS3_FILT_SEL

See MEAS1_FILT_SEL for details.

MEAS3_LED_RGE

See MEAS1_LED_RGE[1:0] for details.

MEAS3_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS3_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS3 Configuration 3 (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PD_SETLNG[1:0]		MEAS3_LED_SETLNG[1:0]		MEAS3_PPG2_DACOFF[1:0]		MEAS3_PPG1_DACOFF[1:0]	
Reset	0x1		0x1		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS3_PD_SETLNG

See MEAS1_PD_SETLNG[1:0] for details.

MEAS3_LED_SETLNG

See MEAS1_LED_SETLNG[1:0] for details.

MEAS3_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS3_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS3 DRVA Current (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS3_DRVA_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS3 DRVB Current (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS3_DRVB_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS3 DRVC Current (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_DRVC_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS3_DRVC_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS4 Selects (0x30)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS4_AMB	MEAS4_DRVC[1:0]		MEAS4_DRVB[1:0]		MEAS4_DRVA[1:0]	
Reset	–	0b0	0x1		0x0		0x0	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS4_AMB

See MEAS1_AMB for details.

MEAS4_DRVC

See MEAS1_DRVC[1:0] for details.

MEAS4_DRVB

See MEAS1_DRVB[1:0] for details.

MEAS4_DRVA

See MEAS1_DRVA[1:0] for details.

MEAS4 Configuration 1 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS4_PPG2_PDSEL	MEAS4_PPG1_PDSEL	MEAS4_TINT[1:0]		MEAS4_AVER[2:0]		
Reset	–	0b0	0b0	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS4_PPG2_PDSEL

See MEAS1_PPG2_PDSEL for details.

MEAS4_PPG1_PDSEL

See MEAS1_PPG1_PDSEL for details.

MEAS4_TINT

See MEAS1_TINT for details.

MEAS4_AVER

See MEAS1_AVER[2:0] for details.

MEAS4 Configuration 2 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_SINC3_SEL	MEAS4_FILT_SEL	MEAS4_LED_RGE[1:0]		MEAS4_PPG2_ADC_RGE[1:0]		MEAS4_PPG1_ADC_RGE[1:0]	
Reset	0b0	0b0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS4_SINC3_SEL

See MEAS1_SINC3_SEL for details.

MEAS4_FILT_SEL

See MEAS1_FILT_SEL for details.

MEAS4_LED_RGE

See MEAS1_LED_RGE[1:0] for details.

MEAS4_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS4_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS4 Configuration 3 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PD_SETLNG[1:0]		MEAS4_LED_SETLNG[1:0]		MEAS4_PPG2_DACOFF[1:0]		MEAS4_PPG1_DACOFF[1:0]	
Reset	0x1		0x1		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS4_PD_SETLNG

See MEAS1_PD_SETLNG[1:0] for details.

MEAS4_LED_SETLNG

See MEAS1_LED_SETLNG[1:0] for details.

MEAS4_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS4_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS4 DRVA Current (0x34)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS4_DRVA_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS4 DRVB Current (0x35)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS4_DRVB_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS4 DRVC Current (0x36)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_DRVC_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS4_DRVC_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS5 Selects (0x38)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS5_AMB	MEAS5_DRVC[1:0]		MEAS5_DRVB[1:0]		MEAS5_DRVA[1:0]	
Reset	–	0b0	0x1		0x0		0x0	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS5_AMB

See MEAS1_AMB for details.

MEAS5_DRVC

See MEAS1_DRVC[1:0] for details.

MEAS5_DRVB

See MEAS1_DRVB[1:0] for details.

MEAS5_DRVA

See MEAS1_DRVA[1:0] for details.

MEAS5 Configuration 1 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS5_PPG2_PDSEL	MEAS5_PPPG1_PDSEL	MEAS5_TINT[1:0]		MEAS5_AVER[2:0]		
Reset	–	0b0	0b0	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS5_PPG2_PDSEL

See MEAS1_PPG2_PDSEL for details.

MEAS5_PPPG1_PDSEL

See MEAS1_PPG1_PDSEL for details.

MEAS5_TINT

See MEAS1_TINT for details.

MEAS5_AVER

See MEAS1_AVER[2:0] for details.

MEAS5 Configuration 2 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_SINC3_SEL	MEAS5_FILT_SEL	MEAS5_LED_RGE[1:0]		MEAS5_PPG2_ADC_RGE[1:0]		MEAS5_PPG1_ADC_RGE[1:0]	
Reset	0b0	0b0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS5_SINC3_SEL

See MEAS1_SINC3_SEL for details.

MEAS5_FILT_SEL

See MEAS1_FILT_SEL for details.

MEAS5_LED_RGE

See MEAS1_LED_RGE[1:0] for details.

MEAS5_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS5_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS5 Configuration 3 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PD_SETLNG[1:0]		MEAS5_LED_SETLNG[1:0]		MEAS5_PPG2_DACOFF[1:0]		MEAS5_PPG1_DACOFF[1:0]	
Reset	0x1		0x1		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS5_PD_SETLNG

See MEAS1_PD_SETLNG[1:0] for details.

MEAS5_LED_SETLNG

See MEAS1_LED_SETLNG[1:0] for details.

MEAS5_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS5_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS5 DRVA Current (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS5_DRVA_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS5 DRVB Current (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS5_DRVB_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS5 DRVC Current (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_DRVC_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS5_DRVC_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS6 Selects (0x40)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS6_AMB	MEAS6_DRVC[1:0]		MEAS6_DRVB[1:0]		MEAS6_DRVA[1:0]	
Reset	–	0b0	0x1		0x0		0x0	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS6_AMB

See MEAS1_AMB for details.

MEAS6_DRVC

See MEAS1_DRVC[1:0] for details.

MEAS6_DRVB

See MEAS1_DRVB[1:0] for details.

MEAS6_DRVA

See MEAS1_DRVA[1:0] for details.

MEAS6 Configuration 1 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS6_PPG2_PDSEL	MEAS6_PPG1_PDSEL	MEAS6_TINT[1:0]		MEAS6_AVER[2:0]		
Reset	–	0b0	0b0	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS6_PPG2_PDSEL

See MEAS1_PPG2_PDSEL for details.

MEAS6_PPG1_PDSEL

See MEAS1_PPG1_PDSEL for details.

MEAS6_TINT

See MEAS1_TINT for details.

MEAS6_AVER

See MEAS1_AVER[2:0] for details.

MEAS6 Configuration 2 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_SINC3_SEL	MEAS6_FILT_SEL	MEAS6_LED_RGE[1:0]		MEAS6_PPG2_ADC_RGE[1:0]		MEAS6_PPG1_ADC_RGE[1:0]	
Reset	0b0	0b0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS6_SINC3_SEL

See MEAS1_SINC3_SEL for details.

MEAS6_FILT_SEL

See MEAS1_FILT_SEL for details.

MEAS6_LED_RGE

See MEAS1_LED_RGE[1:0] for details.

MEAS6_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS6_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS6 Configuration 3 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PD_SETLNG[1:0]		MEAS6_LED_SETLNG[1:0]		MEAS6_PPG2_DACOFF[1:0]		MEAS6_PPG1_DACOFF[1:0]	
Reset	0x1		0x1		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS6_PD_SETLNG

See MEAS1_PD_SETLNG[1:0] for details.

MEAS6_LED_SETLNG

See MEAS1_LED_SETLNG[1:0] for details.

MEAS6_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS6_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS6 DRVA Current (0x44)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS6_DRVA_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS6 DRVB Current (0x45)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS6_DRVB_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS6 DRVC Current (0x46)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_DRVC_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS6_DRVC_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS7 Selects (0x48)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS7_AMB	MEAS7_DRVC[1:0]		MEAS7_DRVB[1:0]		MEAS7_DRVA[1:0]	
Reset	–	0b0	0x1		0x0		0x0	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS7_AMB

See MEAS1_AMB for details.

MEAS7_DRVC

See MEAS1_DRVC[1:0] for details.

MEAS7_DRVB

See MEAS1_DRVB[1:0] for details.

MEAS7_DRVA

See MEAS1_DRVA[1:0] for details.

MEAS7 Configuration 1 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS7_PPG2_PDSEL	MEAS7_PPG1_PDSEL	MEAS7_TINT[1:0]		MEAS7_AVER[2:0]		
Reset	–	0b0	0b0	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS7_PPG2_PDSEL

See MEAS1_PPG2_PDSEL for details.

MEAS7_PPG1_PDSEL

See MEAS1_PPG1_PDSEL for details.

MEAS7_TINT

See MEAS1_TINT for details.

MEAS7_AVER

See MEAS1_AVER[2:0] for details.

MEAS7 Configuration 2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_SINC3_SEL	MEAS7_FILT_SEL	MEAS7_LED_RGE[1:0]		MEAS7_PPG2_ADC_RGE[1:0]		MEAS7_PPG1_ADC_RGE[1:0]	
Reset	0b0	0b0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS7_SINC3_SEL

See MEAS1_SINC3_SEL for details.

MEAS7_FILT_SEL

See MEAS1_FILT_SEL for details.

MEAS7_LED_RGE

See MEAS1_LED_RGE[1:0] for details.

MEAS7_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS7_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS7 Configuration 3 (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_PD_SETLNG[1:0]		MEAS7_LED_SETLNG[1:0]		MEAS7_PPG2_DACOFF[1:0]		MEAS7_PPG1_DACOFF[1:0]	
Reset	0x1		0x1		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS7_PD_SETLNG

See MEAS1_PD_SETLNG[1:0] for details.

MEAS7_LED_SETLNG

See MEAS1_LED_SETLNG[1:0] for details.

MEAS7_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS7_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS7 DRVA Current (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS7_DRVA_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS7 DRVB Current (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS7_DRVB_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS7 DRVC Current (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_DRVC_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS7_DRVC_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS8 Selects (0x50)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS8_AMB	MEAS8_DRVC[1:0]		MEAS8_DRVB[1:0]		MEAS8_DRVA[1:0]	
Reset	–	0b0	0x1		0x0		0x0	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS8_AMB

See MEAS1_AMB for details.

MEAS8_DRVC

See MEAS1_DRVC[1:0] for details.

MEAS8_DRVB

See MEAS1_DRVB[1:0] for details.

MEAS8_DRVA

See MEAS1_DRVA[1:0] for details.

MEAS8 Configuration 1 (0x51)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS8_PPG2_PDSEL	MEAS8_PPG1_PDSEL	MEAS8_TINT[1:0]		MEAS8_AVER[2:0]		
Reset	–	0b0	0b0	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS8_PPG2_PDSEL

See MEAS1_PPG2_PDSEL for details.

MEAS8_PPG1_PDSEL

See MEAS1_PPG1_PDSEL for details.

MEAS8_TINT

See MEAS1_TINT for details.

MEAS8_AVER

See MEAS1_AVER[2:0] for details.

MEAS8 Configuration 2 (0x52)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_SINC3_SEL	MEAS8_FILT_SEL	MEAS8_LED_RGE[1:0]		MEAS8_PPG2_ADC_RGE[1:0]		MEAS8_PPG1_ADC_RGE[1:0]	
Reset	0b0	0b0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS8_SINC3_SEL

See MEAS1_SINC3_SEL for details.

MEAS8_FILT_SEL

See MEAS1_FILT_SEL for details.

MEAS8_LED_RGE

See MEAS1_LED_RGE[1:0] for details.

MEAS8_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS8_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS8 Configuration 3 (0x53)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_PD_SETLNG[1:0]		MEAS8_LED_SETLNG[1:0]		MEAS8_PPG2_DACOFF[1:0]		MEAS8_PPG1_DACOFF[1:0]	
Reset	0x1		0x1		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS8_PD_SETLNG

See MEAS1_PD_SETLNG[1:0] for details.

MEAS8_LED_SETLNG

See MEAS1_LED_SETLNG[1:0] for details.

MEAS8_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS8_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS8 DRVA Current (0x54)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS8_DRVA_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS8 DRVB Current (0x55)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS8_DRVB_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS8 DRVC Current (0x56)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_DRVC_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS8_DRVC_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS9 Selects (0x58)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS9_AMB	MEAS9_DRVC[1:0]		MEAS9_DRVB[1:0]		MEAS9_DRVA[1:0]	
Reset	–	0b0	0x1		0x0		0x0	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS9_AMB

See MEAS1_AMB for details.

MEAS9_DRVC

See MEAS1_DRVC[1:0] for details.

MEAS9_DRVB

See MEAS1_DRVB[1:0] for details.

MEAS9_DRVA

See MEAS1_DRVA[1:0] for details.

MEAS9 Configuration 1 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS9_PPG2_PDSEL	MEAS9_PPG1_PDSEL	MEAS9_TINT[1:0]		MEAS9_AVER[2:0]		
Reset	–	0b0	0b0	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS9_PPG2_PDSEL

See MEAS1_PPG2_PDSEL for details.

MEAS9_PPG1_PDSEL

See MEAS1_PPG1_PDSEL for details.

MEAS9_TINT

See MEAS1_TINT for details.

MEAS9_AVER

See MEAS1_AVER[2:0] for details.

MEAS9 Configuration 2 (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_SINC3_SEL	MEAS9_FILT_SEL	MEAS9_LED_RGE[1:0]		MEAS9_PPG2_ADC_RGE[1:0]		MEAS9_PPG1_ADC_RGE[1:0]	
Reset	0b0	0b0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS9_SINC3_SEL

See MEAS1_SINC3_SEL for details.

MEAS9_FILT_SEL

See MEAS1_FILT_SEL for details.

MEAS9_LED_RGE

See MEAS1_LED_RGE[1:0] for details.

MEAS9_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[1:0] for details.

MEAS9_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_REG[1:0] for details.

MEAS9 Configuration 3 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_PD_SETLNG[1:0]		MEAS9_LED_SETLNG[1:0]		MEAS9_PPG2_DACOFF[1:0]		MEAS9_PPG1_DACOFF[1:0]	
Reset	0x1		0x1		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS9_PD_SETLNG

See MEAS1_PD_SETLNG[1:0] for details.

MEAS9_LED_SETLNG

See MEAS1_LED_SETLNG[1:0] for details.

MEAS9_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[1:0] for details.

MEAS9_PPG1_DACOFF

See MEAS1_PPG1_DACOFF[1:0] for details.

MEAS9 DRVA Current (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS9_DRVA_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS9 DRVB Current (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS9_DRVB_PA

See MEAS1_DRVA_PA[7:0] for details.

MEAS9 DRVC Current (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_DRVC_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS9_DRVC_PA

See MEAS1_DRVA_PA[7:0] for details.

THRESHOLD MEAS SEL (0x68)

BIT	7	6	5	4	3	2	1	0
Field	THRESH2_MEAS_SEL[3:0]				THRESH1_MEAS_SEL[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

THRESH2_MEAS_SEL

This field enables THRESH2 and assigns one of the nine measurements to the second instance of the threshold feature. THRESH2_MEAS_SEL[3:0] selects which of the MEASn (n = 1 to 9) is used for THRESH2_HILO detect.

THRESH2_MEAS_SEL[3:0]	DECODE
0x0	THRESH2_HILO detect is disabled
0x1	MEAS1 selected
0x2	MEAS2 selected
0x3	MEAS3 selected
0x4	MEAS4 selected
0x5	MEAS5 selected
0x6	MEAS6 selected
0x7	MEAS7 selected
0x8	MEAS8 selected
0x9	MEAS9 selected
0xA to 0xF	RESERVED, THRESH2_HILO detect is disabled

THRESH1_MEAS_SEL

This field enables THRESH1 and assigns one of the nine measurements to the first instance of the threshold feature. THRESH1_MEAS_SEL[3:0] selects which of the MEASn (n = 1 to 9) is used for THRESH1_HILO detect.

THRESH1_MEAS_SEL[3:0]	DECODE
0x0	THRESH1_HILO detect is disabled
0x1	MEAS1 selected
0x2	MEAS2 selected
0x3	MEAS3 selected
0x4	MEAS4 selected
0x5	MEAS5 selected
0x6	MEAS6 selected

0x7	MEAS7 selected
0x8	MEAS8 selected
0x9	MEAS9 selected
0xA to 0xF	RESERVED, THRESH1_HILO detect is disabled

THRESHOLD HYST (0x69)

BIT	7	6	5	4	3	2	1	0
Field	THRESH2_ PPG_SEL	THRESH1_ PPG_SEL	–	TIME_HYST[1:0]		LEVEL_HYST[2:0]		
Reset	0b0	0b0	–	0x0		0x0		
Access Type	Write, Read	Write, Read	–	Write, Read		Write, Read		

THRESH2_PPG_SEL

THRESH2_PPG_SEL sets which optical channel the threshold measurement 2 is applied. If THRESH2_PPG_SEL is set to 0 then the threshold measurement 2 is applied to optical channel 1. If THRESH2_PPG_SEL is set to 1 then threshold measurement 2 is applied to optical channel 2.

THRESH2_PPG_SEL	CHANNEL THAT THRESHOLD2 IS APPLIED
0b0	Optical Channel 1
0b1	Optical Channel 2

THRESH1_PPG_SEL

THRESH1_PPG_SEL sets which optical channel the threshold measurement 1 is applied. If THRESH1_PPG_SEL is set to 0 then the threshold measurement 1 is applied to optical channel 1. If THRESH1_PPG_SEL is set to 1 then threshold measurement 1 is applied to optical channel 2.

THRESH2_PPG_SEL	CHANNEL THAT THRESHOLD2 IS APPLIED
0b0	Optical Channel 1
0b1	Optical Channel 2

TIME_HYST

Time hysteresis sets the number of samples that the ambient light corrected exposure signal exceeds the THRESHOLDx_UPPER or below THRESHOLDx_LOWER before the threshold interrupt is set. The value of the ADC counts is applied at ±0.5 x LEVEL_HYST around the THRESHOLDx_UPPER and THRESHOLDx_LOWER. Specifically, in order for an interrupt to be generated from the thresholding function, an ambient light corrected exposure must transition above the THRESHOLDx_UPPER + 0.5 x LEVEL_HYST and stay above THRESHOLDx_UPPER - 0.5 x LEVEL_HYST for TIME_HYST samples or transition below THRESHOLDx_LOWER - 0.5 x LEVEL_HYST and stay below THRESHOLDx_LOWR + 0.5 x LEVEL_HYST for TIME_HYST samples. TIME_HYST parameter applies to both instances of threshold interrupts.

TIME_HYST	NUMBER OF SAMPLES BEFORE INTERRUPT IS SET
0b00	0, time hysteresis disabled
0b01	2 samples
0b10	4 samples
0b11	8 samples

LEVEL_HYST

Level hysteresis sets the amount of ambient light corrected exposure hysteresis to apply to both instances of the threshold function. This value is in ADC counts and is applied at ±0.5 x LEVEL_HYST around the THRESHOLDx_UPPER and THRESHOLDx_LOWER. Specifically, in order for an interrupt to be generated from the thresholding function, an ambient light corrected exposure must transition above the THRESHOLDx_UPPER + 0.5 x LEVEL_HYST and stay above THRESHOLDx_UPPER - 0.5 x LEVEL_HYST for TIME_HYST samples or transition below THRESHOLDx_LOWER - 0.5 x LEVEL_HYST and stay below THRESHOLDx_LOWER + 0.5 x LEVEL_HYST for TIME_HYST samples. LEVEL_HYST parameter applies to both instances of threshold interrupts.

LEVEL_HYST	MAGNITUDE OF HYSTERESIS (LSBs)
0b000	0, Disable Level Hysteresis
0b001	2
0b010	4
0b011	8
0b100	16
0b101	32
0b110	64
0b111	128

PPG HI THRESHOLD1 (0x6A)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD1_UPPER[7:0]							
Reset	0xFF							
Access Type	Write, Read							

THRESHOLD1_UPPER

Upper threshold for instance 1. Each LSB of the threshold represents 2048 LSBs the ambient light exposure code.

It is important to program the THRESHOLD1_UPPER to be greater than the THRESHOLD1_LOWER. Otherwise, the interrupt behavior is undefined.

THRESHOLD1_UPPER	AMBIENT LIGHT CORRECTED EXPOSURE SIGNAL
0x0	0, upper threshold is disabled
0x1	2048
0x2	4096
0x3	6144
•	•
•	•
•	•
0xFD	518144
0xFE	520192
0xFF	522240

PPG LO THRESHOLD1 (0x6B)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD1_LOWER[7:0]							
Reset	0x00							
Access Type	Write, Read							

THRESHOLD1_LOWER

Lower threshold for instance 1. Each LSB of the threshold represents 2048 LSBs the ambient light exposure code.

It is important to program the THRESHOLD1_UPPER to be greater than the THRESHOLD1_LOWER. Otherwise, the interrupt behavior is undefined.

THRESHOLD1_LOWER	AMBIENT LIGHT CORRECTED EXPOSURE SIGNAL
0x0	0, lower threshold is disabled
0x1	2048
0x2	4096
0x3	6144
•	•
•	•
•	•
0xFD	518144
0xFE	520192
0xFF	522240

PPG HI THRESHOLD2 (0x6C)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD2_UPPER[7:0]							
Reset	0xFF							
Access Type	Write, Read							

THRESHOLD2_UPPER

Upper threshold for instance 2. Each LSB of the threshold represents 2048 LSBs the ambient light exposure code.

It is important to program the THRESHOLD2_UPPER to be greater than the THRESHOLD2_LOWER. Otherwise, the interrupt behavior is undefined.

THRESHOLD2_UPPER	AMBIENT LIGHT CORRECTED EXPOSURE SIGNAL
0x0	0, upper threshold is disabled
0x1	2048
0x2	4096
0x3	6144
•	•
•	•
•	•
0xFD	518144

0xFE	520192
0xFF	522240

PPG LO THRESHOLD2 (0x6D)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD2_LOWER[7:0]							
Reset	0x00							
Access Type	Write, Read							

THRESHOLD2_LOWER

Lower threshold for instance 2. Each LSB of the threshold represents 2048 LSBs the ambient light exposure code.

It is important to program the THRESHOLD2_UPPER to be greater than the THRESHOLD2_LOWER. Otherwise, the interrupt behavior is undefined.

THRESHOLD2_LOWER	AMBIENT LIGHT CORRECTED EXPOSURE SIGNAL
0x0	0, lower threshold is disabled
0x1	2048
0x2	4096
0x3	6144
•	•
•	•
•	•
0xFD	518144
0xFE	520192
0xFF	522240

Picket Fence Measurement Select (0x70)

BIT	7	6	5	4	3	2	1	0
Field	PPG2_PF_MEAS_SEL[3:0]				PPG1_PF_MEAS_SEL[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

PPG2_PF_MEAS_SEL

PPG2_PF_MEAS_SEL[3:0] selects LED measurement for optical channel 2 for picket fence detect-and-replace.

PPGX_PF_SEL[3:0] (X= 1, 2)	ENUMERATION	DECODE
0x0	DISABLE	Picket fence detect disabled
0x1	MEAS1	Picket Fence detect and replace is done on measurement programmed in MEAS1 Setup registers for Optical Channel x

0x2	MEAS2	Picket Fence detect and replace is done on measurement programmed in MEAS2 Setup registers for Optical Channel x
0x3	MEAS3	Picket Fence detect and replace is done on measurement programmed in MEAS3 Setup registers for Optical Channel x
0x4	MEAS4	Picket Fence detect and replace is done on measurement programmed in MEAS4 Setup registers for Optical Channel x
0x5	MEAS5	Picket Fence detect and replace is done on measurement programmed in MEAS5 Setup registers for Optical Channel x
0x6	MEAS6	Picket Fence detect and replace is done on measurement programmed in MEAS6 Setup registers for Optical Channel x
0x7	MEAS7	Picket Fence detect and replace is done on measurement programmed in MEAS7 Setup registers for Optical Channel x
0x8	MEAS8	Picket Fence detect and replace is done on measurement programmed in MEAS8 Setup registers for Optical Channel x
0x9	MEAS9	Picket Fence detect and replace is done on measurement programmed in MEAS9 Setup registers for Optical Channel x
0xA to 0xF	RESERVED	Picket Fence detect disabled

PPG1_PF_MEAS_SEL

See PPG2_PF_MEAS_SEL[3:0] for details.

Picket Fence Configuration (0x71)

BIT	7	6	5	4	3	2	1	0
Field	–	PF_ORDER	IIR_TC[1:0]		IIR_INIT_VALUE[1:0]		THRESHOLD_SIGMA_MULT[1:0]	
Reset	–	0x1	0x00		0x00		0x00	
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	

PF_ORDER

PF_ORDER determines which prediction method is used: the last sample or a linear fit to the previous four samples. Refer to the Picket Fence Detect-and-Replace Function section for details.

VALUE	ENUMERATION	DECODE
0	OFF	Last Sample (1 point)
1	ON	Fit 4 points to a line for prediction (default)

IIR_TC

IIR_TC[1:0] determines the IIR filter bandwidth where the lowest setting has the narrowest bandwidth of a first-order filter.

Refer to the Picket Fence Detect-and-Replace Function section for details.

IIR_TC[1:0]	COEFFICIENT	SAMPLES TO 90%
00	1/64	146
01	1/32	72
10	1/16	35
11	1/8	17

IIR_INIT_VALUE

This IIR filter estimates the true standard deviation between the actual and predicted sample and tracks the ADC Range setting.

Refer to the Picket Fence Detect-and-Replace Function section for details.

IIR_INIT_VALUE[1:0]	CODE
00	64
01	48
10	32
11	24

THRESHOLD_SIGMA_MULT

GAIN resulting from the SIGMA_MULT[1:0] setting determines the number of standard deviations of the delta between the actual and predicted sample beyond which a picket-fence event is triggered.

Refer to the Picket Fence Detect-and-Replace Function section for details.

THRESHOLD_SIGMA_MULT[1:0]	GAIN
00	4
01	8
10	16
11	32

Interrupt1 Enable 1 (0x78)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN1	FRAME_RDY_EN1	FIFO_DATA_RDY_EN1	ALC_OVF_EN1	EXP_OVF_EN1	THRESH2_HILO_EN1	THRESH1_HILO_EN1	LED_TX_EN1
Reset	0b0	0b0	0b0	0b0	0b0	0x0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

A_FULL_EN1

If this bit is set to 1, INT1 is activated when the A_FULL bit in the Status 1 Register is asserted.

FRAME_RDY_EN1

If this bit is set to 1, INT1 is activated when the FRAME_RDY bit in the Status 1 Register is asserted.

FIFO_DATA_RDY_EN1

If this bit is set to 1, INT1 is activated when the FIFO_DATA_RDY bit in the Status 1 Register is asserted.

ALC_OVF_EN1

If this bit is set to 1, INT1 is activated when the ALC_OVF bit in the Status 1 Register is asserted.

EXP_OVF_EN1

If this bit is set to 1, INT1 is activated when the EXP_OVF bit in the Status 1 Register is asserted.

THRESH2_HILO_EN1

If this bit is set to 1, INT1 is activated when the THRESH2_HILO bit in the Status 1 Register is asserted.

THRESH1_HILO_EN1

If this bit is set to 1, INT1 is activated when the THRESH1_HILO bit in the Status 1 Register is asserted.

LED_TX_EN1

If this bit is set to 1, INT1 is activated 500ns before any of the nine LED Driver pins, LEDn_DRV (n = 1 to 9) gets asserted. This feature can be used in combination with the MAX20345 boost converter to switch it from a fully "off" state to a fully "on" state; thus, reducing the boost quiescent power and the effects of boost ripple on the MAX86171.

The application should not set any of the other bits in the Interrupt 1 Enable Registers when LED_TX_EN1 is set to 1.

Interrupt1 Enable 2 (0x79)

BIT	7	6	5	4	3	2	1	0
Field	LED9_COMPB_EN1	VDD_OOR_EN1	–	–	–	INVALID_CFG_EN1	–	–
Reset	0b0	0b0	–	–	–	0b0	–	–
Access Type	Write, Read	Write, Read	–	–	–	Write, Read	–	–

LED9_COMPB_EN1

If this bit is set to 1, INT1 is activated when the LED9_COMPB bit in the Status 2 Register is asserted.

VDD_OOR_EN1

If this bit is set to 1, INT1 is activated when the VDD_OOR bit in the Status 2 Register is asserted. If both VDD_OOR_EN1 and VDD_OOR_EN2 are set to 0 then the OOR circuit is shutdown.

INVALID_CFG_EN1

If this bit is set to 1, INT1 is activated when the INVALID_CFG bit in the Status 2 Register is asserted.

Interrupt1 Enable 3 (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	LED8_COMPB_EN1	LED7_COMPB_EN1	LED6_COMPB_EN1	LED5_COMPB_EN1	LED4_COMPB_EN1	LED3_COMPB_EN1	LED2_COMPB_EN1	LED1_COMPB_EN1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

LED8_COMPB_EN1

If this bit is set to 1, INT1 is activated when the LED8_COMPB bit in the Status 3 Register is asserted.

LED7_COMPB_EN1

If this bit is set to 1, INT1 is activated when the LED7_COMPB bit in the Status 3 Register is asserted.

LED6_COMPB_EN1

If this bit is set to 1, INT1 is activated when the LED6_COMPB bit in the Status 3 Register is asserted.

LED5_COMPB_EN1

If this bit is set to 1, INT1 is activated when the LED5_COMPB bit in the Status 3 Register is asserted.

LED4_COMPB_EN1

If this bit is set to 1, INT1 is activated when the LED4_COMPB bit in the Status 3 Register is asserted.

LED3_COMPB_EN1

If this bit is set to 1, INT1 is activated when the LED3_COMPB bit in the Status 3 Register is asserted.

LED2_COMPB_EN1

If this bit is set to 1, INT1 is activated when the LED2_COMPB bit in the Status 3 Register is asserted.

LED1_COMPB_EN1

If this bit is set to 1, INT1 is activated when the LED1_COMPB bit in the Status 3 Register is asserted.

Interrupt2 Enable 1 (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN2	FRAME_RDY_EN2	FIFO_DATA_RDY_EN2	ALC_OVF_EN2	EXP_OVF_EN2	THRESH2_HILO_EN2	THRESH1_HILO_EN2	LED_TX_EN2
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

A_FULL_EN2

If this bit is set to 1, INT2 is activated when the A_FULL bit in the Status 1 Register is asserted

FRAME_RDY_EN2

If this bit is set to 1, INT2 is activated when the FRAME_RDY bit in the Status 1 Register is asserted.

FIFO_DATA_RDY_EN2

If this bit is set to 1, INT2 is activated when the FIFO_DATA_RDY bit in the Status 1 Register is asserted.

ALC_OVF_EN2

If this bit is set to 1, INT2 is activated when the ALC_OVF bit in the Status 1 Register is asserted

EXP_OVF_EN2

If this bit is set to 1, INT2 is activated when the EXP_OVF bit in the Status 1 Register is asserted.

THRESH2_HILO_EN2

If this bit is set to 1, INT2 is activated when the THRESH2_HILO bit in the Status 1 Register is asserted.

THRESH1_HILO_EN2

If this bit is set to 1, INT2 is activated when the THRESH1_HILO bit in the Status 1 Register is asserted.

LED_TX_EN2

If this bit is set to 1, INT2 is activated 500ns before any of the nine LED Driver pins, LEDn_DRV (n = 1 to 9) gets asserted. This feature can be used in combination with MAX20345 boost converter to switch it from a fully "off" state to a fully "on" state; thus, reducing the boost quiescent power and the effects of boost ripple on the MAX86171.

The application should not set any of the other bits in the Interrupt 2 Enable Registers when LED_TX_EN2 is set to 1.

Interrupt2 Enable 2 (0x7D)

BIT	7	6	5	4	3	2	1	0
Field	LED9_COMPB_EN2	VDD_OOR_EN2	–	–	–	INVALID_CFG_EN2	–	–
Reset	0b0	0b0	–	–	–	0b0	–	–
Access Type	Write, Read	Write, Read	–	–	–	Write, Read	–	–

LED9_COMPB_EN2

If this bit is set to 1, INT2 is activated when the LED9_COMPB bit in the Status 2 Register is asserted.

VDD_OOR_EN2

If this bit is set to 1, INT2 is activated when the VDD_OOR bit in the Status 2 Register is asserted. If both VDD_OOR_EN1 and VDD_OOR_EN2 are set to 0 then the OOR circuit is shutdown

INVALID_CFG_EN2

If this bit is set to 1, INT2 is activated when the INVALID_CFG bit in the Status 2 Register is asserted.

Interrupt2 Enable 3 (0x7E)

BIT	7	6	5	4	3	2	1	0
Field	LED8_COMPB_EN2	LED7_COMPB_EN2	LED6_COMPB_EN2	LED5_COMPB_EN2	LED4_COMPB_EN2	LED3_COMPB_EN2	LED2_COMPB_EN2	LED1_COMPB_EN2
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

LED8_COMPB_EN2

If this bit is set to 1, INT2 is activated when the LED8_COMPB bit in the Status 3 Register is asserted.

LED7_COMPB_EN2

If this bit is set to 1, INT2 is activated when the LED7_COMPB bit in the Status 3 Register is asserted.

LED6_COMPB_EN2

If this bit is set to 1, INT2 is activated when the LED6_COMPB bit in the Status 3 Register is asserted.

LED5_COMPB_EN2

If this bit is set to 1, INT2 is activated when the LED5_COMPB bit in the Status 3 Register is asserted.

LED4_COMPB_EN2

If this bit is set to 1, INT2 is activated when the LED4_COMPB bit in the Status 3 Register is asserted.

LED3_COMPB_EN2

If this bit is set to 1, INT2 is activated when the LED3_COMPB bit in the Status 3 Register is asserted.

LED2_COMPB_EN2

If this bit is set to 1, INT2 is activated when the LED2_COMPB bit in the Status 3 Register is asserted.

LED1_COMPB_EN2

If this bit is set to 1, INT2 is activated when the LED1_COMPB bit in the Status 3 Register is asserted.

Part ID (0xFF)

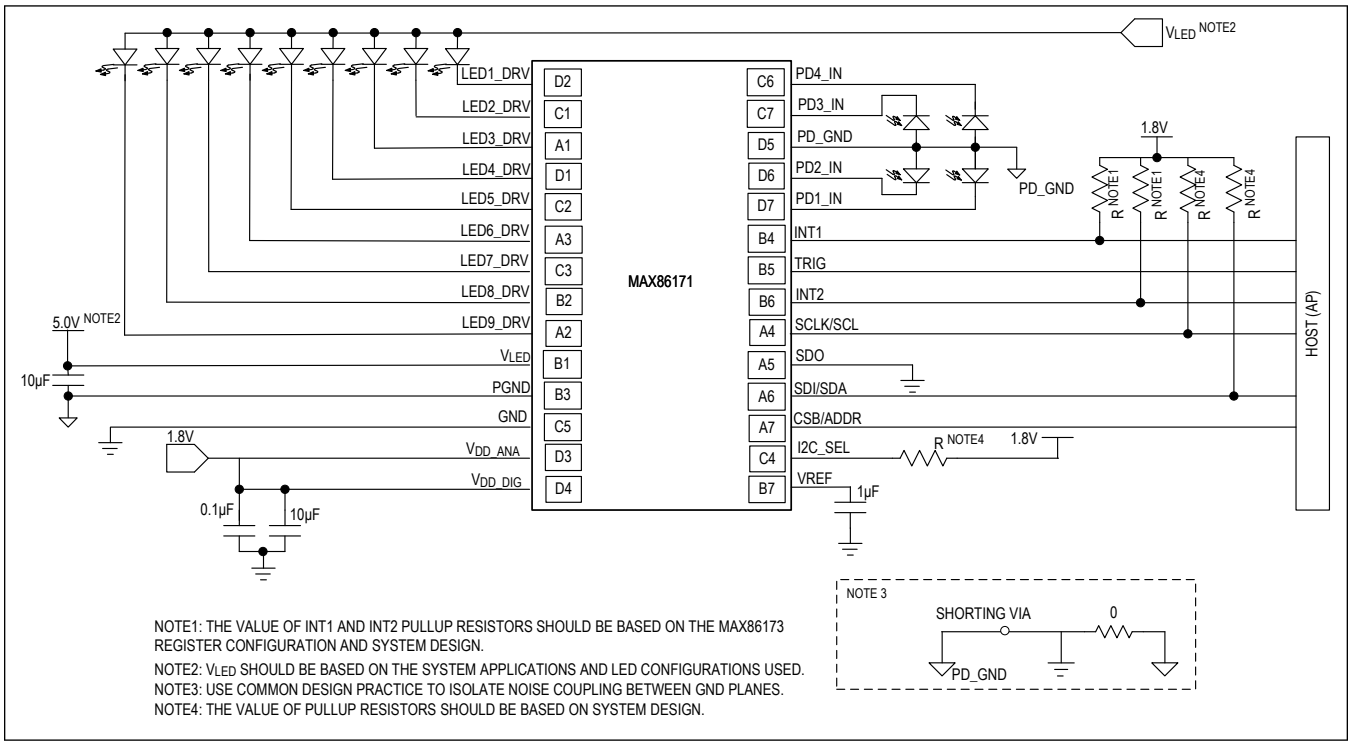
BIT	7	6	5	4	3	2	1	0
Field	PART_ID[7:0]							
Reset	0x2C							
Access Type	Read Only							

PART_ID

This register stores the part identifier for the chip.

Typical Application Circuits

I²C Mode



NOTE1: THE VALUE OF INT1 AND INT2 PULLUP RESISTORS SHOULD BE BASED ON THE MAX86173 REGISTER CONFIGURATION AND SYSTEM DESIGN.

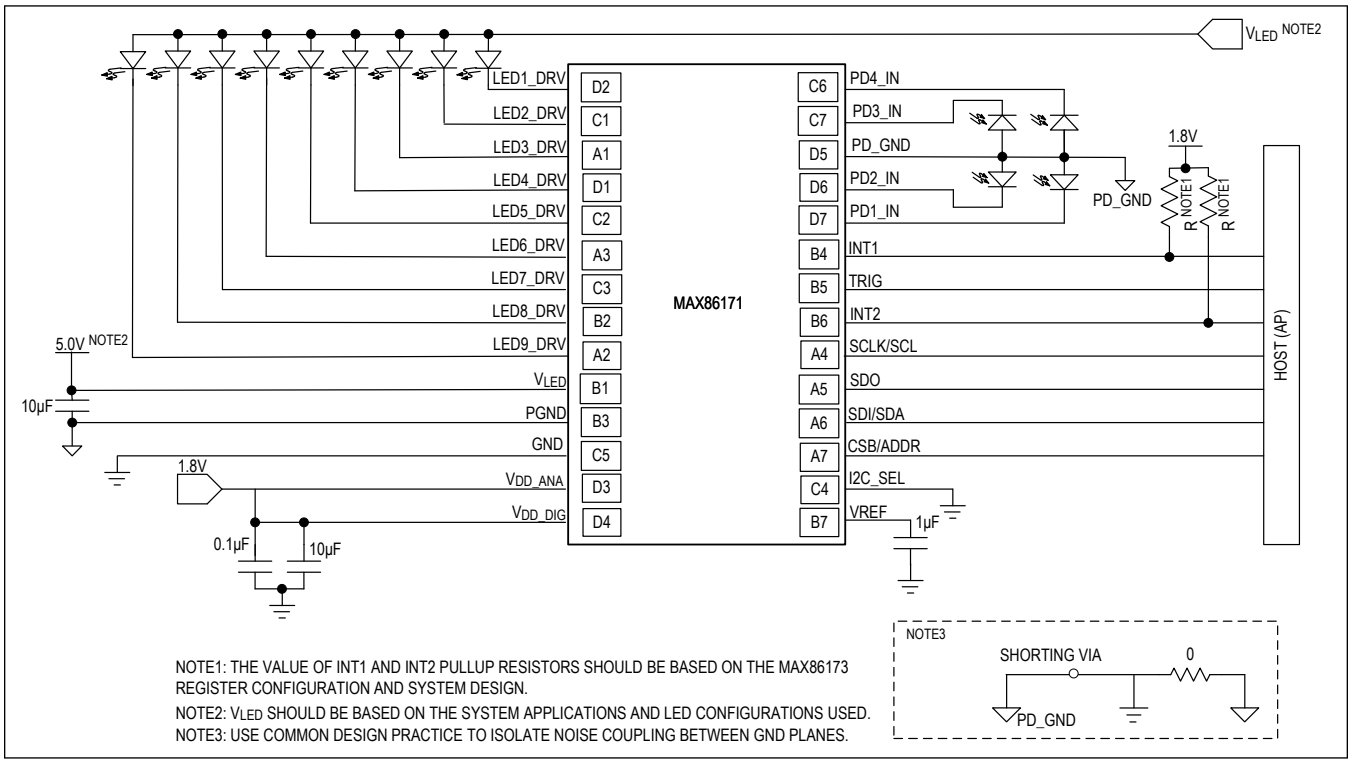
NOTE2: V_{LED} SHOULD BE BASED ON THE SYSTEM APPLICATIONS AND LED CONFIGURATIONS USED.

NOTE3: USE COMMON DESIGN PRACTICE TO ISOLATE NOISE COUPLING BETWEEN GND PLANES.

NOTE4: THE VALUE OF PULLUP RESISTORS SHOULD BE BASED ON SYSTEM DESIGN.

Typical Application Circuits (continued)

SPI Mode



Ordering Information

PART NUMBER	TEMP.RANGE	BUMP
MAX86171ENI+	-40°C to +85°C	28 WLP
MAX86171ENI+T	-40°C to +85°C	28 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/19	Initial release	—
1	2/21	Updated the *Benefits and Features, Simplified Block Diagram, Pin Description, Detailed Description, Optical Receiver Overview, Scan Modes, Scan_Mode_, Measurement Sequence Control (address 0x0C to address 0x0D), Picket Fence Detect-and-Replace Function, and Typical Application Circuits* sections; replaced Figures 18–21; updated Register Bits FR_CLK_DIV_H	1, 7, 18–21, 27, 34, 40–42, 65, 102–103
2	10/21	Updated title, *Simplified Block Diagram*, *Absolute Maximum Ratings*, replaced Figure 4, 18–21, updated FiFO_A_FULL (address 0x09), *Slave Address*, *Typical Application Circuits I^2C Mode*, *Typical Application Circuits SPI Mode*, and *PWR_RDY*	1, 3, 20, 28, 36, 38–40, 48, 97, 98
3	12/21	Updated *Ordering Information*	98
4	06/22	Updated *Ordering Information*	98

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