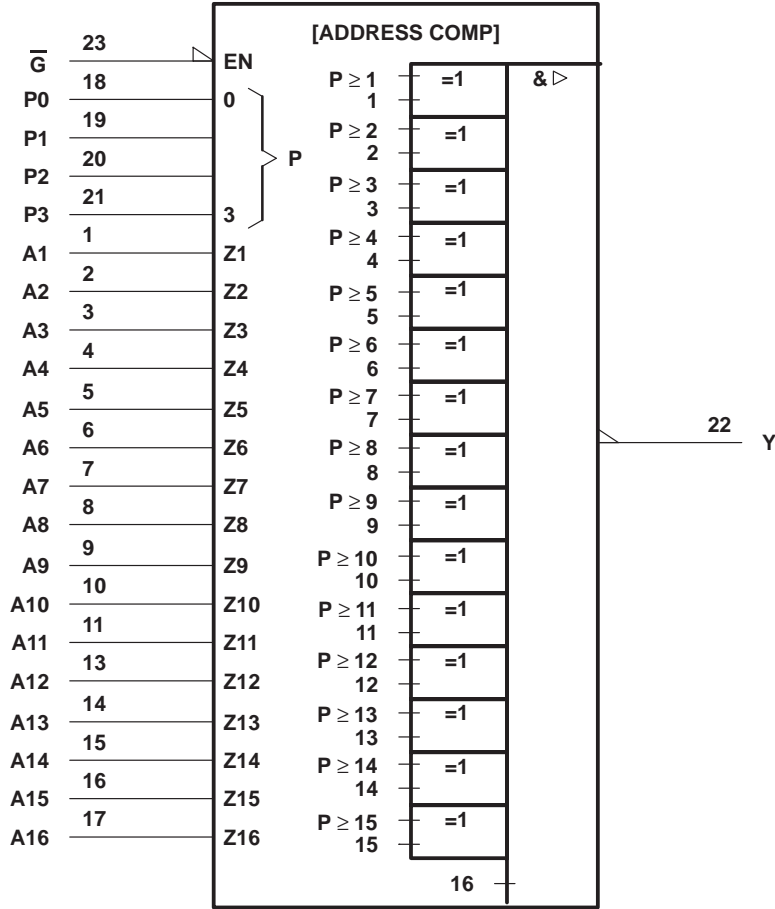


SN74ALS677A 16-BIT ADDRESS COMPARATOR

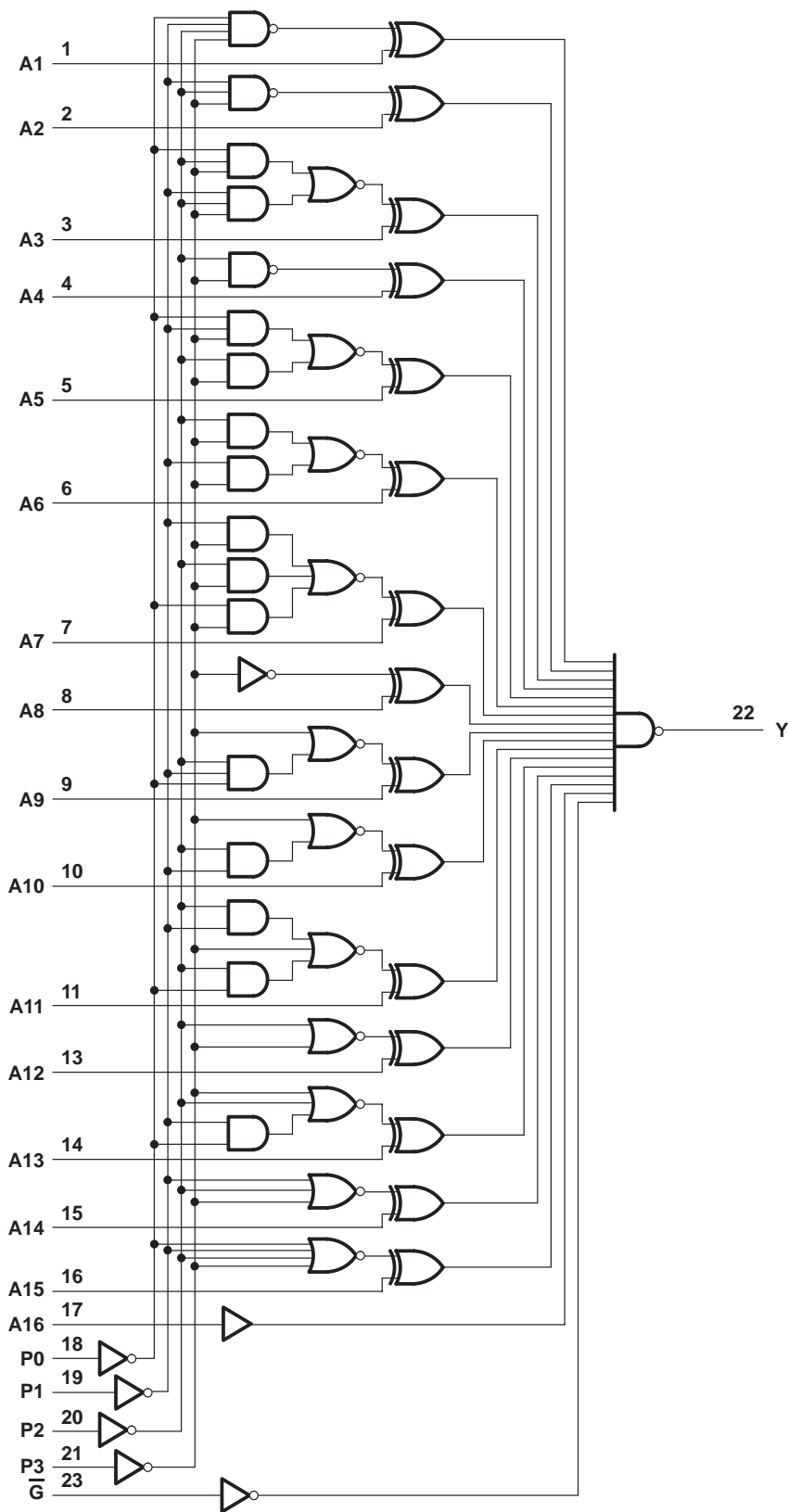
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			-2.6	mA
I_{OL} Low-level output current			24	mA
T_A Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT	
V_{IK}	$V_{CC} = 4.5 V$, $I_I = -18 mA$			-1.2	V	
V_{OH}	$V_{CC} = 4.5 V$ to $5.5 V$, $I_{OH} = -0.4 mA$	$V_{CC} - 2$			V	
	$V_{CC} = 4.5 V$, $I_{OH} = -2.6 mA$	2.4	3.2			
V_{OL}	$V_{CC} = 4.5 V$	$I_{OL} = 12 mA$		0.25	0.4	V
		$I_{OL} = 24 mA$		0.35	0.5	
I_I	$V_{CC} = 5.5 V$, $V_I = 7 V$			0.1	mA	
I_{IH}	$V_{CC} = 5.5 V$, $V_I = 2.7 V$			20	μA	
I_{IL}	$V_{CC} = 5.5 V$, $V_I = 0.4 V$			-0.1	mA	
I_{O}^{\S}	$V_{CC} = 5.5 V$, $V_O = 2.25 V$	-30		-112	mA	
I_{CC}	$V_{CC} = 5.5 V$		21	33	mA	

‡ All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 V$ to $5.5 V$, $C_L = 50 pF$, $R_L = 500 \Omega$, $T_A = MIN$ to $MAX^{\dagger\dagger}$		UNIT
			MIN	MAX	
t_{PLH}	Any P	Y	4	25	ns
t_{PHL}			8	38	
t_{PLH}	Any A	Y	5	22	ns
t_{PHL}			5	30	
t_{PLH}	\bar{G}	Y	3	13	ns
t_{PHL}			5	35	

†† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



APPLICATION INFORMATION

The SN74ALS677A can be wired to recognize any one of 2^{16} addresses. The number of lows in the address determines the input pattern for the P inputs. Those system address lines that are low in the address to be recognized are connected to the lowest-numbered A inputs of the address comparator. The system address lines that are high are connected to the highest-numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	L	L	H	H	H	H

Because the address contains six lows and ten highs, the following connections are made:

- P3 to 0 V, P2 to V_{CC} , P1 to V_{CC} , and P0 to 0 V
- System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order
- The remaining ten system address lines to comparator inputs A7 through A16 in any convenient order

The output provides an active-low enabling signal.

Figure 1 shows a modulo-N synchronous counter. The 'ALS163B provides a low-level clear signal when $N = FEFF_{16}$.

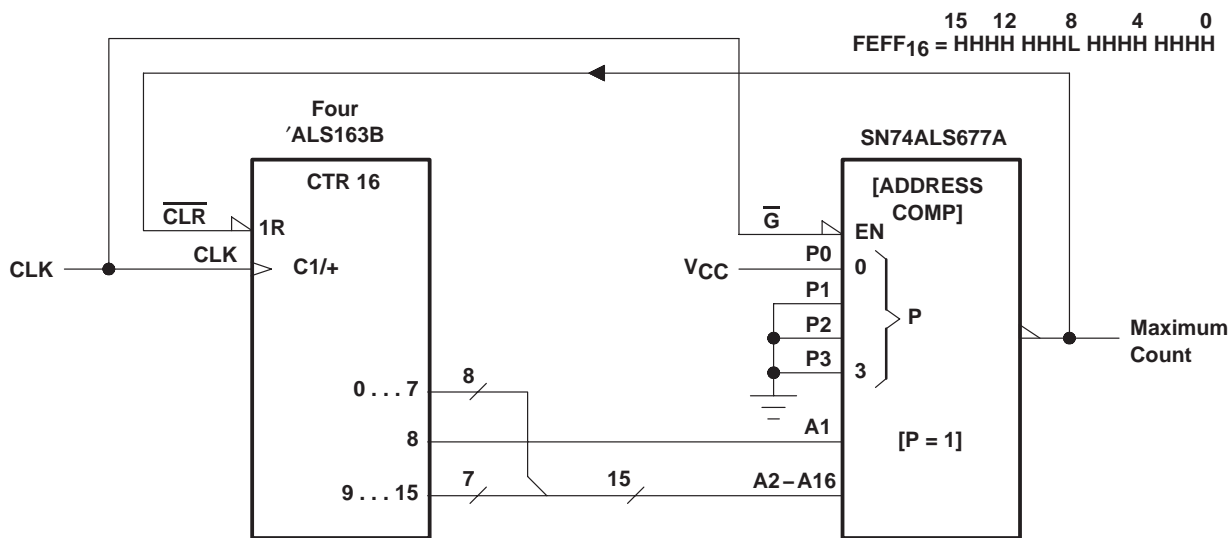


Figure 1. Modulo-N Synchronous Counter

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- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms



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