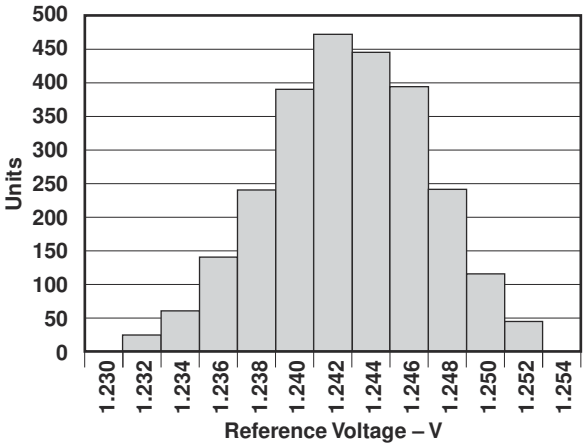
TLV3011-Q1 和 TLV3012-Q1 具有集成 1.24V 电压基准的低功耗比较器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 低静态电流：5 µA（最大值）
- 集成电压基准：1.242 V
- 输入共模范围：超过电源轨 200mV
- 电压基准初始精度：1%
- 开漏输出选项 (TLV3011-Q1)
- 推挽输出选项 (TLV3012-Q1)
- 快速响应时间：6uS
- 低电源电压范围：1.8V 至 5.5V

2 应用

- 车道偏离警告
- 仪表组
- 收费标签
- 资产跟踪
- 电池管理系统



基准电压分布

3 说明

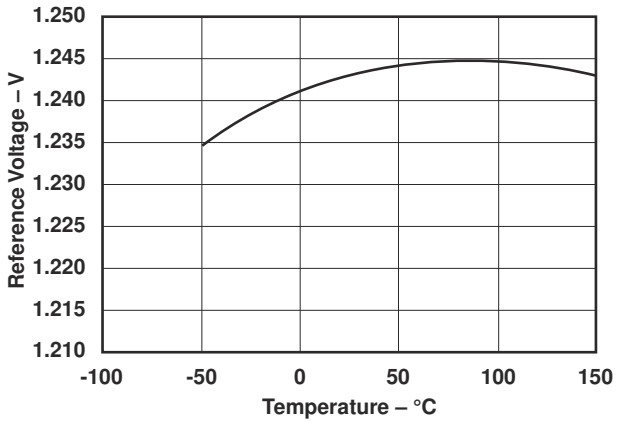
TLV3011-Q1 是一款低功耗、开漏输出比较器；TLV3012-Q1 是一款推挽输出比较器。这两款器件均具有未指定的片上电压基准，静态电流为 5 µA（最大值），输入共模范围超出电源轨 200mV，单电源工作电压范围为 1.8V 至 5.5V。集成的 1.242V 系列电压基准提供 100ppm/°C（最大）的低漂移，在高达 10nF 的容性负载下保持稳定，并且可以提供高达 0.5mA（典型值）的输出电流。

TLV3011-Q1 和 TLV3012-Q1 采用微型 SOT23-6 封装，可实现节省空间的设计；采用 SC-70 封装，可更大限度地节省电路板面积。两个版本的额定工作温度范围为 –40°C 至 +125°C。

器件信息

器件型号	封装 (1)	封装尺寸（标称值）
TLV3011-Q1、TLV3012-Q1	SOT-23 (6)	2.90mm × 1.60mm
	SC-70 (6)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



基准电压与温度间的关系

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (June 2019) to Revision B (August 2022)	Page
• 在 DBV 和 DCK 封装中添加了 TLV3011-Q1	1
• 在 SOT-23 (DBV) 中添加了 TLV3012-Q1	1
• 为 DBV 封装添加了新表	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

Changes from Revision * (March 2011) to Revision A (June 2019)	Page
• 添加了 HBM 和 CDM ESD 等级和分级等级还添加了 AEC-Q100 器件温度等级	1
• 更改了*应用* 列表	1
• 添加了*引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• 从数据表中删除了 TLV3011-Q1 器件，并从 TLV3012-Q1 器件型号中删除了 *A*	1
• Deleted the *Package Ordering Information* section	3
• Moved the switching characteristics from the *Electrical Characteristics* table to the *Switching Characteristics* table	8

5 Pin Configuration and Functions

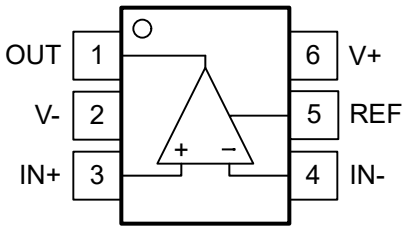


图 5-1. DCK, DBV Package
6-Pin SC-70, SOT-23
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT	O	Comparator Output
2	V –	-	Negative (lowest) power supply
3	IN+	I	Non-inverting comparator input
4	IN –	I	Inverting comparator input
5	REF	O	Reference Output
6	V+	-	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.5	7	V
Input pins (IN+, IN–) from (V–)(2)	–0.5	(V+) + 0.5	V
Current into Input pins (IN+, IN–)(2)	–10	10	mA
Output short circuit current(3)	Continuous		mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-0111	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Thermal Information

THERMAL METRIC(1)		TLV3011-Q1, TLV3012-Q1		UNIT
		DCK (SC-70)	DBV (SOT-23)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.8	162.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	120.5	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.2	42.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.9	21.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.0	41.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage, V_S = (V+) – (V–)	1.8	5.5	V
Input Voltage Range, I_{VR}	(V-) - 0.2	(V+) + 0.2	V
Output voltage range from (V–) for open drain	V-	⩽ V+	V
Ambient Temperature, T_A	–40	125	°C

6.5 Electrical Characteristics - DBV Package

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 1.8V and 5.5V, V_{CM} = V_S /2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = (V–)	–6	±0.3	6	mV
V_{OS}	Input offset voltage	V_{CM} = (V–) T_A = –40°C to +125°C	–9		9	mV
dV_{IO}/dT	Input offset voltage drift	V_{CM} = (V–) T_A = –40°C to +125°C		±12		µV/°C
PSRR	power supply rejection ratio	V_{CM} = (V–) V_S = 1.8 V to 5.5 V T_A = –40°C to +125°C		100	1000	µV/V
V_{HYS}	Input hysteresis voltage	T_A = –40°C to +125°C	2	6	8	mV
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S /2	–10(1)	±4.5	10(1)	pA
I_{OS}	Input offset current	V_{CM} = V_S /2	–10(1)	±1	10(1)	pA
INPUT COMMON MODE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V to 5.5 V	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common mode rejection ratio	V_{CM} = (V–) + 1.5V to (V+) + 0.2V	57	74		dB
CMRR	Common mode rejection ratio	V_{CM} = (V–) - 0.2V to (V+) + 0.2V	50	62		dB
R_{CM}	Input Common Mode Resistance			10^{13}		Ω
C_{IC}	Input Common Mode Capacitance			2		pF
INPUT IMPEDANCE						
R_{DM}	Input Differential Mode Resistance			10^{13}		Ω
C_{ID}	Input Differential Mode Capacitance			4		pF
OUTPUT						
V_{OL}	Voltage swing from (V–)	V_S = 5 V I_{SINK} = 5 mA T_A = –40°C to +125°C		160	200	mV
V_{OH}	Voltage swing from (V+) (for Push-Pull only)	V_S = 5 V I_{SOURCE} = 5 mA T_A = –40°C to +125°C		90	200	mV
VOLTAGE REFERENCE						
V_{OUT}	Reference Voltage		1.223	1.242	1.260	V
	Accuracy			±0.25%	±1.5%	
	Reference Voltage	T_A = –40°C to +125°C	1.208	1.242	1.276	V
dV_{OUT}/d_T	Temperature Drift	T_A = –40°C to +125°C		40	100	ppm/℃
dV_{OUT}/dI_{LOAD}	Load Regulation, Sourcing	0 mA < I_{SOURCE} ⩽ 0.5 mA		0.36	1(1)	mV/mA
	Load Regulation, Sinking	0 mA < I_{SINK} ⩽ 0.5 mA		6.6		mV/mA
ILOAD	Output Current			0.5		mA

6.5 Electrical Characteristics - DBV Package (continued)

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V –) = 1.8V and 5.5V, V_{CM} = V_S /2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dV_{OUT}/dV_S	Line Regulation	1.8 V ⩽ V_S ⩽ 5.5 V		10	100(1)	µV/V
V_{noise}	Noise	f = 0.1 Hz to 10 Hz		0.2		mV_{PP}
POWER SUPPLY						
I_Q	Quiescent current per comparator	Output is logic high		2.8	5	µA

(1) Ensured by characterization

6.6 Switching Characteristics - DBV Package

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V –) = 1.8 V and 5.5 V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-LH}	Propagation delay time, low-to-high	f = 10 kHz, V_{STEP} = 1V, V_{OD} = 10 mV, C_L = 10 pF		12		µs
T_{PD-LH}	Propagation delay time, low-to-high	f = 10 kHz, V_{STEP} = 1V, V_{OD} = 100 mV, C_L = 10 pF		6		µs
T_{PD-HL}	Propagation delay time, high-to-low	f = 10 kHz, V_{STEP} = 1V, V_{OD} = 10 mV, C_L = 10 pF		13.5		µs
T_{PD-HL}	Propagation delay time, high-to-low	f = 10 kHz, V_{STEP} = 1V, V_{OD} = 100 mV, C_L = 10 pF		6.5		µs
T_{RISE}	Output Rise Time, 20% to 80%, push-pull output	C_L = 10 pF		100		ns
T_{RISE}	Output Rise Time, 20% to 80%, open-drain output	R_L = 10 kΩ, C_L = 10 pF		200		ns
T_{FALL}	Output Fall Time, 80% to 20%	C_L = 10 pF		100		ns
T_{FALL}	Output Fall Time, 80% to 20%, open-drain output	R_L = 10 kΩ, C_L = 10 pF		200		ns

6.7 Electrical Characteristics - DCK Package

V_S = 1.8 V to 5.5 V, at T_A = 25°C, V_{OUT} = V_S, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = 0 V, I_O = 0 V		0.5	15	mV
dV_{OS}/dT	Input offset voltage vs temperature	T_A = –40°C to +125°C		±12		µV/°C
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5.5 V		100	1000	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		±10		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		±10		pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = –0.2 V to (V+) – 1.5 V	60	74		dB
		V_{CM} = –0.2 V to (V+) + 0.2 V	54	62		
INPUT IMPEDANCE						
	Common mode			10^{13} // 2		Ω // pF
	Differential			10^{13} // 4		Ω // pF
OUTPUT						
V_{OL}	Voltage output low from rail	V_S = 5 V, I_{OUT} = –5 mA		160	200	mV
V_{OH}	Voltage output high from rail	V_S = 5 V, I_{OUT} = 5 mA		90	200	mV
	Short-circuit current				See Typical Characteristics	
VOLTAGE REFERENCE						
V_{OUT}	Output voltage		1.208	1.242	1.276	V
	Initial accuracy				±1%	
dV_{OUT}/d_T	Temperature drift	–40°C ≤ T_A ≤ 125°C		40	100	ppm/°C
dV_{OUT}/dI_{LOAD}	Load regulation, sourcing	0 mA < I_{SOURCE} ≤ 0.5 mA		0.36	1	mV/mA
	Load regulation, sinking	0 mA < I_{SINK} ≤ 0.5 mA		6.6		
I_{LOAD}	Output current			0.5		mA
dV_{OUT}/dV_{IN}	Line regulation	1.8 V ≤ V_{IN} ≤ 5.5 V		10	100	µV/V
NOISE						
	Reference voltage noise	f = 0.1 Hz to 10 Hz		0.2		mV_{PP}
POWER SUPPLY						
V_S	Specified voltage		1.8		5.5	V
	Operating voltage range		1.8		5.5	V
I_Q	Quiescent current	V_S = 5 V, V_O = High		2.8	5	µA
TEMPERATURE						
	Operating range		–40		125	°C
	Storage range		–65		150	°C

6.8 Switching Characteristics - DCK Package

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Propagation delay time, low to high	f = 10 kHz, V_{STEP} = 1 V, input overdrive = 10 mV		12		µs
		f = 10 kHz, V_{STEP} = 1 V, input overdrive = 100 mV		6		
	Propagation delay time, high to low	f = 10 kHz, V_{STEP} = 1 V, input overdrive = 10 mV		13.5		µs
		f = 10 kHz, V_{STEP} = 1 V, input overdrive = 100 mV		6.5		
t_r	Rise time	C_L = 10 pF		100		ns
t_f	Fall time	C_L = 10 pF		100		ns

7 Typical Characteristics

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.

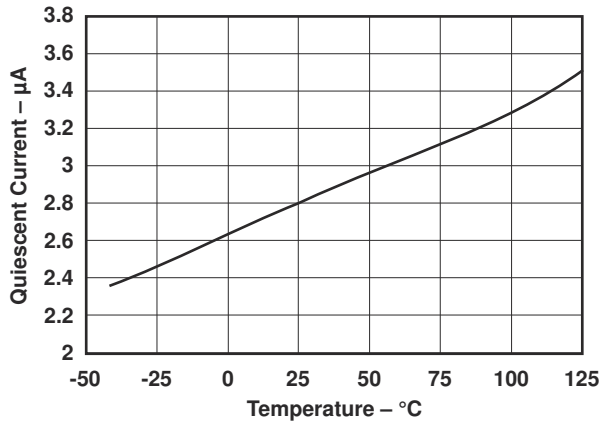


图 7-1. Quiescent Current vs Temperature

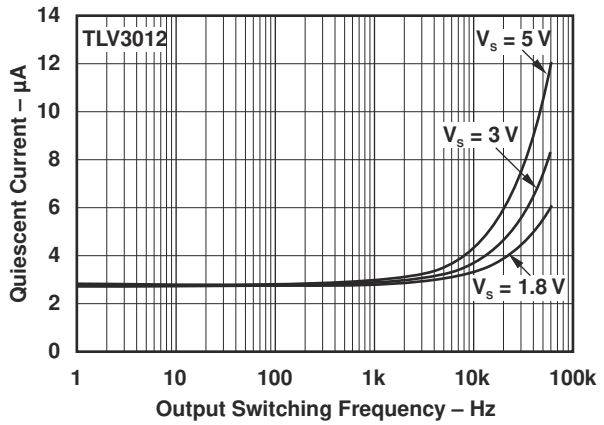


图 7-2. Quiescent Current vs Output Switching Frequency

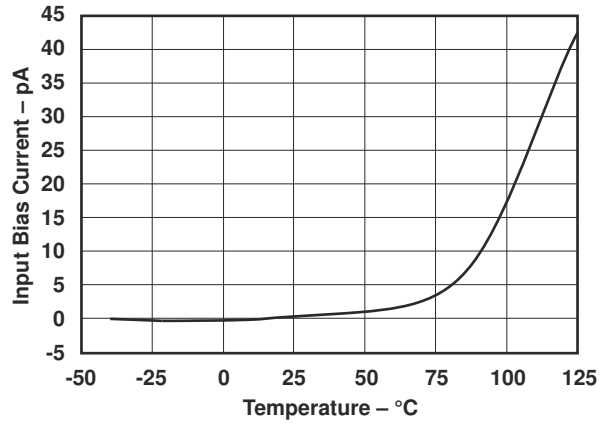


图 7-3. Input Bias Current vs Temperature

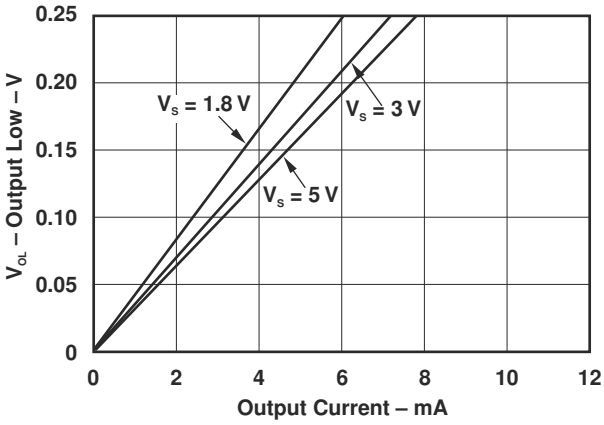


图 7-4. Output Low vs Output Current

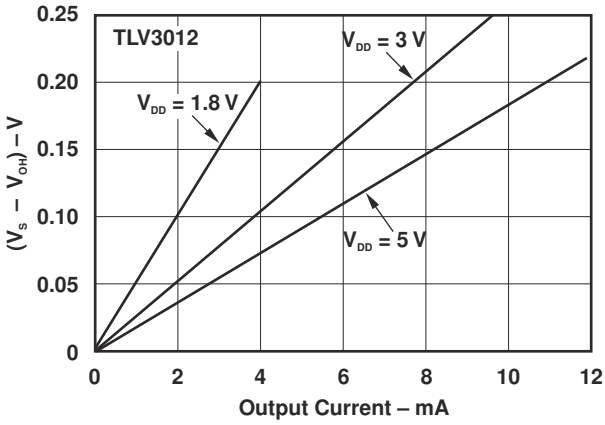


图 7-5. Output High vs Output Current

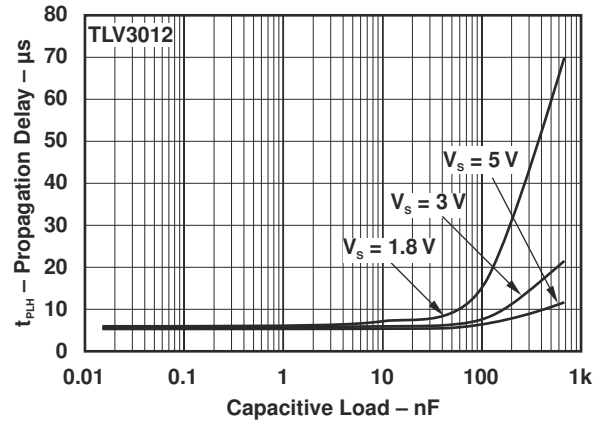


图 7-6. Propagation Delay (t_{PLH}) vs Capacitive Load

7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.

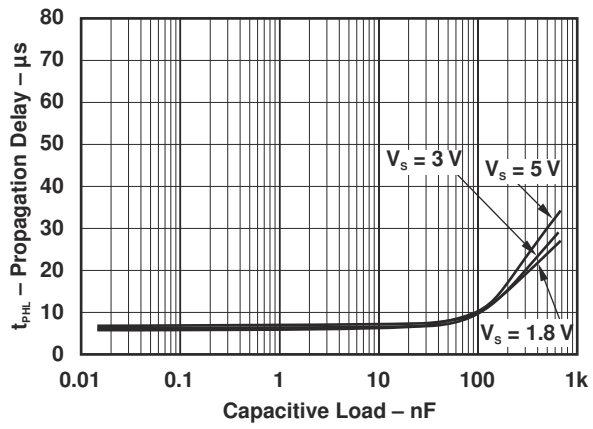


图 7-7. Propagation Delay (t_{PHL}) vs Capacitive Load

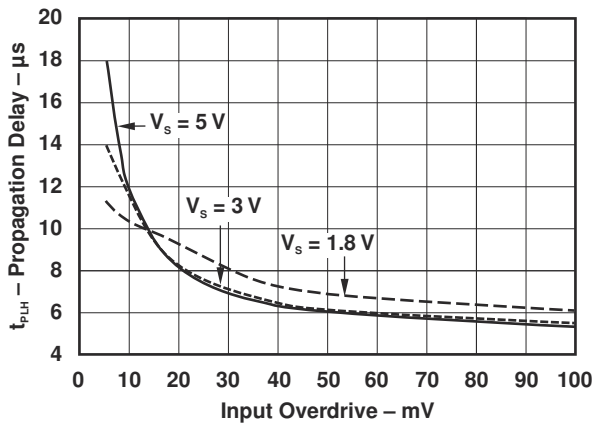


图 7-8. Propagation Delay (t_{PLH}) vs Input Overdrive

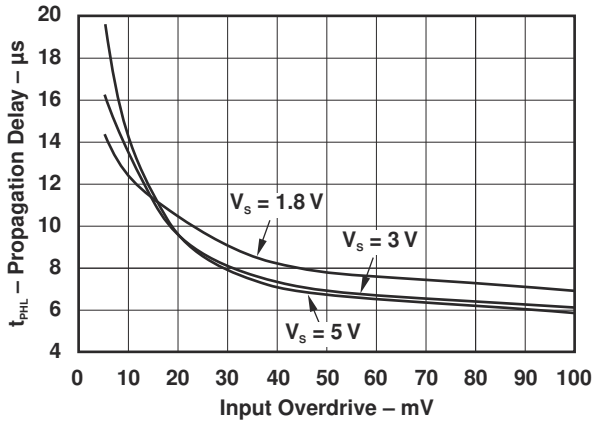


图 7-9. Propagation Delay (t_{PHL}) vs Input Overdrive

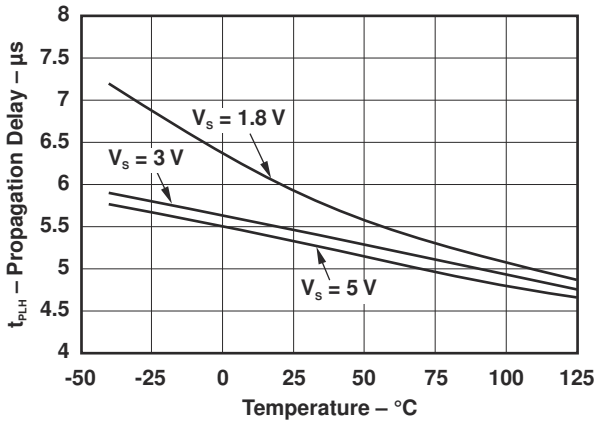


图 7-10. Propagation Delay (t_{PLH}) vs Temperature

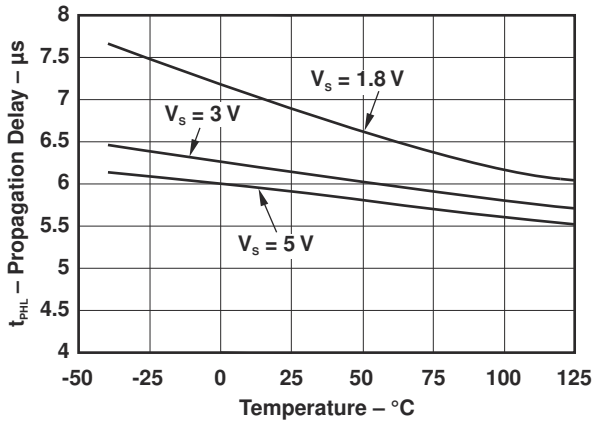


图 7-11. Propagation Delay (t_{PHL}) vs Temperature

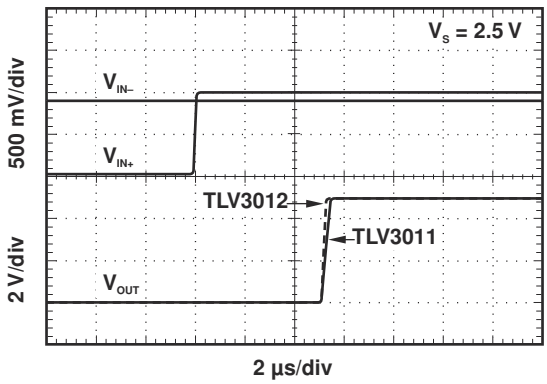


图 7-12. Propagation Delay (t_{PLH})

7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.

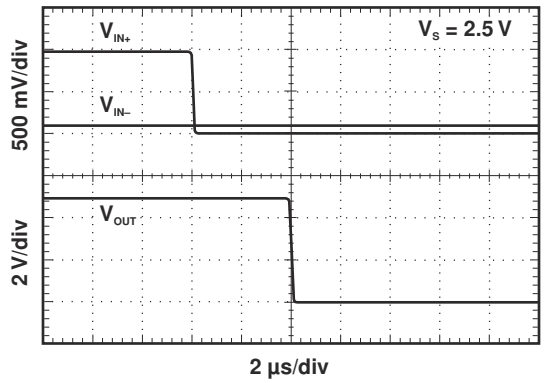


图 7-13. Propagation Delay (t_{PHL})

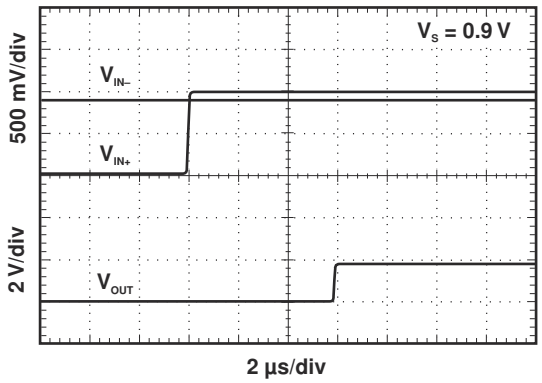


图 7-14. Propagation Delay (t_{PLH})

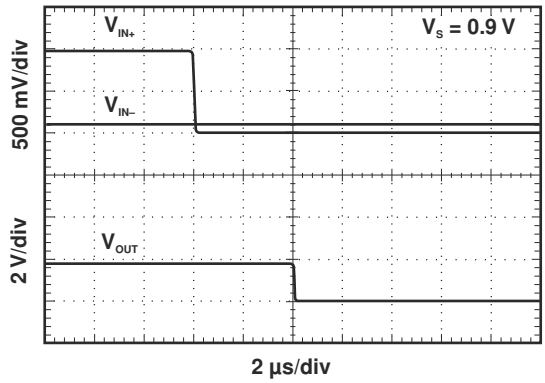


图 7-15. Propagation Delay (t_{PHL})

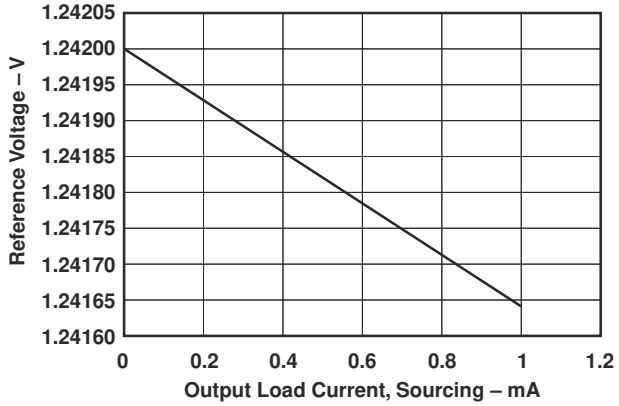


图 7-16. Reference Voltage vs Output Load Current (Sourcing)

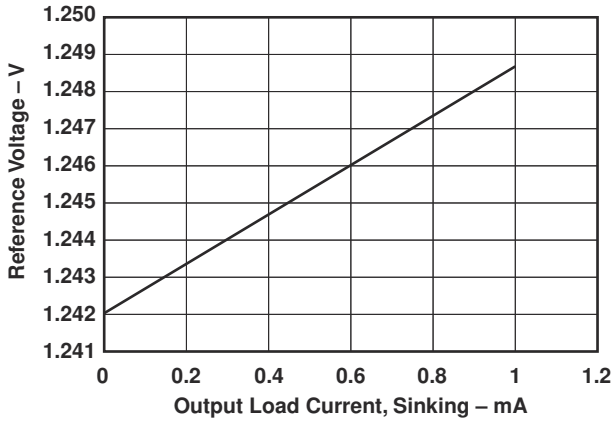


图 7-17. Reference Voltage vs Output Load Current (Sinking)

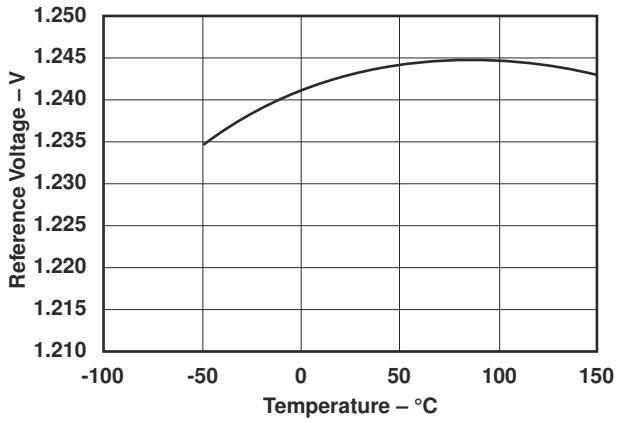


图 7-18. Reference Voltage vs Temperature

7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.

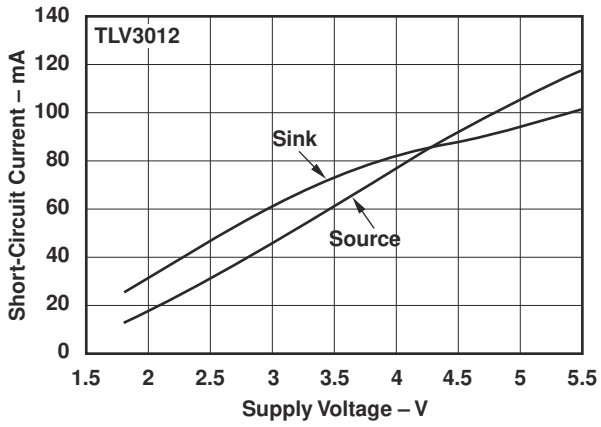


图 7-19. Short-Circuit Current vs Supply Voltage

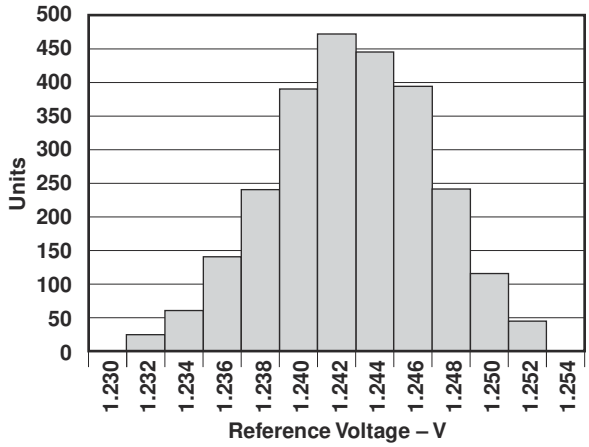


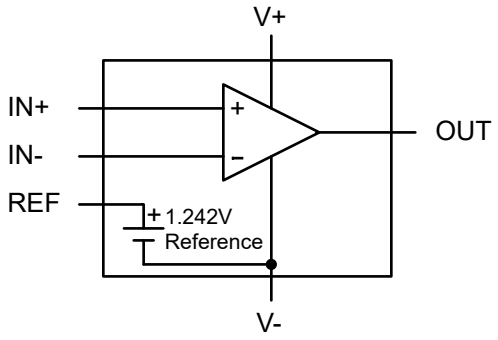
图 7-20. Reference Voltage Distribution

8 Detailed Description

8.1 Overview

The TLV301x-Q1 is a MicroPower comparator with an integrated reference that is well suited for compact, low-current, precision voltage detection applications. With a high-accuracy, internal reference of 1.242 V and 5 uA of quiescent current, the TLV301x-Q1 enables power conscious systems to monitor and respond quickly to fault conditions.

8.2 Functional Block Diagram



8.3 Feature Description

The TLV301x-Q1 is comprised of a rail-to-rail input comparator with open-drain or push-pull output options and a voltage reference that is externally available.

8.4 Device Functional Modes

The TLV301x-Q1 requires an operating voltage between 1.8 V and 5.5 V for the comparator output to reflect the voltage applied to the inputs. Similarly, the reference output (REF) will also be valid over the same operating voltage range.

8.4.1 Open Drain Output (TLV3011-Q1)

The TLV3011-Q1 features an Open-Drain (sinking only) output that allows multiple devices to be driven by a single pull-up resistor to accomplish an OR function, making the TLV3011-Q1 useful for logic applications. The value of the pull-up resistor and supply voltage used will affect current consumption due to additional current drawn when the output is in a low state. This effect can be seen in the typical curve Quiescent Current vs Output Switching Frequency.

The pull-up voltage should NOT exceed the V+ suppply.

8.4.2 Push-Pull Output (TLV3012-Q1)

The TLV3012-Q1 has a "Push-Pull" output capable of both sinking and sourcing current. The push-pull output stage is optimal for reduced power budget applications by eliminating the need for a pull-up resistor and features no shoot-through current. Do not tie push-pull outputs together.

8.4.3 Voltage Reference

The integrated 1.242-V voltage reference offers low 100-ppm/°C (maximum) drift provided on a seporate output pin that allows use of external dividers or to provide a reference voltage for other external circuitry. The reference is stable with up to a 10-nF capacitive load and can sink or source up to 500µA (typical) of output current.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TLV301x-Q1 comparator family with on-chip 1.242-V series reference with the choice of either open-drain or push-pull output stages.

A typical supply current of 2.8 μA and small packaging combine with 1.8-V supply requirements to make the TLV301x devices optimal for battery and portable designs.

图 9-1 shows the typical connections for the TLV3012-Q1 device.

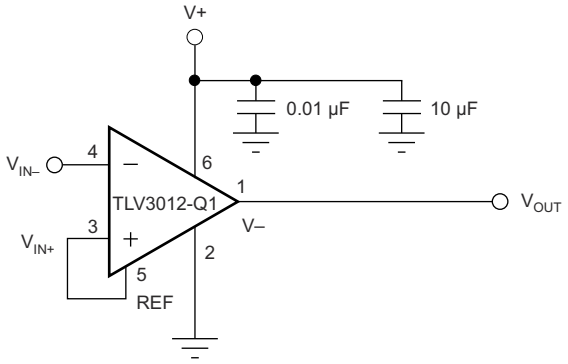


图 9-1. Basic Connections of the TLV3012-Q1

9.1.1 External Hysteresis

Comparator inputs have no noise immunity within the range of specified offset voltage (±12 mV). For noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. The typical comparator threshold of the TLV3012-Q1 device is ±0.5 mV. To prevent multiple switching within the comparator threshold of the TLV3012-Q1 device, external hysteresis may be added by connecting a small amount of feedback to the positive input. 图 9-2 shows a typical topology used to introduce hysteresis, described by 方程式 1.

$$V_{HYST} = \frac{V+ \times R1}{R1 + R2} \quad (1)$$

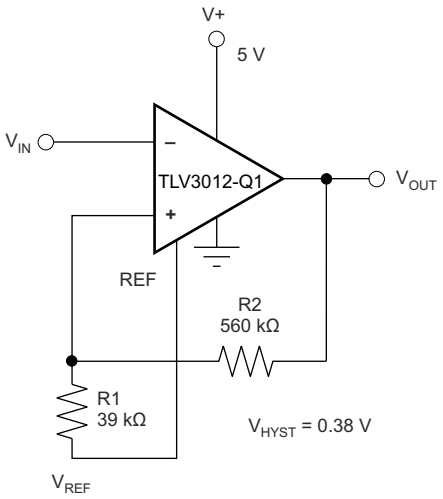


图 9-2. Adding Hysteresis

The V_{HYST} voltage sets the value of the transition voltage required to switch the comparator output by increasing the threshold region, thereby reducing sensitivity to noise.

9.2 Typical Application

9.2.1 Under-Voltage Detection

Under-voltage detection is frequently required to alert the system that a battery voltage has dropped below the usable voltage level. Figure 23 shows a simple under-voltage detection circuit using the TLV3012-Q1 which is configured as a non-inverting comparator with the integrated 1.242 V reference is externally connected to the inverting input pin (IN-).

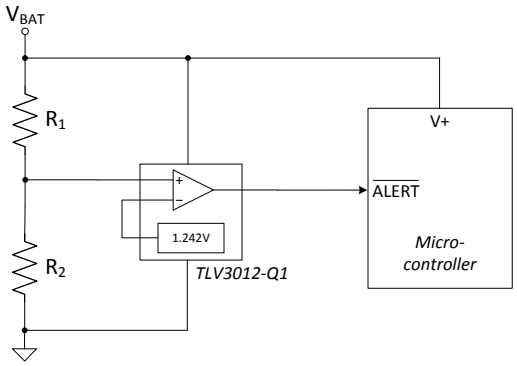


图 9-3. Under-Voltage Detection

9.2.1.1 Design Requirements

For this design, follow these design requirements:

- Operate from power supply that powers the microcontroller.
- Under-voltage alert is active low.
- Logic low output when V_{BAT} is less than 2.0V.

9.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 图 9-3. Connect (V+) to V_{BAT} which also powers the microcontroller. Resistors R_1 and R_2 create the under-voltage alert level of 2.0 V. When the battery voltage sags down to 2.0 V, the resistor divider voltage crosses V_{REF}, the 1.242 V reference threshold of the TLV3012-Q1. This causes the comparator

output to transition from a logic high to a logic low. The push-pull output of the TLV3012-Q1 is selected since the comparator operating voltage is shared with the microcontroller which is receiving the under-voltage alert signal.

方程式 2 is derived from the analysis of 图 9-3.

$$V_{REF} = \frac{R_2}{R_1 + R_2} \times V_{BAT} \tag{2}$$

where

- R_1 and R_2 are the resistor values for the resistor divider connected to IN+
- V_{BAT} is the voltage source that is being monitored for an undervoltage condition.
- V_{REF} is the falling edge threshold where the comparator output changes state from high to low

Rearranging 方程式 2 and solving for R_1 yields 方程式 3.

$$R_1 = \frac{(V_{BAT} - V_{REF})}{V_{REF}} \times R_2 \tag{3}$$

For the specific undervoltage detection of 2.0 V using the TLV3012-Q1, the following results are calculated.

$$R_1 = \frac{(2.0 - 1.242)}{1.242} \times 1M = 610\ k\Omega \tag{4}$$

where

- R_2 is set to 1 MΩ
- V_{BAT} is set to 2.0 V
- V_{REF} is set to1.242 V

Choose R_{TOTAL} (R_1 + R_2) such that the current through the divider is at least 100 times higher than the input bias current (I_{BIAS}). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

9.2.1.3 Application Curve

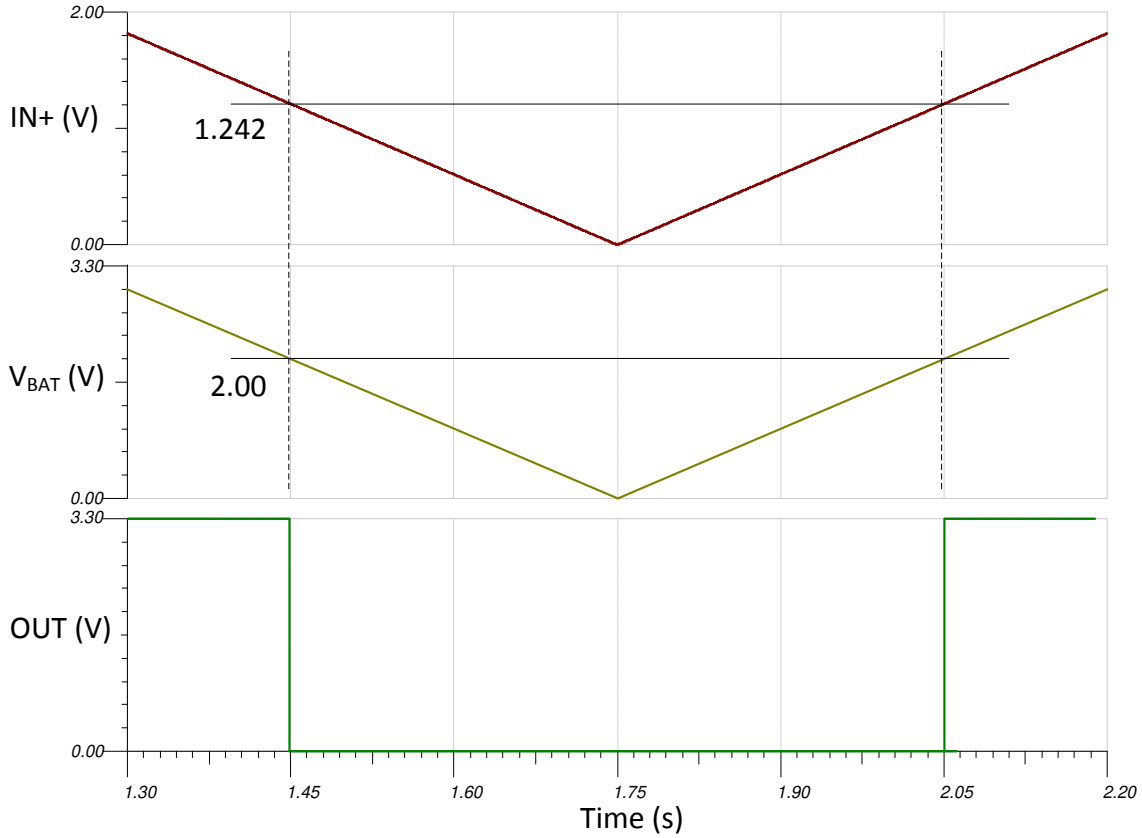


图 9-4.

9.3 System Examples

9.3.1 Power-On Reset

The reset circuit shown in 图 9-5 provides a time-delayed release of reset to the MSP430™ microcontroller. Operation of the circuit is based on a stabilization time constant of the supply voltage, rather than on a predetermined voltage value. The negative input is a reference voltage created by the internal voltage reference. The positive input is an RC circuit that provides a power-up delay. When power is applied, the output of the comparator is low, holding the processor in the reset condition. Only after allowing time for the supply voltage to stabilize does the positive input of the comparator become higher than the negative input, resulting in a high output state, releasing the processor for operation. The stabilization time required for the supply voltage is adjustable by the selection of the RC component values. Use of a lower-valued resistor in this portion of the circuit does not increase current consumption, because no current flows through the RC circuit after the supply has stabilized.

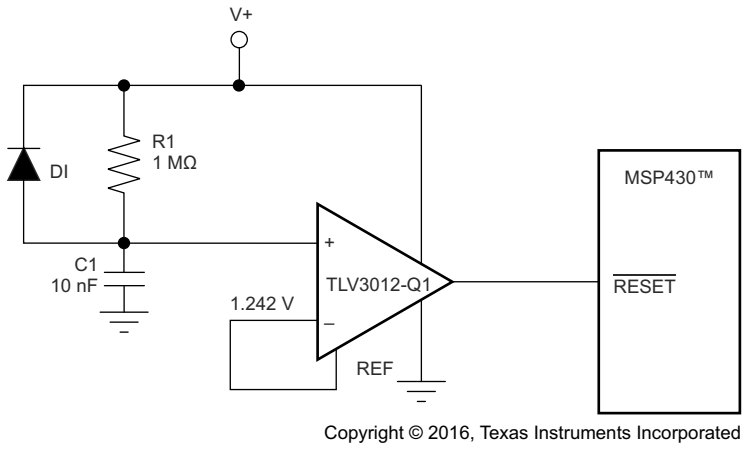


图 9-5. TLV3012-Q1 Configured as Power-Up Reset Circuit for the MSP430™ Microcontroller

The reset delay needed depends on the power-up characteristics of the system power supply. R_1 and C_1 are selected to allow enough time for the power supply to stabilize. D_1 provides rapid reset if power is lost. In this example, the $R_1 \times C_1$ time constant is 10 ms.

9.3.2 Relaxation Oscillator

The TLV3012-Q1 device can be configured as a relaxation oscillator to provide a simple and inexpensive clock output (see 图 9-6). The capacitor is charged at a rate of T = 0.69RC and discharges at a rate of 0.69RC. Therefore, the period is T = 1.38RC. R_1 may be a different value than R_2.

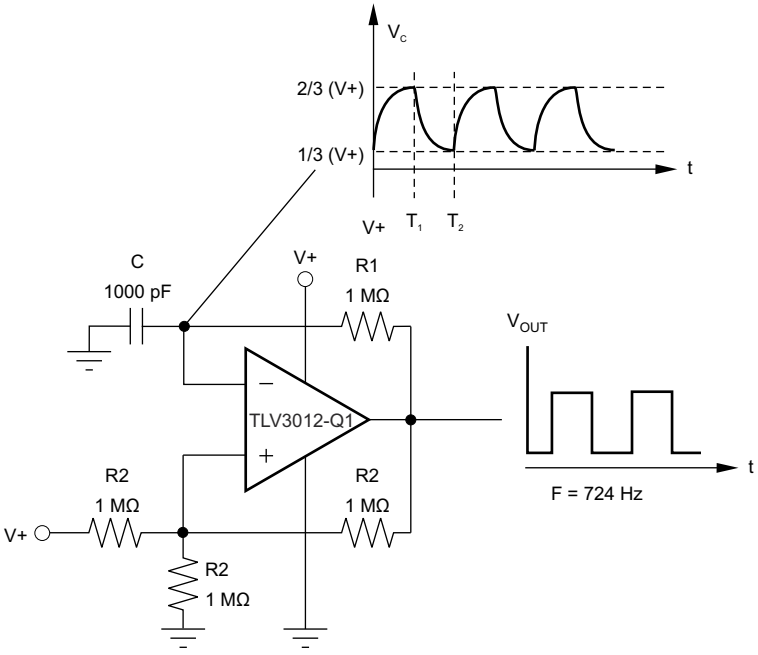


图 9-6. TLV3012-Q1 Configured as Relaxation Oscillator

9.4 Power Supply Recommendations

The TLV3012-Q1 has a recommended operating voltage range (V_S) of 1.8 V to 5.5 V. V_S is defined as (V+) – (V-). Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and – 2.5 V create comparable operating voltages for V_S. However, when bipolar supply voltages are used, it is important to realize that the reference

(REF) and logic low level of the comparator output is referenced to (V-). Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current in the EC Table.

9.5 Layout

9.5.1 Layout Guidelines

To minimize supply noise, power supplies should be capacitively decoupled by a 0.1-μF ceramic capacitor. Comparators are sensitive to input noise and precautions such as proper grounding (use of ground plane), supply bypassing, and guarding of high-impedance nodes minimize the effects of noise and help to ensure specified performance.

9.5.2 Layout Example

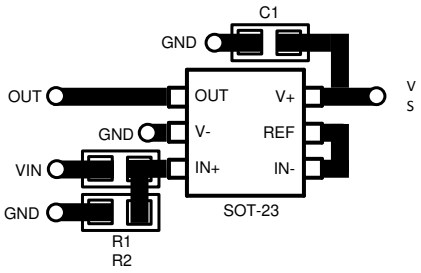


图 9-7. Layout Example

10 Device and Documentation Support

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

MSP430™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3011AQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2Q7F	Samples
TLV3011AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1M6	Samples
TLV3012AQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2Q8F	Samples
TLV3012AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3011-Q1, TLV3012-Q1 :

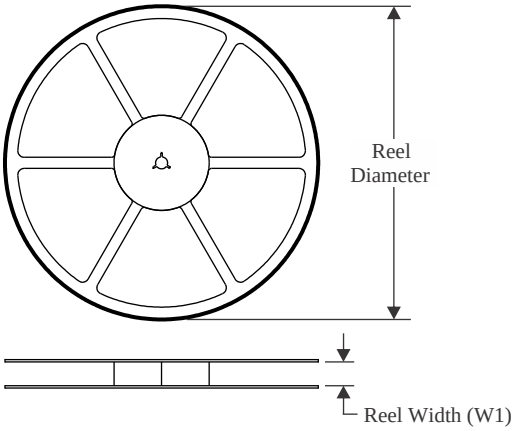
- Catalog : TLV3011, TLV3012
- Enhanced Product : TLV3011-EP

NOTE: Qualified Version Definitions:

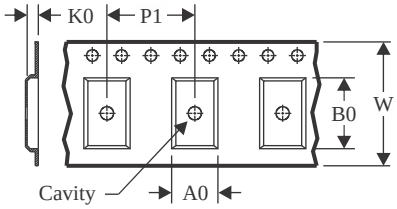
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

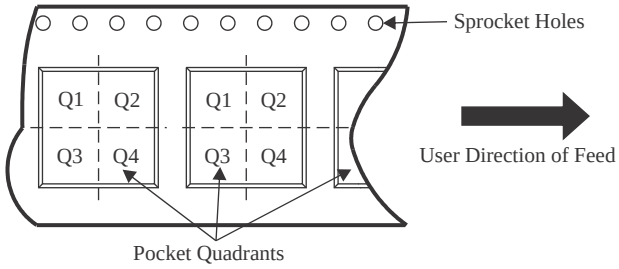


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

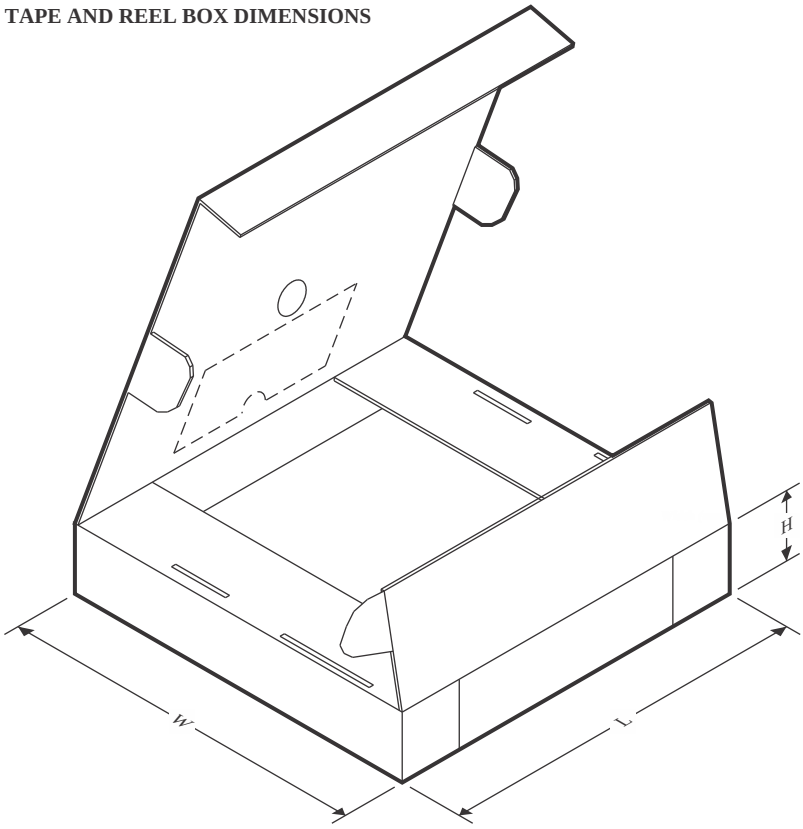
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3011AQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3012AQDCKRQ1	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

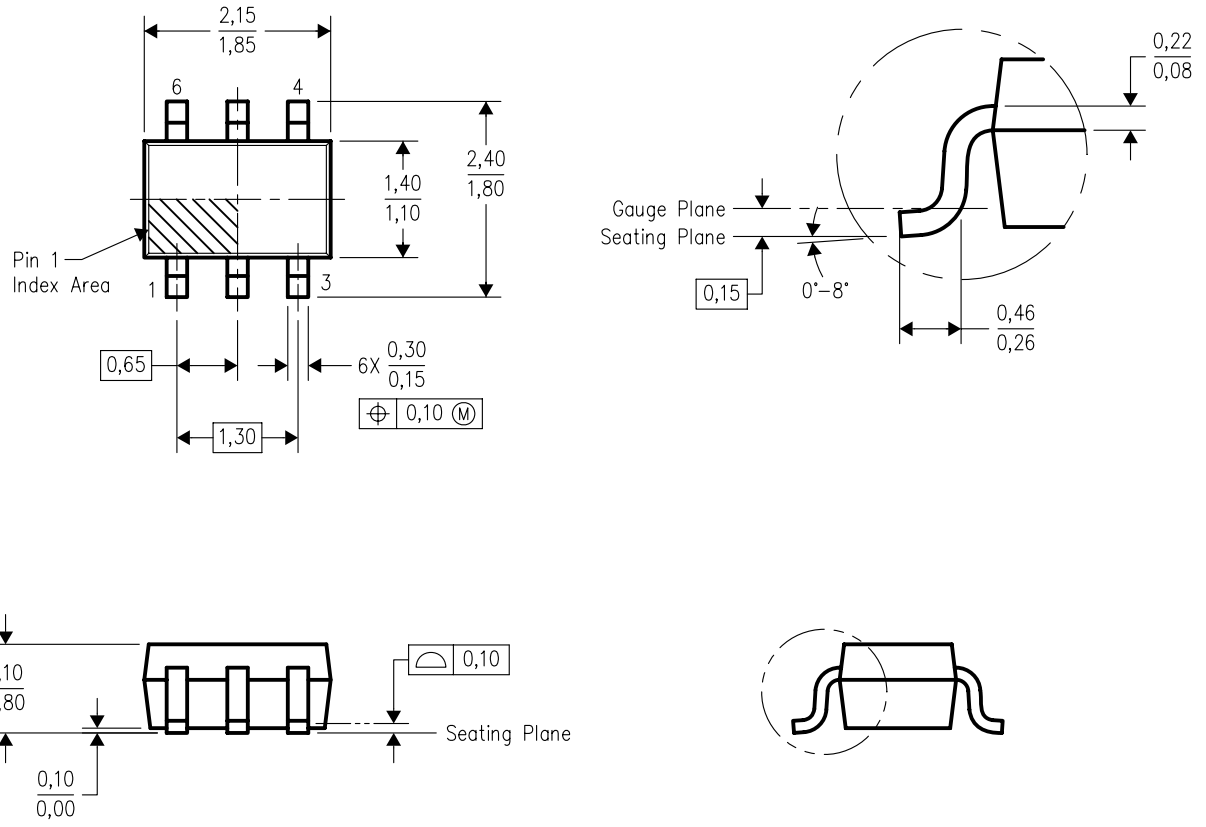
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3011AQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
TLV3012AQDCKRQ1	SC70	DCK	6	3000	200.0	183.0	25.0

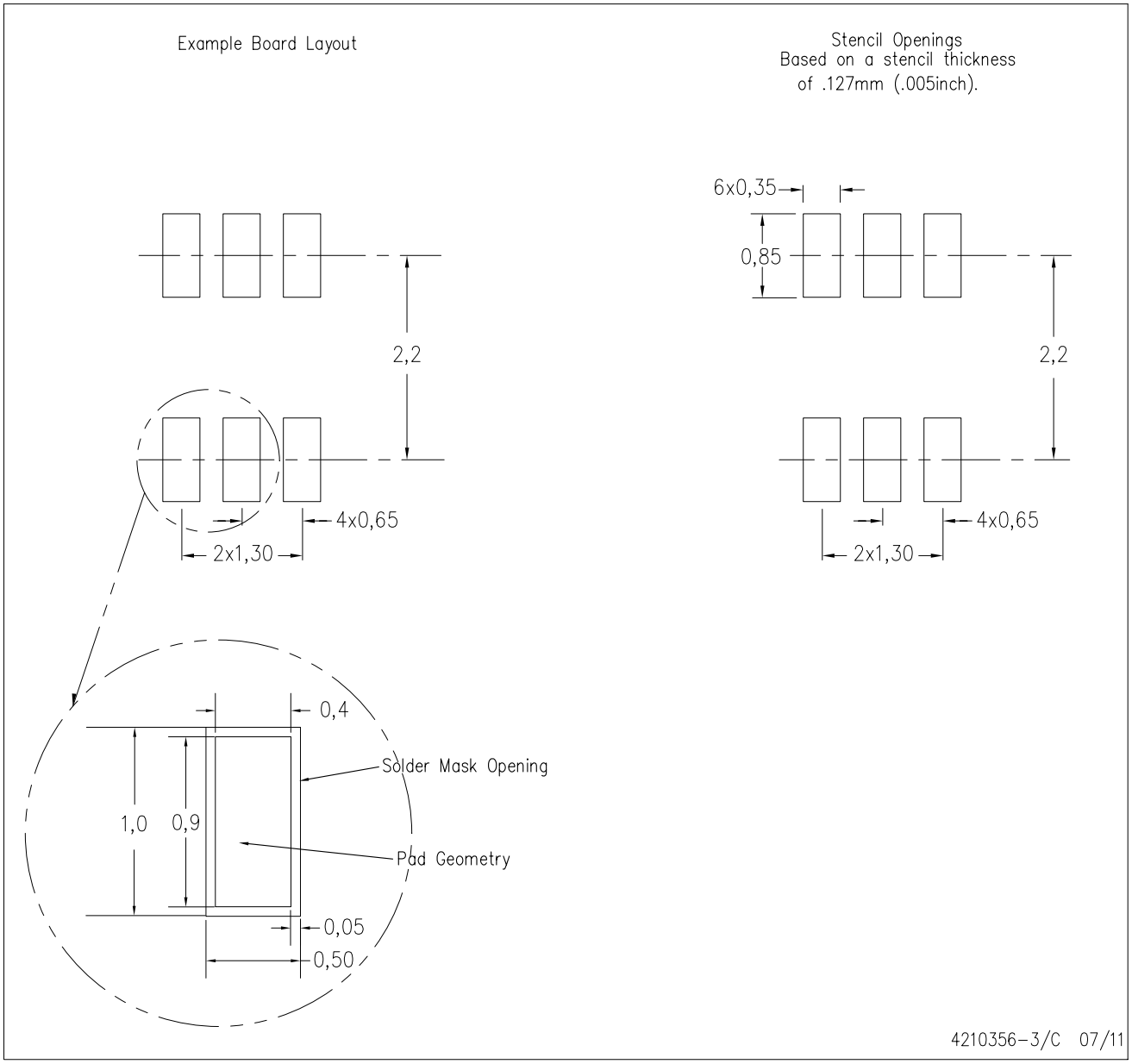
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



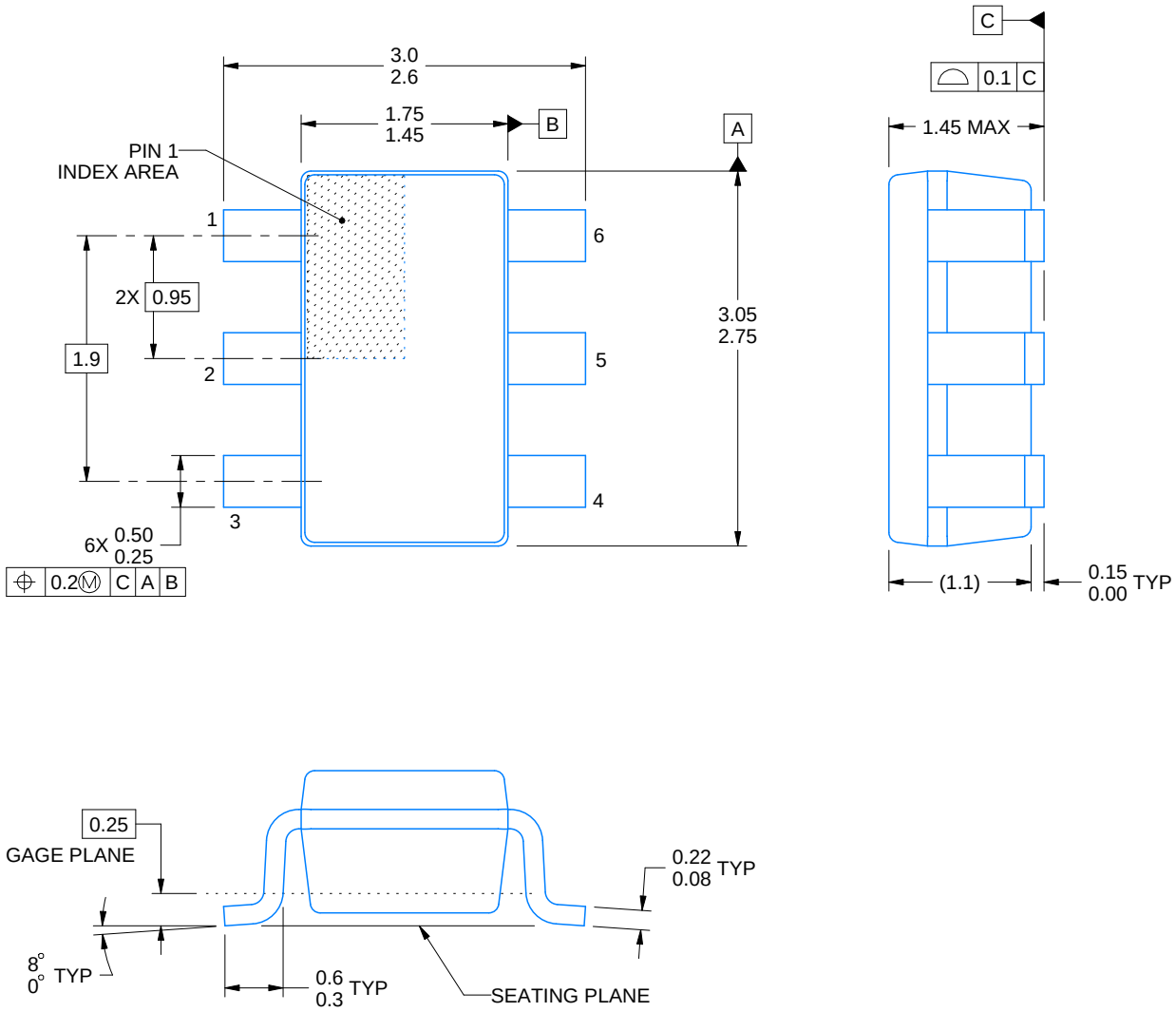
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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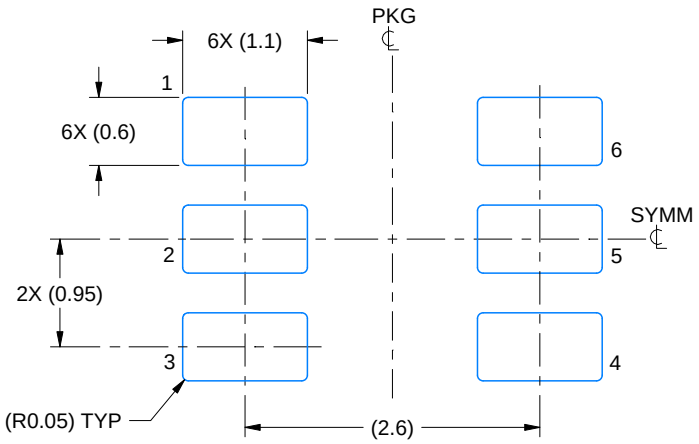
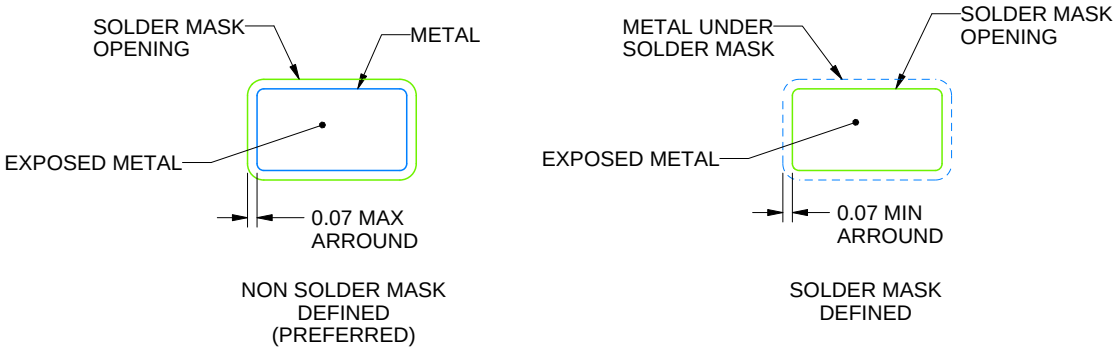
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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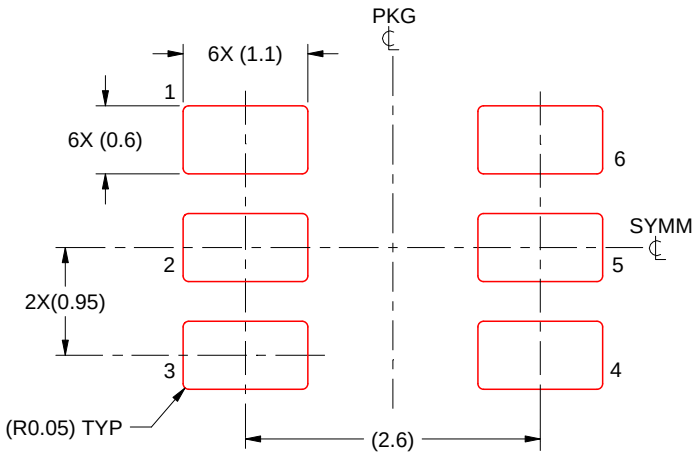
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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