CC2592 2.4GHz 范围扩展器

1 介绍

1.1 特性

- 与德州仪器 (TI) 2.4GHz 低功率 RF 器件的无缝对接
- +22dBm 输出功率
- CC2520，CC253X 和 CC85XX 上 3dB 典型经改进灵敏度
- 极少的外部组件
  - 集成开关
  - 集成匹配网络
  - 集成不平衡变压器
  - 集成电感器
  - 集成功率放大器 (PA)
  - 集成低噪声放大器 (LNA)
- 通过 HGM 端子的 LNA 增益数字控制
- 断电时 (LNA_EN = PA_EN = 0)，电流 100nA
- 低发送流耗
  - 对于 +22dBm，PAE = 34%，电压 3V 时的电流为 155mA
- 低接收流耗
  - 针对高增益模式的 4.0mA 电流
  - 针对低增益模式的 1.9mA 电流
- 4.7dB LNA 噪声系数，其中包括传输/接收 (T/R) 开关和外部天线
- 符合 RoHS 环保标准的 4mm x 4mm 四方扁平无引线 (QFN)-16 封装
- 2.0V 至 3.7V 工作电压
- -40°C 至 +125°C 运行温度范围

1.2 应用范围

- 所有 2.4GHz 工业、科学及医疗设备 (ISM) 频带系统
- 无线传感器网络
- 无线工业系统
- IEEE 802.15.4 和 ZigBee® 计量系统
- IEEE 802.15.4 和 ZigBee 网关
- 无线消费类电子系统
- 无线音频系统

1.3 说明

CC2592 器件是一款针对低功率和低压 2.4GHz 无线应用的经济高效且高性能的 RF 前端。

CC2592 器件是一款针对德州仪器 (TI) 所有 CC25XX 2.4GHz 低功率 RF 收发器、发射器和片上系统产品的范围扩展器。

为了增加链路预算，CC2592 器件提供一个可增加输出功率的功率放大器，以及一个具有低噪声系数的 LNA，以提升接收器灵敏度。

CC2592 器件提供一个极小尺寸，高输出功率 RF 设计，此设计采用 4mm x 4mm 四方扁平无引线 (QFN)-16 封装。

CC2592 器件包含高性能无线应用简单设计所需的 PA，LNA，开关，RF 匹配和不平衡变压器。

1.4 功能方框图

图 1-1 显示了 CC2592 器件的简化方框图。

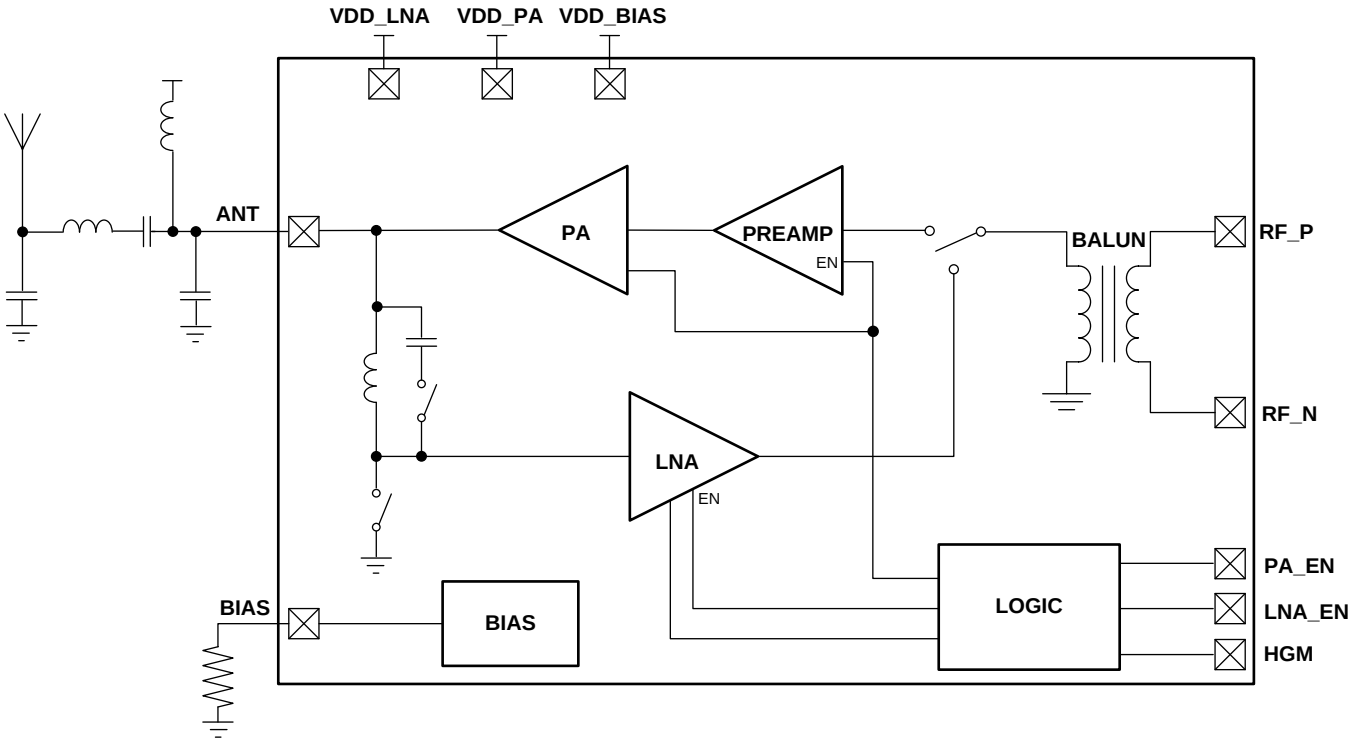


图 **1-1. CC2592** 简化方框图

修订历史记录

日期	文献编号	更改
2014 年 2 月	SWRS159	最初发布版本

2 Device Characteristics

2.1 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Conditions	Value	Unit
Supply voltage	All supply terminals must have the same voltage	–0.3 to 3.8	V
Voltage on any digital terminal		–0.3 to VDD+0.3, max 3.8	V
Input RF level		+10	dBm

2.2 Handling Ratings

Under no circumstances must the handling ratings be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Conditions	Value	Unit
Storage temperature range		–50 to 150	°C
ESD	Human Body Model	2000	V
	Charge Device Model	1000	V

2.3 Recommended Operating Conditions

The operating conditions for the CC2592 device are listed below.

Parameter	Conditions	Min	Max	Unit
Ambient temperature range		–40	125	°C
Operating supply voltage		2.0	3.7	V
Operating frequency range		2400	2483.5	MHz

2.4 Electrical Characteristics

T_c = 25°C, VDD = 3.0 V, f_{RF} = 2440 MHz (unless otherwise noted). Measured on CC2592EM reference design including external matching components.

Parameter	Test Conditions	Min	Typ	Max	Unit
Receive current, high-gain mode	HGM = 1		4		mA
Receive current, low-gain mode	HGM = 0		1.9		mA
Transmit current	P_{OUT} = 20 dBm		123		mA
	P_{OUT} = 22 dBm		155		
Transmit current	No input signal		50		mA
Power down current	EN = 0		0.1	0.3	µA
High-input level (control terminals)	PA_EN, LNA_EN, HGM	1.3		Vdd	V
Low-input level (control terminals)	PA_EN, LNA_EN, HGM			0.3	V
Power down - Receive mode switching time			1		µs
Power down - Transmit mode switching time			1		µs
RF Receive					
Gain, high-gain mode	HGM = 1		11		dB
Gain, low-gain mode	HGM = 0		6		dB
Gain variation over frequency	2400 to 2483.5 MHz, HGM = 1		2		dB
Gain variation over power supply	2.0 V to 3.7 V, HGM = 1		1.5		dB
Gain variation over temperature	–40°C to 85°C, HGM = 1		1.7		dB
Gain variation over temperature	85°C to 125°C, HGM = 1		1		dB
Noise figure, high-gain mode	HGM = 1, including internal T/R switch and external antenna match		4.7		dB
Input 1-dB compression, high-gain mode	HGM = 1		–18		dBm
Input IP3, high-gain mode	HGM = 1		–9		dBm
Input reflection coefficient, S11	HGM = 1, measured at antenna port		–15		dB
RF Transmit					
Gain			24		dB
Output power, P_{OUT}	P_{IN} = 0.0 dBm		20.3		dBm
	P_{IN} = 4.0 dBm		21.9		
Power added efficiency, PAE	P_{OUT} = 22 dBm		34		%
Output 1-dB compression			15		dBm
Output power variation over frequency	2400 to 2483.5 MHz, P_{IN} = 4 dBm		0.5		dB
Output power variation over power supply	2.0 V to 3.7 V, P_{IN} = 4 dBm		3.8		dB
Output power variation over temperature	–40°C to 125°C, P_{IN} = 4 dBm		1.7		dB
Second harmonic power	FCC requirement			–41.2	dBm
Third harmonic power	FCC requirement			–41.2	dBm
VSWR	No damage	20:1			
	Stability	7.5:1			

3 Device Information

3.1 Terminal and I/O Configuration

Figure 3-1 and Table 3-1, provide the terminal layout and description for the CC2592 device.

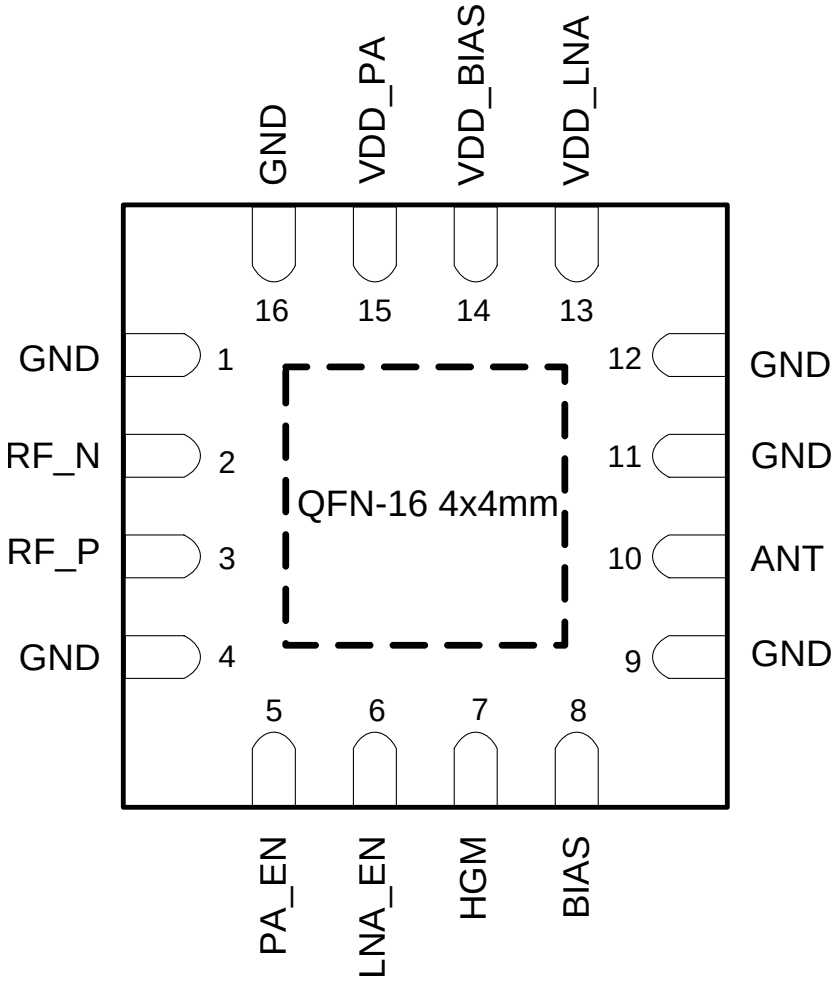


Figure 3-1. Terminal Top View

Table 3-1. Terminal Functions

Terminal		Type	Description
No.	Name		
–	GND	Ground	The exposed die attach pad must be connected to a solid ground plane. See CC2592EM reference design for the recommended layout.
1, 4, 9, 11, 12, 16	GND	Ground	Ground connections. Only terminals 9, 11, and 12 should be shorted to the die attach pad on the top PCB layer.
2	RF_N	RF	RF interface toward CC25xx device
3	RF_P	RF	RF interface toward CC25xx device
5	PA_EN	Digital input	Digital control terminal. See Table 9-1 for details.
6	LNA_EN	Digital input	Digital control terminal. See Table 9-1 or details.
7	HGM	Digital input	Digital control terminal HGM = 1 → Device in High Gain Mode HGM = 0 → Device in Low Gain Mode
8	BIAS	Analog	Biasing input. Resistor between this node and ground sets bias current for PA and LNA.
10	ANT	RF	Antenna interface
13	VDD_LNA	Power	2.0- to 3.7-V power
14	VDD_BIAS	Power	2.0- to 3.7-V power
15	VDD_PA	Power	2.0- to 3.7-V power

4 Sensitivity Improvement Example

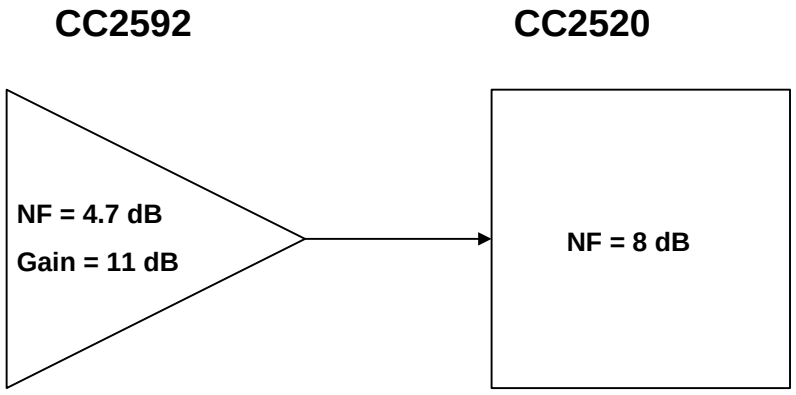


Figure 4-1.

The noise factor of a system consisting of the CC2592 device and a CC2520 device, as seen in Figure 4-1 is given by:

$$F = F_1 + \frac{F_2 - 1}{G_1} = 10^{\frac{4.7}{10}} + \frac{10^{\frac{8}{10}} - 1}{10^{\frac{11}{10}}} = 3.37 \quad (1)$$

The noise figure is:

$$NF = 10\log(F) = 10\log(3.37) = 5.28 \text{ dB} \quad (2)$$

The noise figure is reduced from 8 dB for the CC2520 standalone to 5.28 dB for the CC2592 and CC2520 device combination, leading to a 2.72-dB theoretical improvement in sensitivity.

In practice, tests on the CC2592 and CC25XX devices show around 3-dB improvement in sensitivity. For the CC2538 and CC2592 devices, the improvement is almost 4 dB (approximately –97 dBm to –101 dBm)

5 CC2592EM Evaluation Module

Figure 5-1 shows an evaluation module circuit of the CC2592 device.

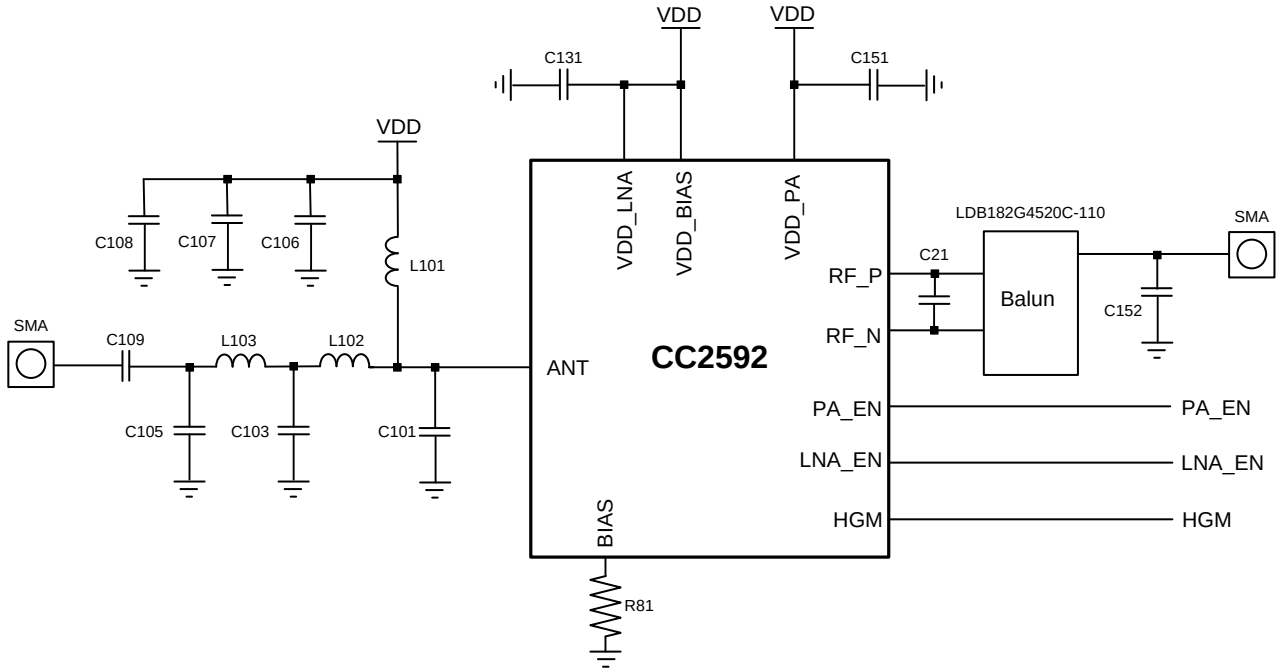


Figure 5-1. CC2592 Evaluation Module

Table 5-1 lists the materials in the CC2592 evaluation module circuit.

Table 5-1. List of Materials

Device	Function	Value
L101	PA bias inductor	4.7 nH, Multilayer chip inductor
L102	Part of antenna match	1 nH, Multilayer chip inductor
L103	Part of antenna match	1.8 nH, Multilayer chip inductor
C101	Part of antenna match	2.2-pF 0402 Chip capacitor
C103	Part of antenna match	2.2-pF 0402 Chip capacitor
C105	Part of antenna match	0.1-pF 0402 Chip capacitor
C106	Decoupling	12-pF 0402 Chip capacitor
C107	Decoupling	1-nF 0402 Chip capacitor
C108	Decoupling	1-µF 0402 Chip capacitor
C109	DC block	18-pF 0402 Chip capacitor
C21	Balun matching capacitor	0.2-pF 0402 Chip capacitor
C152	Balun matching capacitor	0.3-pF 0402 Chip capacitor
C131	Decoupling	1-nF 0402 Chip capacitor
C151	Decoupling	12-pF 0402 Chip capacitor
R81	Bias resistor	3.9 kΩ, 0402 resistor

6 Typical Characteristics

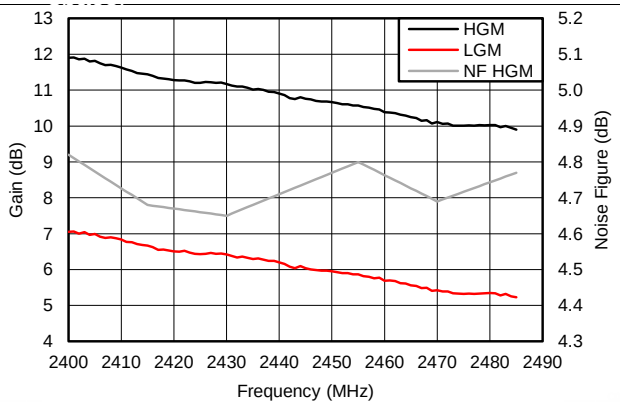


Figure 1. LNA Gain and Noise Figure Versus Frequency

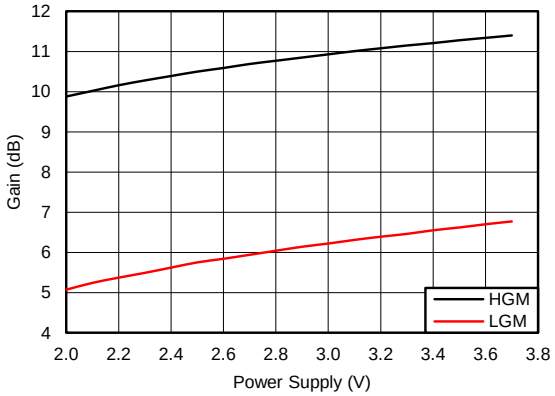


Figure 2. LNA Gain Versus Power Supply

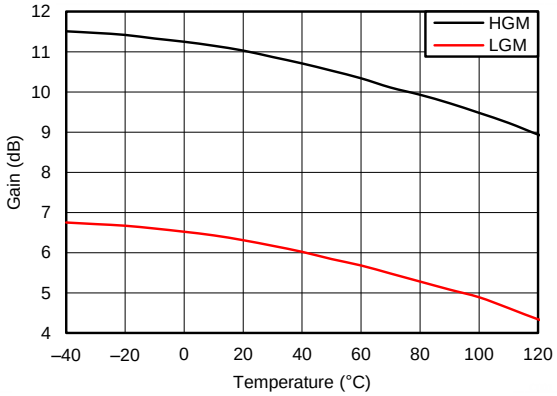


Figure 3. LNA Gain Versus Temperature

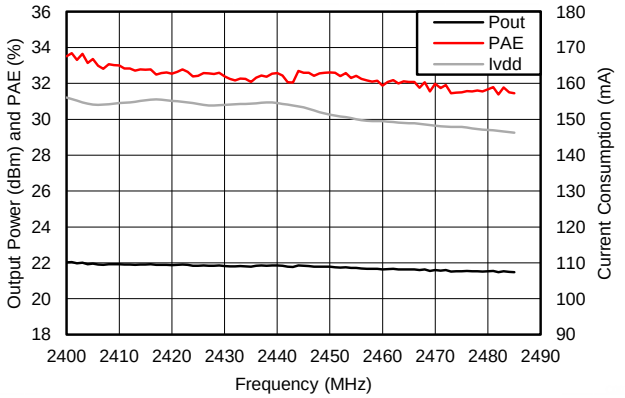


Figure 4. Output Power, PAE, and Current Consumption Versus Frequency
Input Power Level = +4 dBm

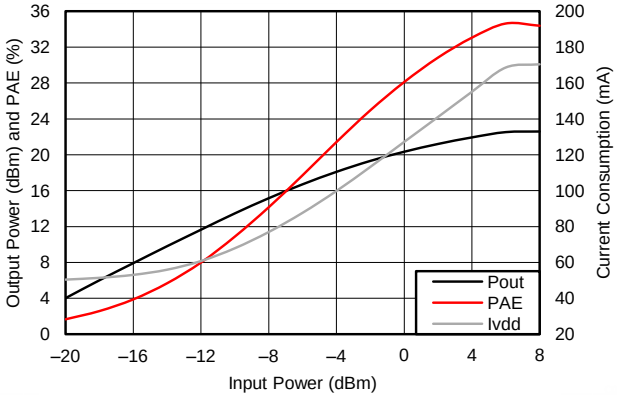


Figure 5. Output Power, PAE, and Current Consumption Versus Input Power

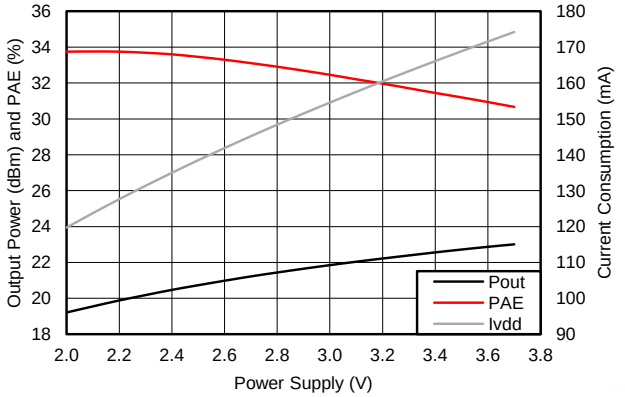


Figure 6. Output Power, PAE, and Current Consumption Versus Power Supply
Input Power Level = +4 dBm

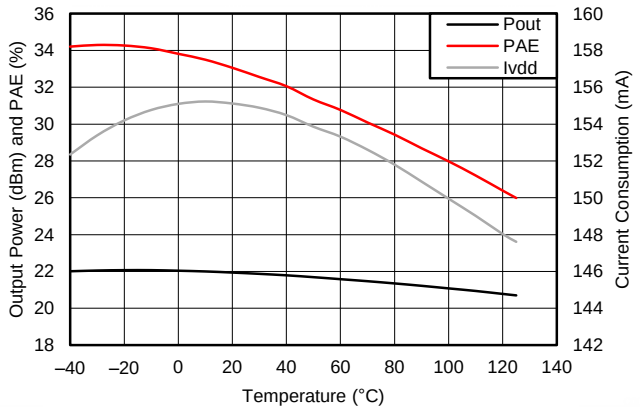


Figure 7. Output Power, PAE, and Current Consumption Versus Temperature Input Power Level = +4 dBm

7 Controlling the Output Power from CC2592

The output power of the CC2592 device is controlled by controlling the input power. The CC2592 PA is designed to work in compression (class AB).

Driving the CC2592 device too far into saturation might result in spurious emissions and harmonics above regulatory limits. This caution should especially be considered for systems targeting a wide operating temperature range, where a combination of low temperature, low supply voltage, and a transceiver that increases output power (drive level) at low temperature, can result in high spurious emissions.

Figure 7-1 shows the maximum recommended drive level versus temperature and supply voltage.

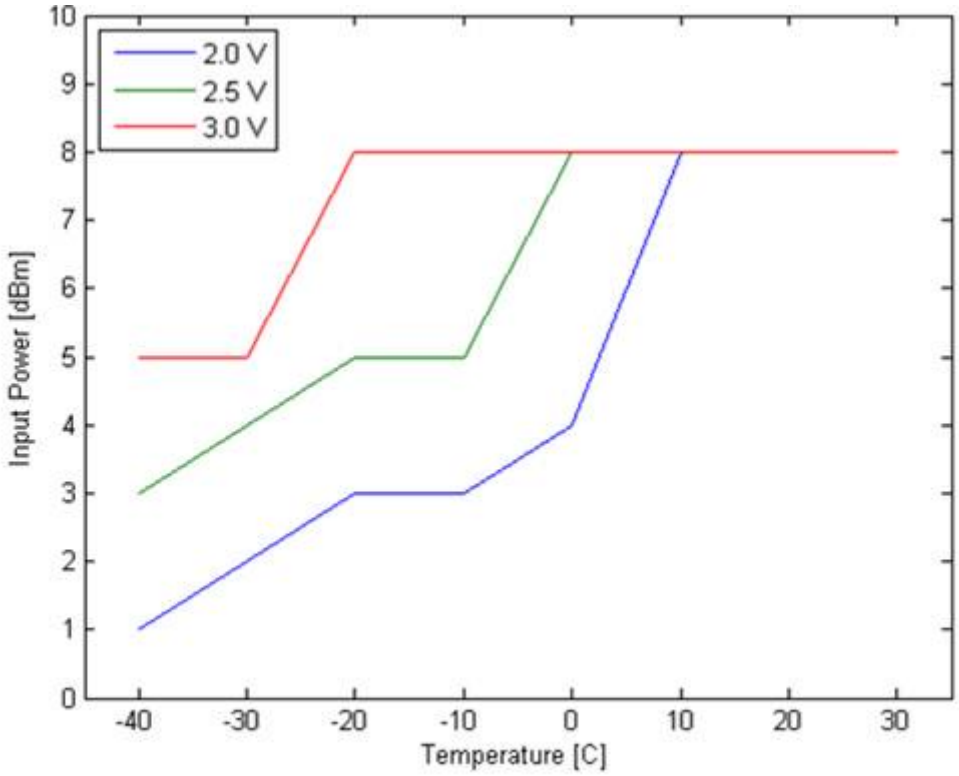


Figure 7-1. Maximum Recommended Drive Level

8 Input Levels on Control Terminals

The three digital control terminals (PA_EN, LNA_EN, and HGM) have built-in level-shifting functionality, meaning that if the CC2592 device operates off a 3.7-V supply voltage, the control terminals still sense 1.6- to 1.8-V signals as a logical 1. However, the input voltages should not have a logical 1 level that is higher than the supply.

9 Connecting the CC2592 Device to a CC25xx Device

Table 9-1 shows the control logic for connecting CC2592 to a CC25xx device.

Table 9-1. Control Logic for Connecting CC2592 to a CC25xx Device

PA_EN	LNA_EN	HGM	Mode of Operation
0	0	X	Power Down
X	1	0	RX Low-Gain Mode
X	1	1	RX High-Gain Mode
1	0	X	TX

Figure 9-1 shows the application circuit for the CC2592 and CC253X devices.

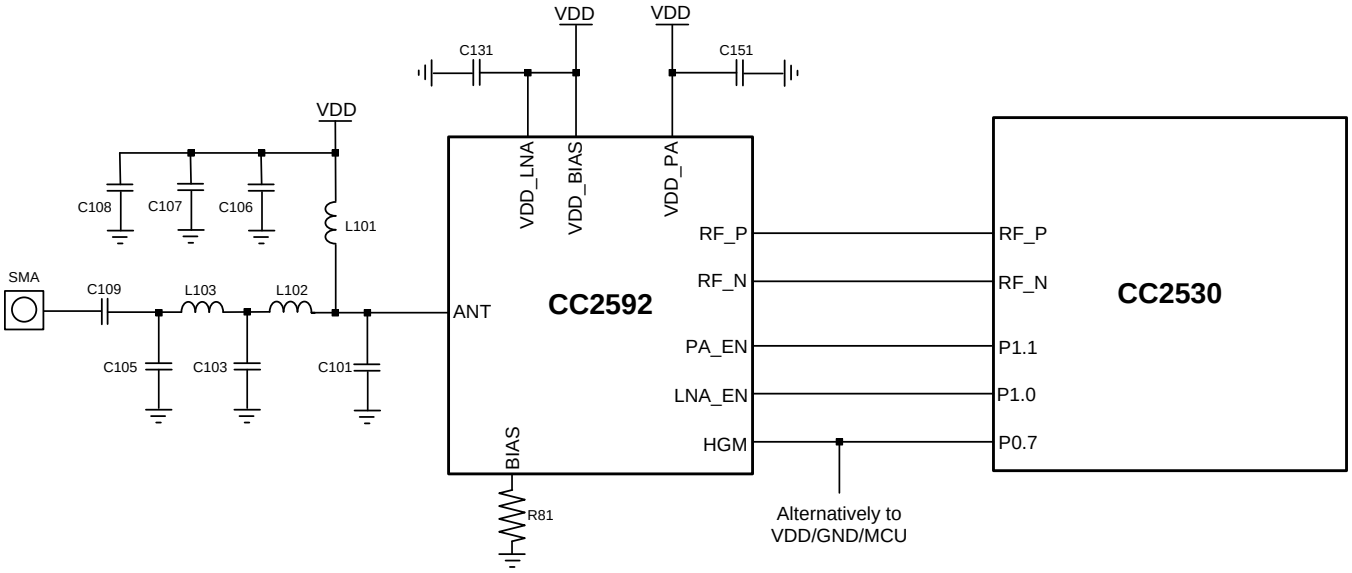


Figure 9-1. Application Circuit Example for CC2530 + CC2592

10 Device and Documentation Support

10.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CC2592	Click here	Click here	Click here	Click here	Click here

10.2 Trademarks

ZigBee is a registered trademark of ZigBee Alliance.

10.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2592RGVR	ACTIVE	VQFN	RGV	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CC2592	Samples
CC2592RGVT	ACTIVE	VQFN	RGV	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CC2592	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

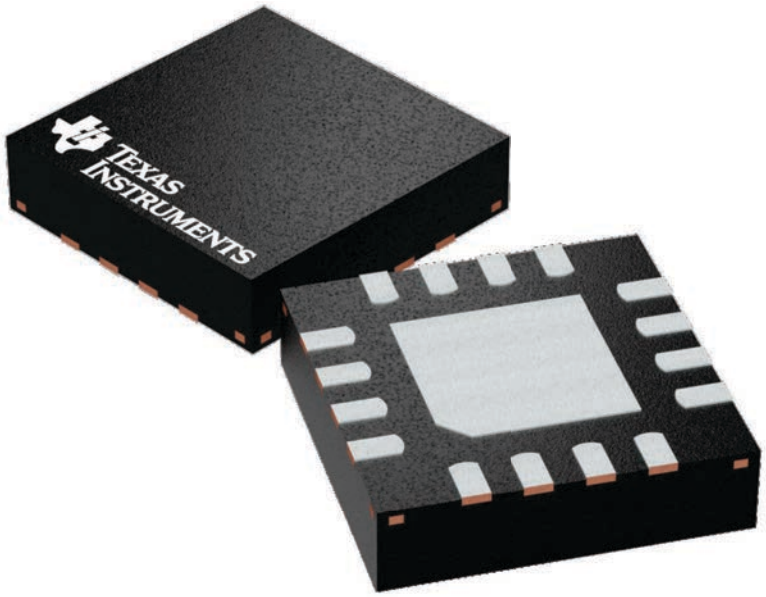
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

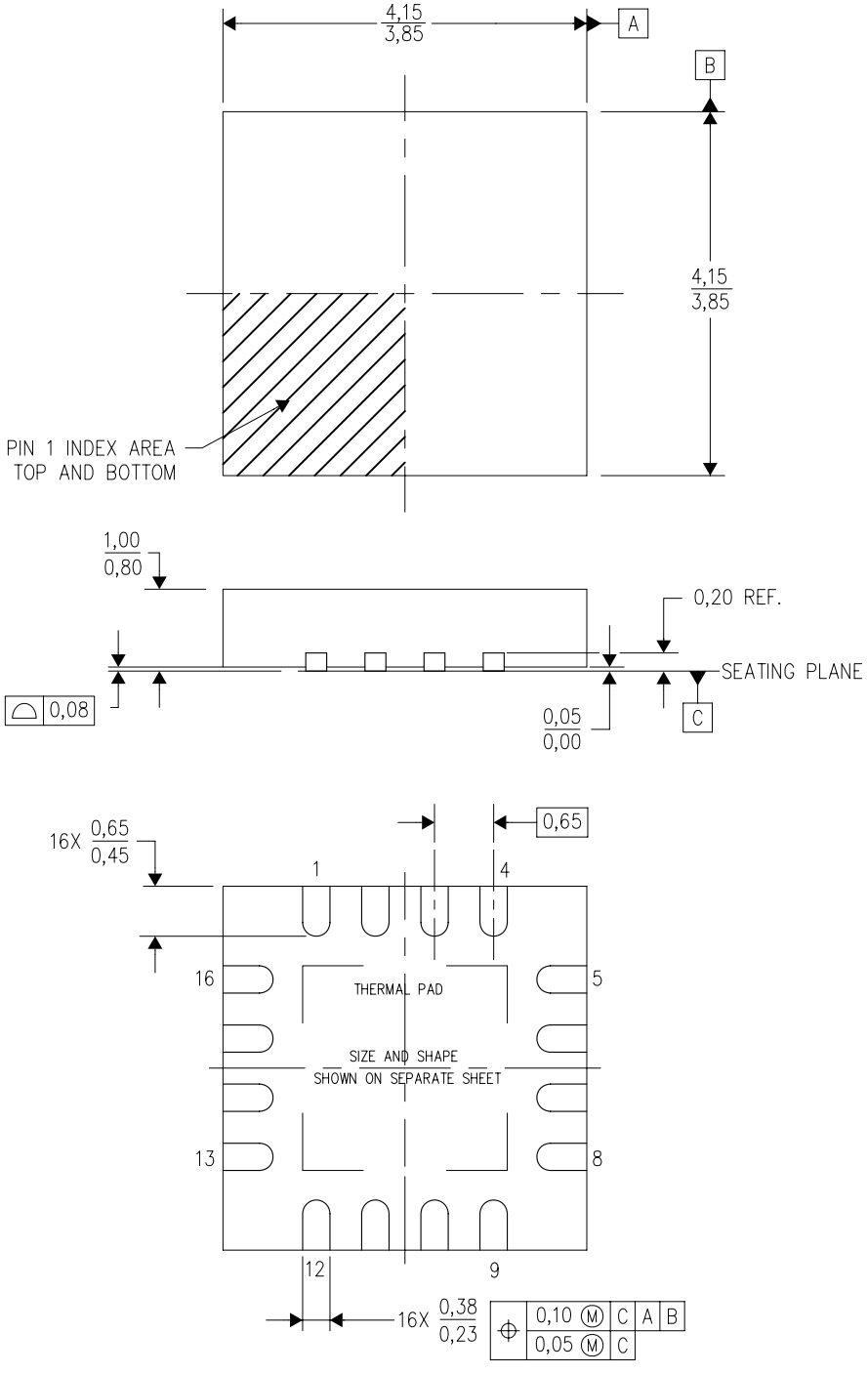
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224748/A

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

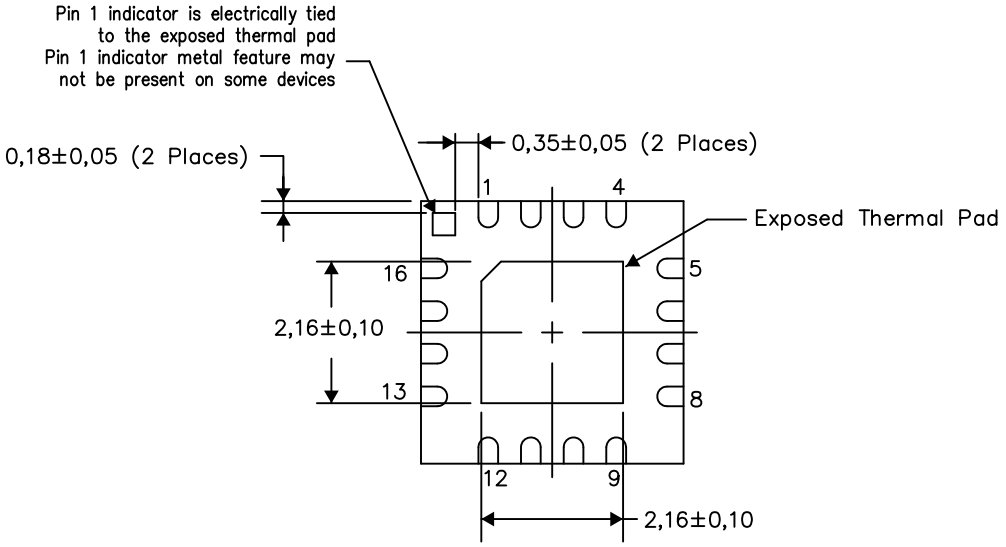
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



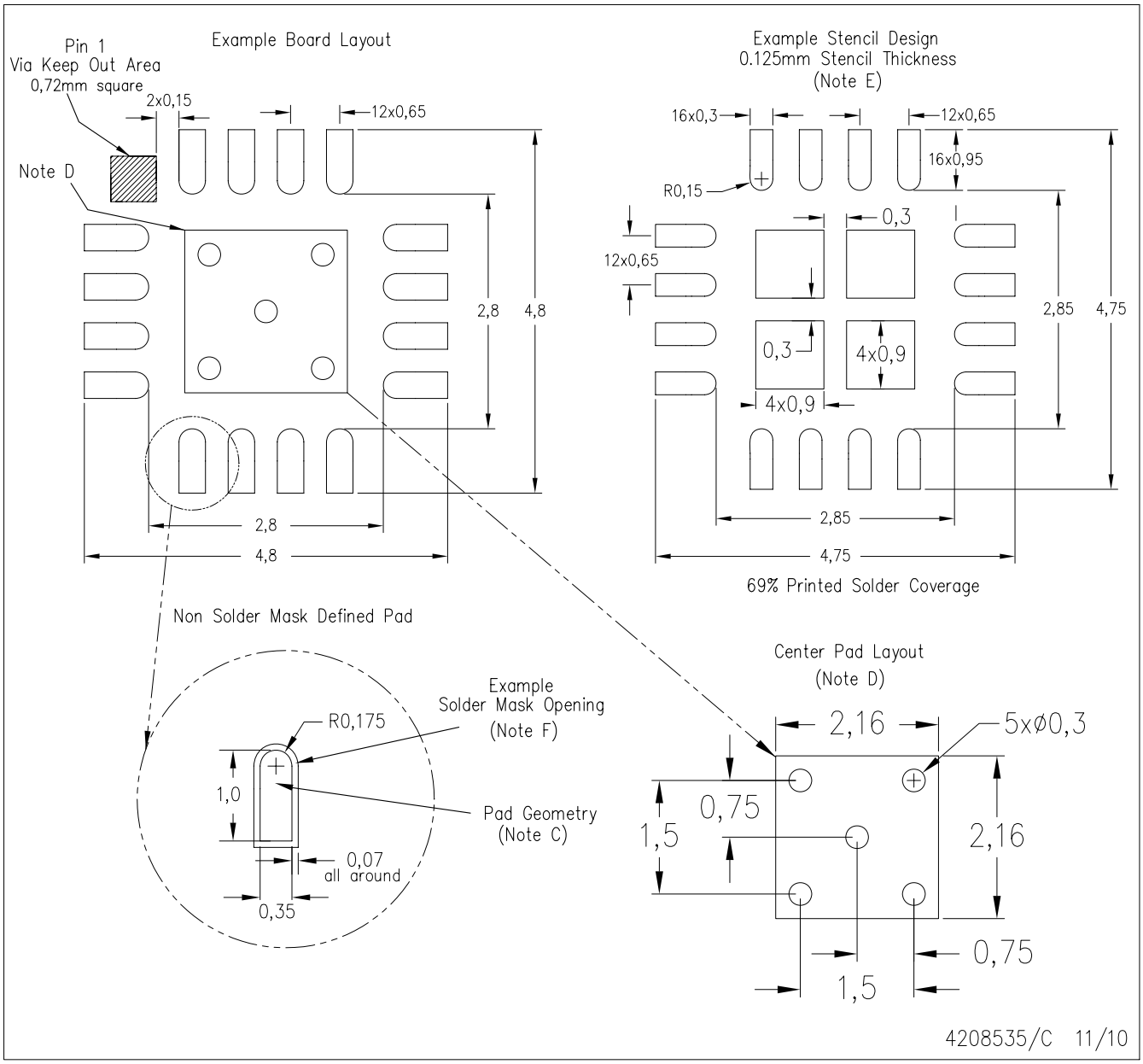
Bottom View

Exposed Thermal Pad Dimensions

4206351–2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



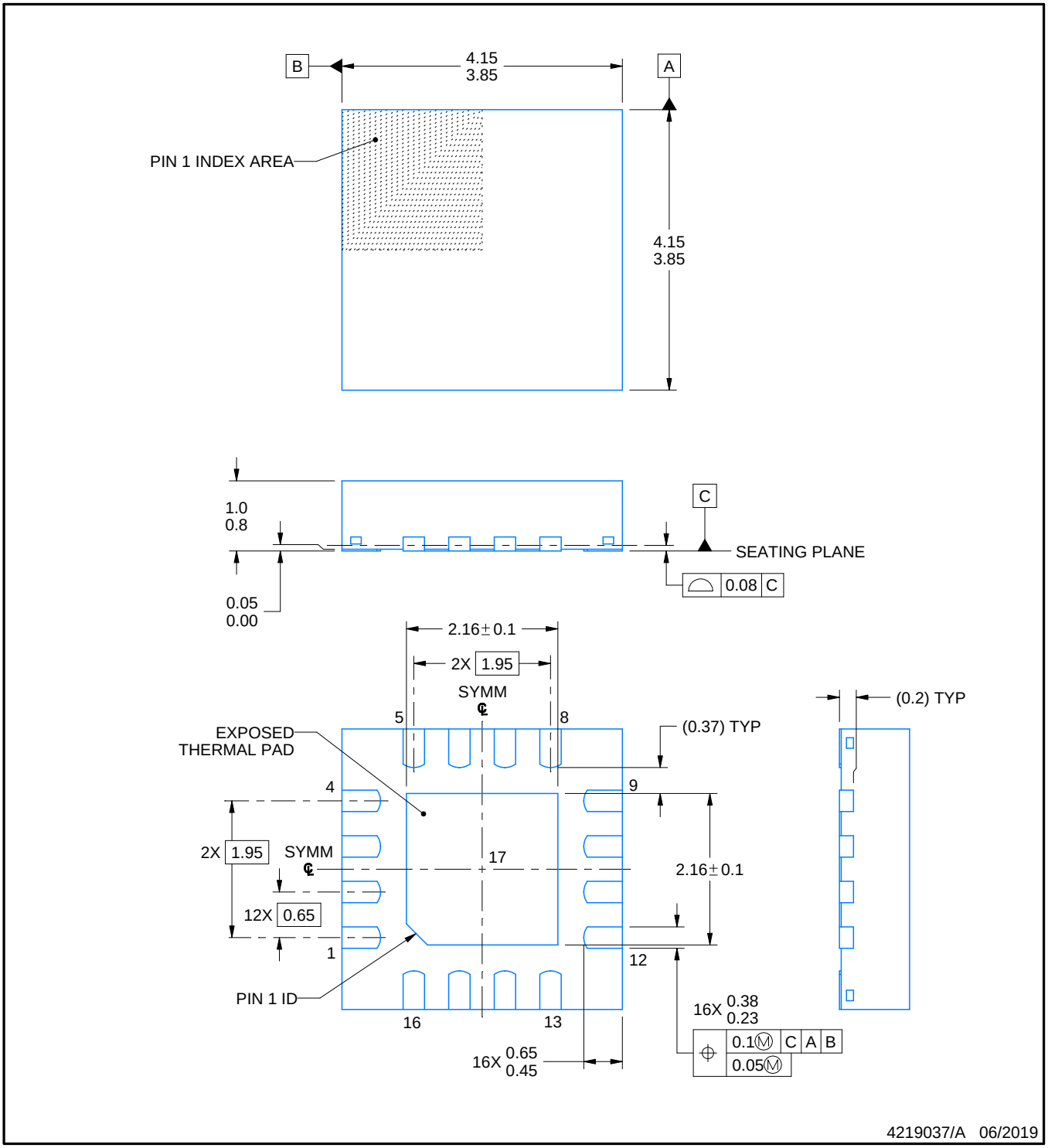
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

RGV0016A

PACKAGE OUTLINE

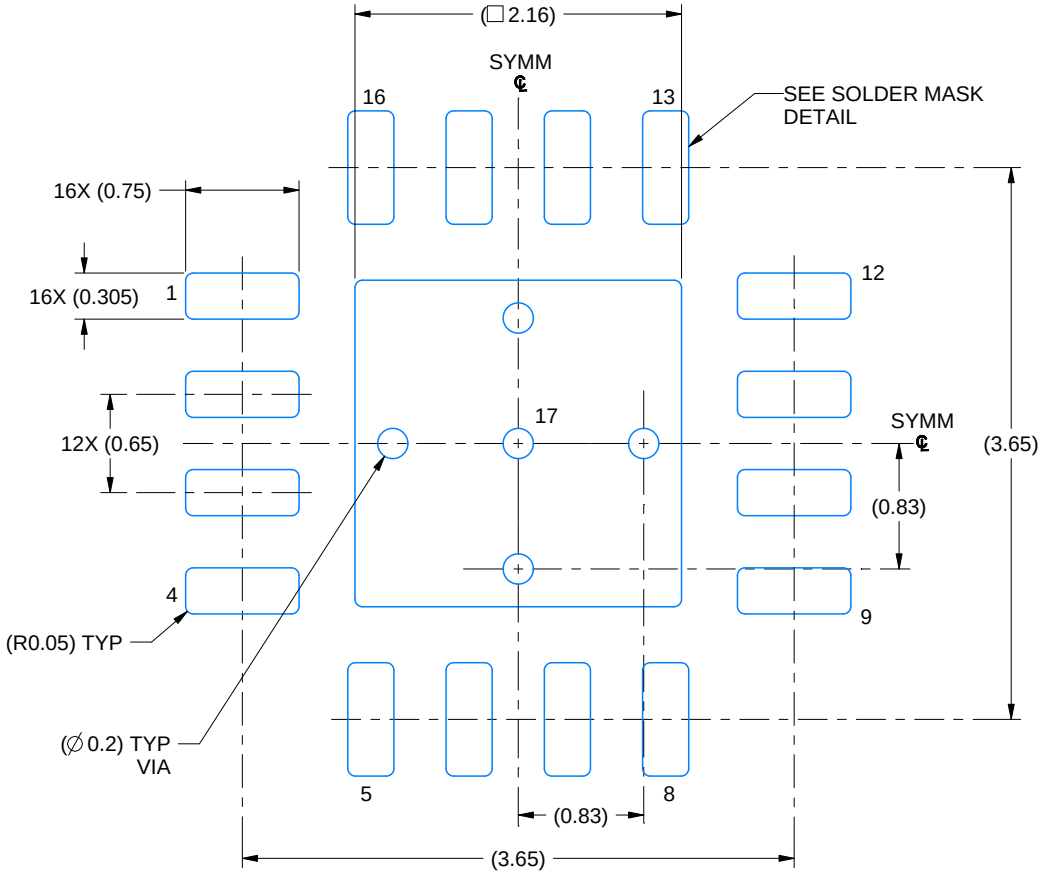
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

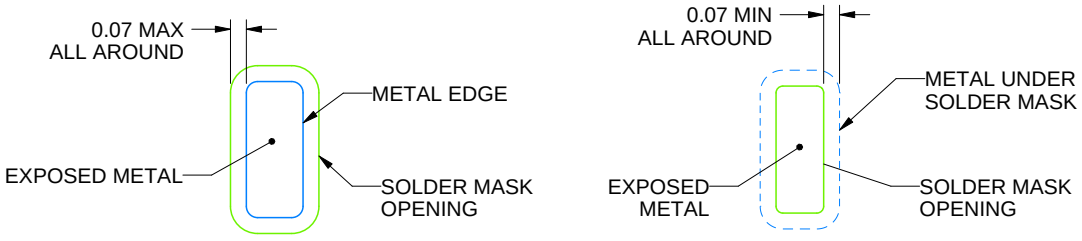


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

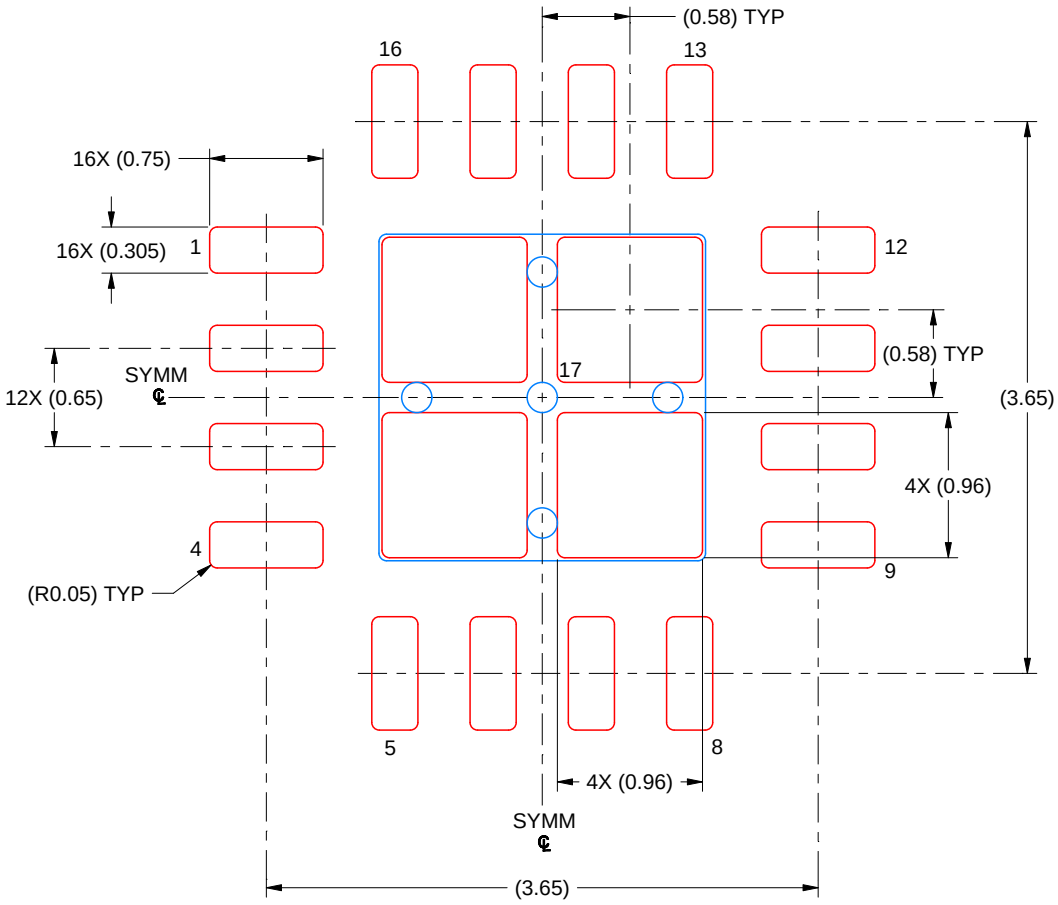
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219037/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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