TPS2375x 符合 IEEE 802.3at 标准的高效 PoE 接口和直流/直流控制器

1 特性

- 可为功率高达 30W 的（输入）受电设备供电
- 直流/直流控制，针对隔离式转换器进行了优化
- 支持高效拓扑结构
- 完整的 PoE 接口
- 符合 IEEE 802.3at 标准且具有状态标志的增强型分类
- 适配器 ORing 支持
- 可编程频率具有同步功能
- 稳定耐用的 100V，0.5Ω 热插拔金属氧化物半导体场效应晶体管 (MOSFET)
- -40°C 至 125°C 的工作结点温范围
- 行业标准 PowerPAD™HTSSOP-20

2 应用

- IEEE 802.3at 兼容器件
- 视频和网络语音 (VoIP) 电话
- RFID 阅读器
- 多频带访问点
- 监控摄像机

3 说明

TPS23754 和 TPS23756 器件具有合并的以太网供电 (PoE) 受电设备 (PD) 接口和电流模式直流/直流控制器（专门针对隔离式转换器进行了优化）。此 PoE 接口支持 IEEE 802.3at 标准。

TPS23754 和 TPS23756 支持多个输入电压 ORing 选项，其中包括最高电压、外部适配器首选项和 PoE 首选项。这些 特性 使得设计人员在任何情况下都能确定哪个电源承担负载。

PoE 接口 具有 与高功率中跨供电设备 (PSE) 兼容（符合 IEEE 802.3at 标准）所需的新扩展硬件分类。签名检测引脚也可被用来强制关闭 PoE 供电。使用一个单个电阻器可将分类设定为已定义类别中的任何一个。

该直流/直流控制器 采用 两个具有可编程死区时间的互补栅极驱动器。这简化了有源钳位正向转换器或优化的栅极驱动器设计，从而实现高效的反激式拓扑。如果只需单个 MOSFET 拓扑需要，则可以禁用第二个栅极驱动器。该控制器还 具有 内部软启动、自举启动电源、电流模式补偿以及 78% 最大占空比等特性。一个可编程和可同步振荡器可针对使用效率对设计进行优化并简化控制器的使用以升级现有的电源设计。具有一个缺省周期的精确可编程消隐简化了常见电流感测滤波器设计平衡。

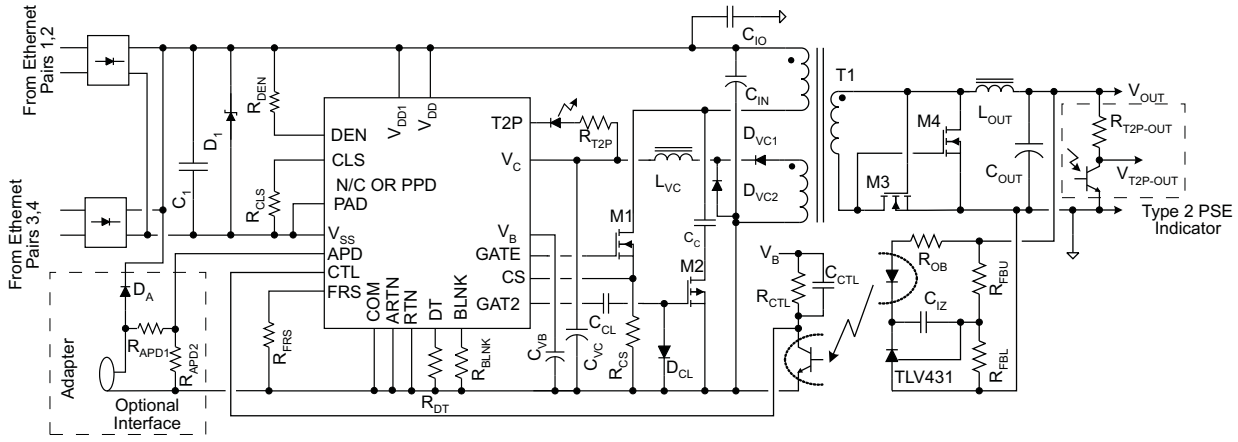
TPS23754 器件具有 15V 的转换器启动电压阈值，而 TPS23756 器件具有 9V 的转换器启动电压阈值。TPS23754-1 使用 no-connect（不连接）连接状态取代了 PPD 引脚，从而增大引脚间距。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS23754	HTSSOP (20)	6.50mm x 4.40mm
TPS23754-1		
TPS23756		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

使用 **TPS23754** 的高效转换器



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision H (September 2015) to Revision I **Page**

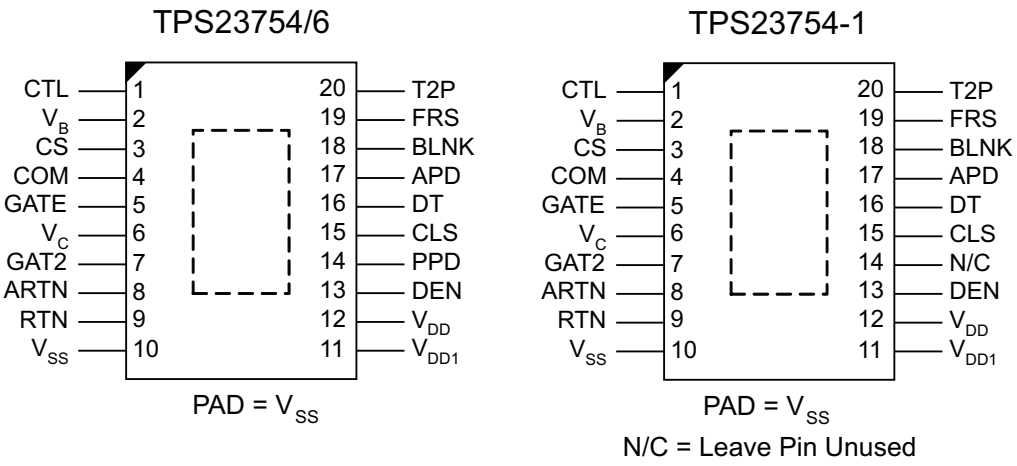
- 已更改 将标题更改成了 *TPS2375x 符合 IEEE 802.3at 标准的高效 PoE 接口和直流/直流控制器* 1

Changes from Revision G (October 2013) to Revision H **Page**

- 添加了*引脚配置和功能* 部分、*ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- Changed "Operating junction temperature" row to "Maximum junction temperature", and updated the MIN and MAX values to Internally limited 4

5 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TPS23754 and TPS23756	TPS23754-1		
APD	17	17	I	Raising $V_{APD} – V_{ARTN}$ above 1.5 V disables the internal hotswap switch, turns class off, and forces T2P active. This forces power to come from a external $V_{DD1-RTN}$ adapter. Tie APD to ARTN when not used.
ARTN	8	8	—	ARTN is the DC-DC converter analog return. Tie to RTN and COM on the circuit board.
BLNK	18	18	I	Connect to ARTN to use the internally set current-sense blanking period, or connect a resistor from BLNK to ARTN to program a more accurate period.
CLS	15	15	I	Connect a resistor from CLS to V_{SS} to program classification current. 2.5 V is applied to the program resistor during classification to set class current.
COM	4	4	—	Gate driver return, connect to ARTN and RTN.
CS	3	3	I/O	DC-DC converter switching MOSFET current sense input. See R_{CS} in Figure 27.
CTL	1	1	I	The control loop input to the pulse-width modulator (PWM), typically driven by output regulation feedback (for example, optocoupler). Use V_B as a pullup for CTL.
DEN	13	13	I/O	Connect a 24.9-kΩ resistor from DEN to V_{DD} to provide the PoE detection signature. Pulling this pin to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off.
DT	16	16	I	Connect a resistor from DT to ARTN to set the GATE to GAT2 dead time. Tie DT to V_B to disable GAT2 operation.
FRS	19	19	I	Connect a resistor from FRS to ARTN to program the converter switching frequency. FRS may be used to synchronize the converter to an external timing source.
GATE	5	5	O	Gate drive output for the main DC-DC converter switching MOSFET.
GAT2	7	7	O	Gate drive output for a second DC-DC converter switching MOSFET (see Figure 27).
NC	—	14	—	Float this no-connect pin.
PAD	—	—	—	Connect to V_{SS}.
PPD	14	—	I	Raising $V_{PPD-VSS}$ above 1.55 V enables the hotswap MOSFET and activates T2P. Connecting PPD to V_{DD} enables classification when APD is active. Tie PPD to V_{SS} or float when not used.
RTN	9	9	—	RTN is the output of the PoE hotswap MOSFET.
T2P	20	20	O	Active low output that indicates a PSE has performed the IEEE 802.3at type 2 hardware classification, PPD is active, or APD is active.

Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	TPS23754 and TPS23756	TPS23754-1		
V_B	2	2	O	5.1-V bias rail for DC-DC control circuits and the feedback optocoupler. Typically bypass with a 0.1 μF to ARTN.
V_C	6	6	I/O	DC-DC converter bias voltage. Connect a 0.47 μF (minimum) ceramic capacitor to ARTN at the pin, and a larger capacitor to power start-up.
V_{DD}	12	12	I	Connect to the positive PoE input power rail. V_{DD} powers the PoE interface circuits. Bypass with a 0.1-μF capacitor and protect with a TVS.
V_{DD1}	11	11	I	Source of DC-DC converter start-up current. Connect to V_{DD} for many applications.
V_{SS}	10	10	—	Connect to the negative power rail derived from the PoE source.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2). Voltage with respect to V_{SS} unless otherwise noted.

		MIN	MAX	UNIT
Input voltage	ARTN(2), COM(2), DEN, PPD, RTN(3), V_{DD}, V_{DD1}	–0.3	100	V
	CLS(4)	–0.3	6.5	
	[APD, BLNK(4), CTL, DT(4), FRS(4), VB(4)] to [ARTN, COM]	–0.3	6.5	
	CS to [ARTN,COM]	–0.3	V_B	
	[ARTN, COM] to RTN	–2	2	
Voltage	V_C, T2P, to [ARTN, COM]	–0.3	19	V
	GATE(4), GAT2(4) to [ARTN, COM]	–0.3	V_C+ 0.3	
Sinking current	RTN	Internally limited		mA
Sourcing current	V_B	Internally limited		mA
Average Sourcing or sinking current	GATE, GAT2		25	mArms
Maximum junction temperature, $T_{J(MAX)}$		Internally limited		°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ARTN and COM must be tied to RTN.
(3) I_{RTN} = 0 for V_{RTN} > 80 V.
(4) Do not apply voltage to these pins

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	
		System level (contact/air) at RJ-45(3)	8000 / 15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) ESD per EN61000-4-2. A power supply containing the TPS23754 was subjected to the highest test levels in the standard. See the ESD section.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted). Voltage with respect to V_{SS} (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input voltage range	ARTN, COM, PPD, RTN, V_{DD}, V_{DD1}	0		57	V
	T2P, V_C to [ARTN, COM]	0		18	V
	APD, CTL, DT to [ARTN, COM]	0		V_B	V
	CS to [ARTN, COM]	0		2	V
Continuous RTN current ($T_J \le 125°C$)(2)				825	mA
Sourcing current	V_B	0	2.5	5	mA
V_B capacitance		0.08			µF
R_{BLNK}		0		350	kΩ
Synchronization pulse width input (when used)		25			ns
Operating junction temperature range, T_J		–40		125	°C

(1) ARTN and COM tied to RTN.
(2) This is the minimum current limit value. Viable systems are designed for maximum currents less than this value with reasonable margin. IEEE 802.3at permits 600-mA continuous loading.

6.4 Thermal Information

THERMAL METRIC(1)		TPS23754, TPS23754-1, TPS23756 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter(2)	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance junction to case top for devices mounted per SLMA002. $T_J = T_{TOP} + (\Psi_{JT} \times P_J)$. Use Ψ_{JT} to validate T_J from measurements.

6.5 Electrical Characteristics

Unless otherwise noted: CS = COM = APD = CTL = RTN = ARTN, GATE and GAT2 float, R_{FRS}= 68.1 kΩ, R_{BLNK}= 249 kΩ, DT = V_B, PPD = V_{SS}, T2P open, C_{VB} = C_{VC} = 0.1 µF, R_{DEN} = 24.9 kΩ, R_{CLS} open, 0 V ≤ (V_{DD}, V_{DD1}) ≤ 57 V, 0 V ≤ V_C ≤ 18 V, –40°C ≤ T_J ≤ 125°C. Typical specifications are at 25°C.

CONTROLLER SECTION ONLY

[V_{SS} = RTN and V_{DD} = V_{DD1}] or [V_{SS} = RTN = V_{DD}], all voltages referred to [ARTN, COM]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C						
V_{CUV}	UVLO	V_C rising '754	14.3	15	15.7	V
		V_C rising '756	8.7	9	9.3	
V_{CUVH}		Hysteresis '754 (1)	6.2	6.5	6.8	
		Hysteresis '756 (1)	3.3	3.5	3.7	
	Operating current	V_C = 12 V, CTL = V_B, R_{DT} = 68.1 kΩ	0.7	0.92	1.2	mA
t_{ST}	Bootstrap start-up time, C_{VC} = 22 µF	TPS23756, V_{DD1} = 10.2 V, V_C(0) = 0 V	50	85	175	ms
		TPS23756, V_{DD1} = 35 V, V_C(0) = 0 V	27	45	92	
		TPS23754, V_{DD1} = 19.2 V, V_C(0) = 0 V	49	81	166	
		TPS23754, V_{DD1} = 35 V, V_C(0) = 0 V	44	75	158	
	Start-up current source is I_{VC}	TPS23754, V_{DD1} = 19.2 V, V_C = 13.9 V	1.7	3.4	5.5	mA
		TPS23756, V_{DD1} = 10.2 V, V_C = 8.6 V	0.44	1.06	1.8	
		TPS23754, TPS23756, V_{DD1} = 48 V, V_C = 0 V	2.7	4.8	6.8	
V_B						
	Voltage	6.5 V ≤ V_C ≤ 18 V, 0 ≤ I_{VB} ≤ 5 mA	4.8	5.1	5.25	V
FRS						
	Switching frequency	CTL = V_B, measure GATE				kHz
		R_{FRS} = 68.1 kΩ	227	253	278	
D_{MAX}	Duty cycle	CTL= V_B, measure GATE	76%	78%	80%	
V_{SYNC}	Synchronization	Input threshold	2	2.2	2.4	V
CTL						
V_{ZDC}	0% duty cycle threshold	V_{CTL} ↓ until GATE stops	1.3	1.5	1.7	V
	Input resistance		70	100	145	kΩ
CS						
V_{CSMAX}	Maximum threshold voltage	V_{CTL} = V_B, V_{CS} rising until GATE duty cycle drops	0.5	0.55	0.6	V
V_{SLOPE}	Internal slope compensation voltage	Peak voltage at maximum duty cycle, referenced to CS	120	155	185	mV
I_{SL_EX}	Peak slope compensation current	V_{CTL} = V_B, I_{CS} at maximum duty cycle	30	42	54	µA
	Bias current (sourcing)	DC component of I_{CS}	1	2.5	4.3	µA
GATE						
	Source current	V_{CTL} = V_B, V_C = 12 V, GATE high, pulsed measurement	0.37	0.6	0.95	A
	Sink current	V_{CTL} = V_B, V_C = 12 V, GATE low, pulsed measurement	0.7	1	1.4	A
GAT2						
	Source current	V_{CTL} = V_B, V_C = 12 V, GAT2 high, R_{DT} = 24.9 kΩ, pulsed measurement	0.37	0.6	0.95	A
	Sink current	V_{CTL} = V_B, V_C = 12 V, GAT2 low, R_{DT} = 24.9 kΩ, pulsed measurement	0.7	1	1.4	A

(1) The hysteresis tolerance tracks the rising threshold for a given device.

Electrical Characteristics (continued)

Unless otherwise noted: CS = COM = APD = CTL = RTN = ARTN, GATE and GAT2 float, R_{FRS}= 68.1 kΩ, R_{BLNK}= 249 kΩ, DT = V_B, PPD = V_{SS}, T2P open, C_{VB} = C_{VC} = 0.1 µF, R_{DEN} = 24.9 kΩ, R_{CLS} open, 0 V ≤ (V_{DD}, V_{DD1}) ≤ 57 V, 0 V ≤ V_C ≤ 18 V, –40°C ≤ T_J ≤ 125°C. Typical specifications are at 25°C.

CONTROLLER SECTION ONLY

[V_{SS} = RTN and V_{DD} = V_{DD1}] or [V_{SS} = RTN = V_{DD}], all voltages referred to [ARTN, COM]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
APD / PPD						
V_{APDEN}	APD threshold voltage	V_{APD} rising	1.43	1.5	1.57	V
V_{APDH}		Hysteresis (1)	0.29	0.31	0.33	
V_{PPDEN}	PPD threshold voltage	V_{PPD}- V_{VSS} rising, UVLO disable	1.45	1.55	1.65	V
V_{PPDH}		Hysteresis (1)	0.29	0.31	0.33	
V_{PPD2}		V_{PPD}- V_{VSS} rising, Class enable	7.4	8.3	9.2	V
V_{PPD2H}		Hysteresis (1)	0.5	0.6	0.7	
	APD leakage current (source or sink)	V_C = 12 V, V_{APD} = V_B			1	µA
I_{PPD}	PPD sink current	$V_{PPD-VSS}$ = 1.5 V	2.5	5	7.5	µA
THERMAL SHUTDOWN						
	turnon temperature	T_J rising	135	145	155	°C
	Hysteresis(2)			20		°C

(2) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

6.6 Electrical Characteristics: PoE and Control

[V_{DD} = V_{DD1}] or [V_{DD1} = RTN], V_C = RTN, COM = RTN = ARTN, all voltages referred to V_{SS} unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DETECTION (DEN)		(VDD = VDD1 = RTN = V_{SUPPLY} positive)				
	Detection current	Measure I_{SUPPLY}				
		V_{DD} = 1.6 V	62	64.3	66.5	µA
		V_{DD} = 10 V	399	406	414	
	Detection bias current	V_{DD} = 10 V, float DEN, measure I_{SUPPLY}, **Note:** Not during Mark state		5.6	10	µA
V_{PD_DIS}	Hotswap disable threshold		3	4	5	V
	DEN leakage current	V_{DEN} = V_{DD} = 57 V, float V_{DD1} and RTN, measure I_{DEN}		0.1	5	µA
CLASSIFICATION (CLS)		(V_{DD} = V_{DD1} = RTN = V_{SUPPLY} positive)				
I_{CLS}	Classification current, applies to both cycles	13 V ≤ V_{DD} ≤ 21 V, Measure I_{SUPPLY}				mA
		R_{CLS} = 1270 Ω	1.8	2.1	2.4	
		R_{CLS} = 243 Ω	9.9	10.4	10.9	
		R_{CLS} = 137 Ω	17.6	18.5	19.4	
		R_{CLS} = 90.9 Ω	26.5	27.7	29.3	
		R_{CLS} = 63.4 Ω	38	39.7	42	
	Classification mark resistance	5.6 V ≤ V_{DD} ≤ 9.4 V	7.5	9.7	12	kΩ
V_{CL_ON}	Classification regulator lower threshold	Regulator turns on, V_{DD} rising	11.2	11.9	12.6	V
V_{CL_H}		Hysteresis(1)	1.55	1.65	1.75	
V_{CU_OFF}	Classification regulator upper threshold	Regulator turns off, V_{DD} rising	21	22	23	V
V_{CU_H}		Hysteresis(1)	0.5	0.75	1	
V_{MSR}	Mark state reset	V_{DD} falling	3	4	5	V
	Leakage current	V_{DD} = 57 V, V_{CLS} = 0 V, DEN = V_{SS}, measure I_{CLS}			1	µA

(1) The hysteresis tolerance tracks the rising threshold for a given device.

Electrical Characteristics: PoE and Control (continued)

[V_{DD} = V_{DD1}] or [V_{DD1} = RTN], V_C = RTN, COM = RTN = ARTN, all voltages referred to V_{SS} unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PASS DEVICE (RTN)		(V_{DD1} = RTN)				
	On resistance		0.25	0.43	0.75	Ω
	Current limit	V_{RTN} = 1.5 V, V_{DD} = 48 V, pulsed measurement	850	970	1100	mA
	Inrush limit	V_{RTN} = 2 V, V_{DD}: 0 V → 48 V, pulsed measurement	100	140	180	mA
	Foldback voltage threshold	V_{DD} rising	11	12.3	13.6	V
UVLO						
V_{UVLO_R}	UVLO threshold	V_{DD} rising	33.9	35	36.1	V
V_{UVLO_H}		Hysteresis(1)	4.4	4.55	4.76	
T2P						
	ON characteristic	Perform classification algorithm, $V_{T2P-RTN}$ = 1 V, CTL = ARTN	2			mA
	Leakage current	V_{T2P} = 18 V, CTL = V_B			10	μA
THERMAL SHUTDOWN						
	Turnoff temperature	T_J rising	135	145	155	°C
	Hysteresis(2)			20		°C

(2) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CTL						
	Soft-start period	Interval from switching start to V_{CSMAX}	1.9	3.9	6.2	ms
BLNK						
	Blanking delay (In addition to t_1)	BLNK = RTN	35	55	78	ns
		R_{BLNK} = 49.9 kΩ	38	55	70	
DT						
	Dead time See Figure 1 for t_{DTx} definition	CTL = V_B, C_{GATE} = 1 nF, C_{GAT2} = 1 nF, measure GATE, GAT2				ns
t_{DT1}		R_{DT} = 24.9 kΩ, GAT2 ↑ to GATE ↑	40	50	62.5	
t_{DT2}		R_{DT} = 24.9 kΩ, GATE ↓ to GAT2 ↓	40	50	62.5	
t_{DT1}		R_{DT} = 75 kΩ, GAT2 ↑ to GATE ↑	120	150	188	
t_{DT2}		R_{DT} = 75 kΩ, GATE ↓ to GAT2 ↓	120	150	188	
CS						
t_1	Turnoff delay	V_{CS} = 0.65 V	24	40	70	ns
PoE AND CONTROL - T2P						
t_{T2P}	Delay	From start of switching to T2P active	5	9	15	ms

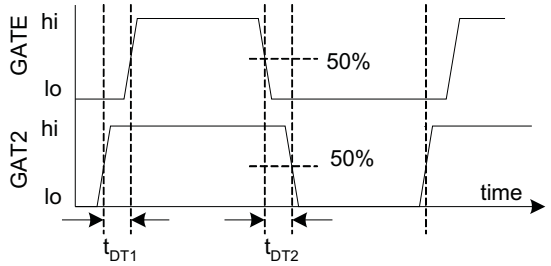


Figure 1. GATE and GAT2 Timing and Phasing

6.8 Typical Characteristics

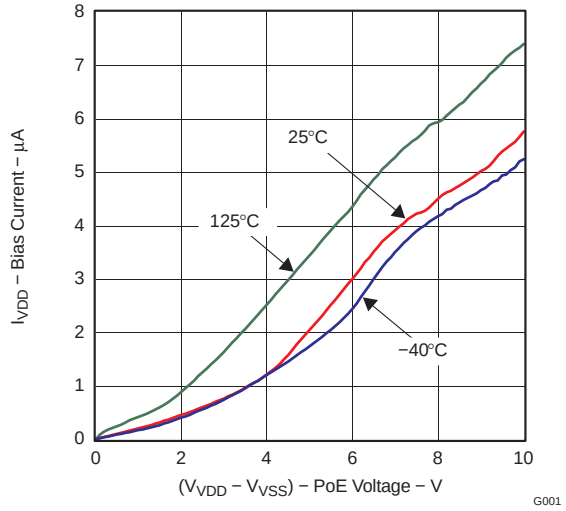


Figure 2. Detection Bias Current vs Voltage

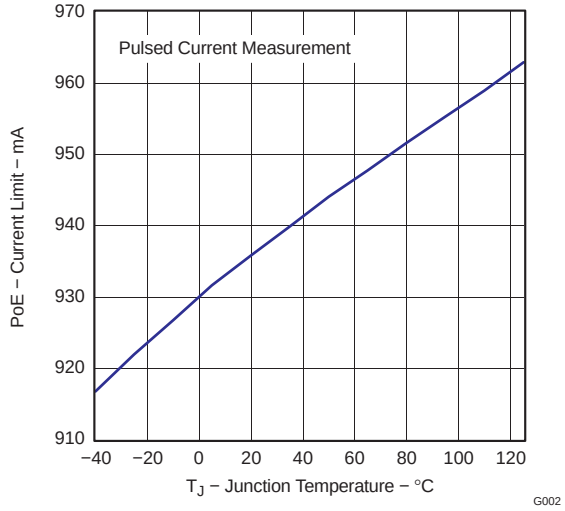


Figure 3. PoE Current Limit vs Temperature

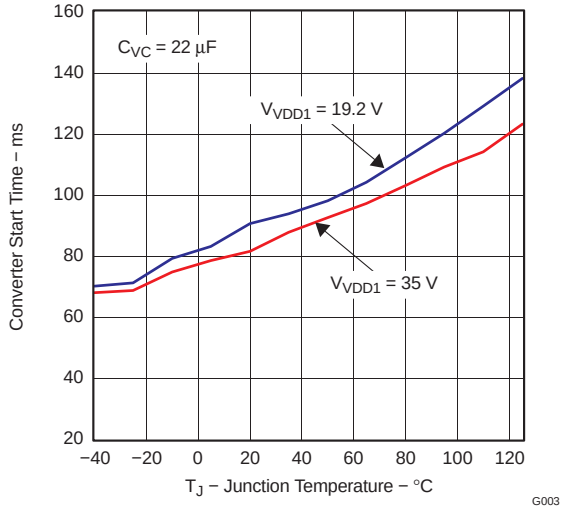


Figure 4. '754 Converter Start Time vs Temperature

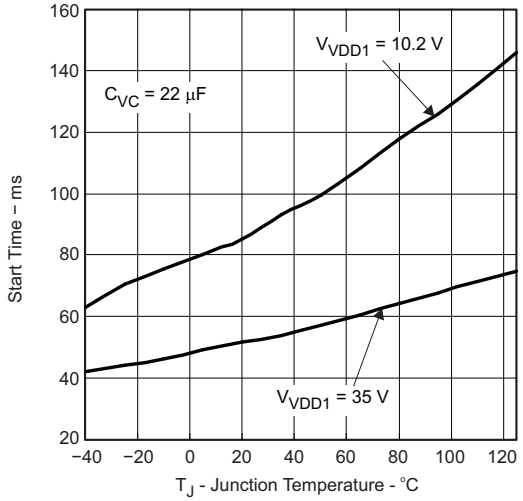


Figure 5. '756 Converter Start Time vs Temperature

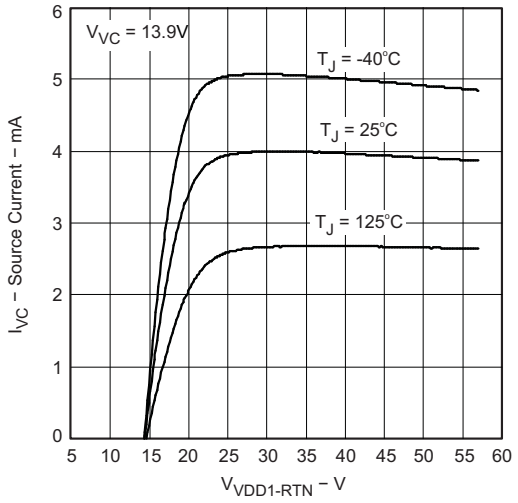


Figure 6. '754 Converter Start-Up Current vs V_{VDD1}

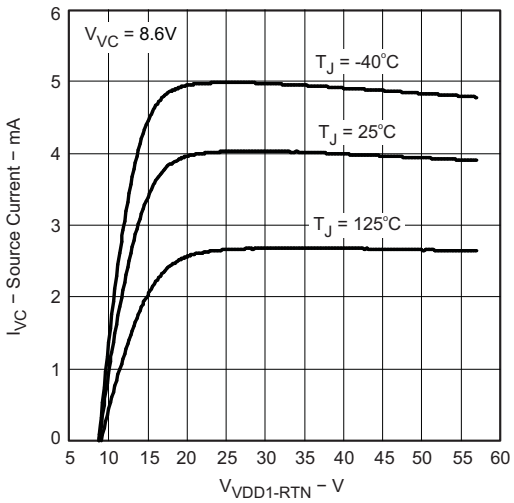


Figure 7. '756 Converter Start-Up Current vs V_{VDD1}

Typical Characteristics (continued)

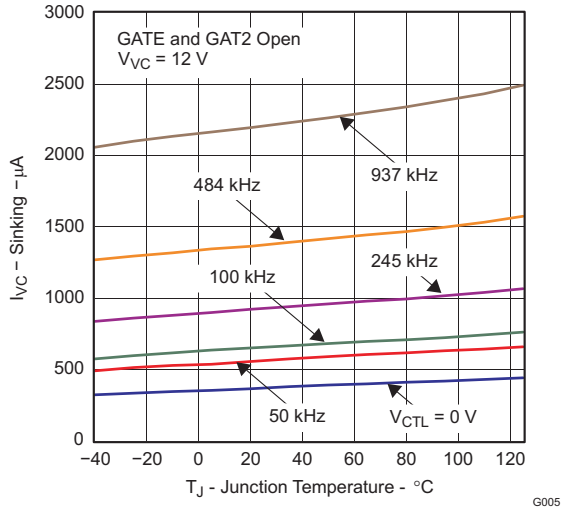


Figure 8. Controller Bias Current vs Temperature

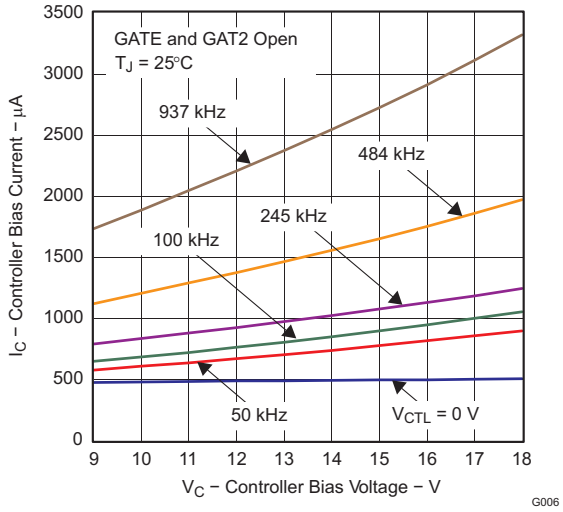


Figure 9. '754 Controller Bias Current vs Voltage

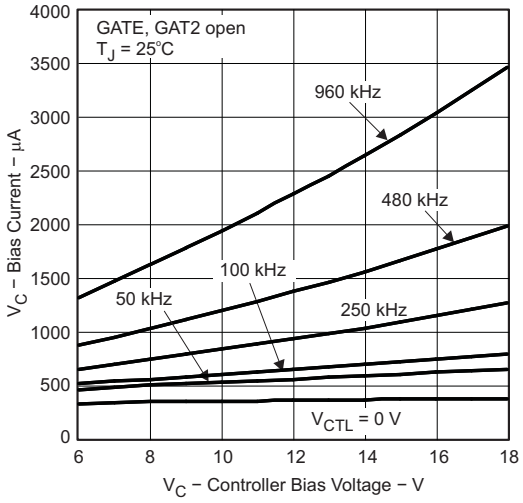


Figure 10. '756 Controller Bias Current vs Voltage

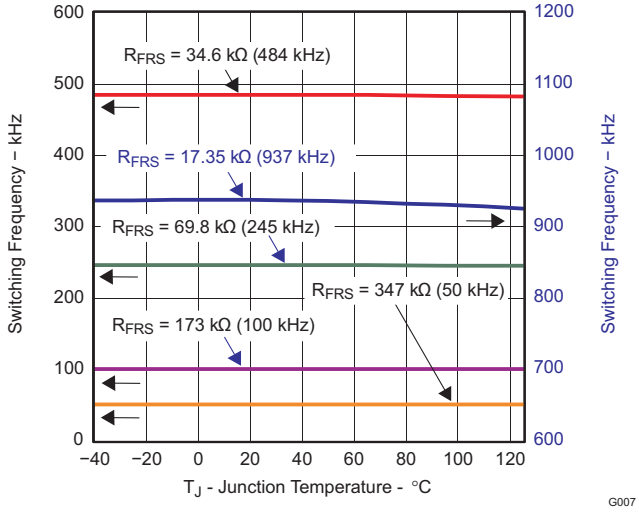


Figure 11. Switching Frequency vs Temperature

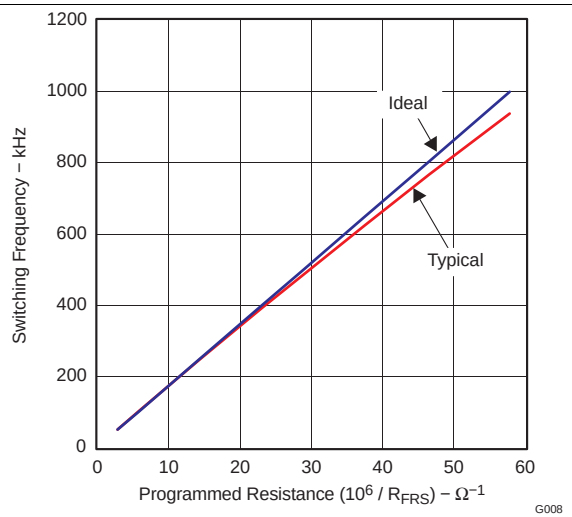


Figure 12. Switching Frequency vs Program Conductance

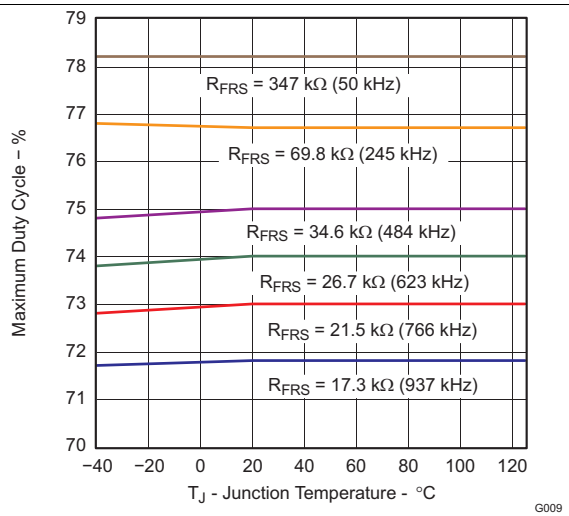


Figure 13. Maximum Duty Cycle vs Temperature

Typical Characteristics (continued)

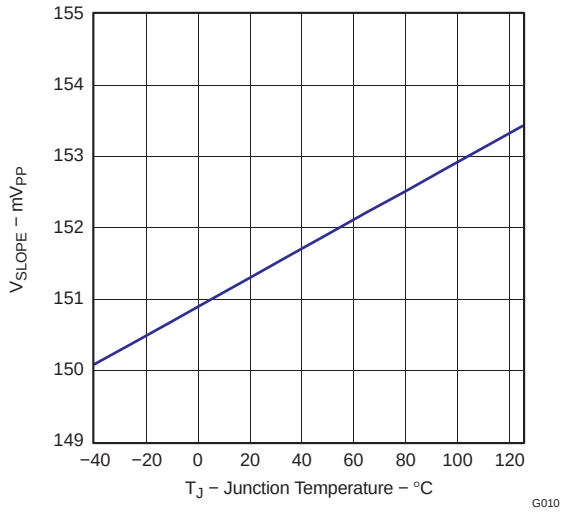


Figure 14. Current Slope Compensation Voltage vs Temperature

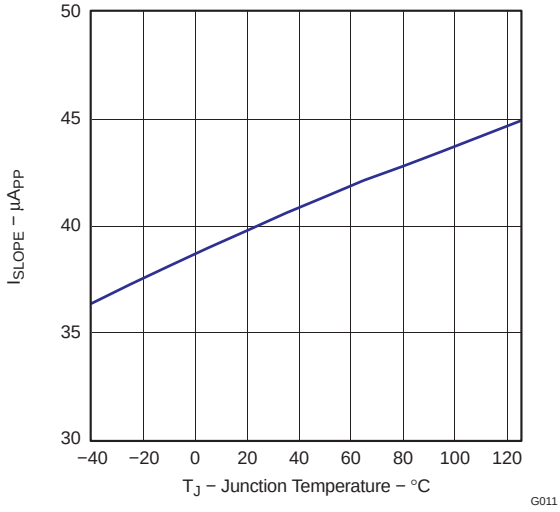


Figure 15. Current Slope Compensation Current vs Temperature

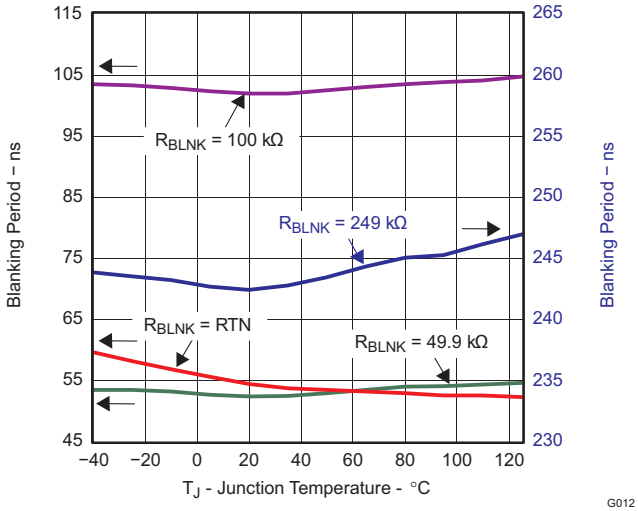


Figure 16. Blanking Period vs Temperature

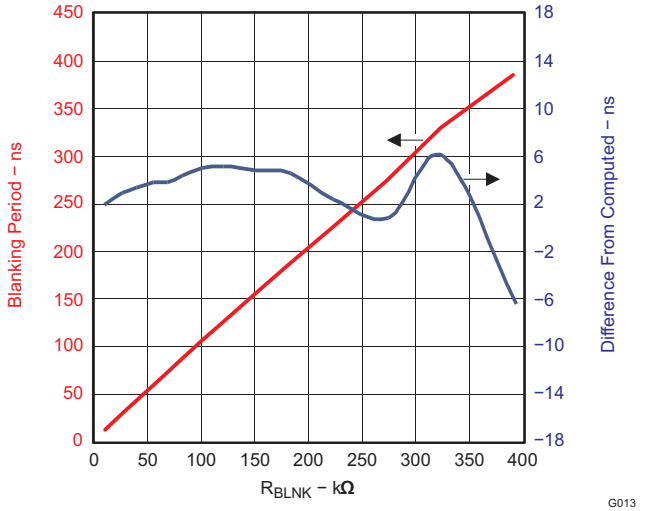


Figure 17. Blanking Period vs Blanking Resistance (R_{BLNK})

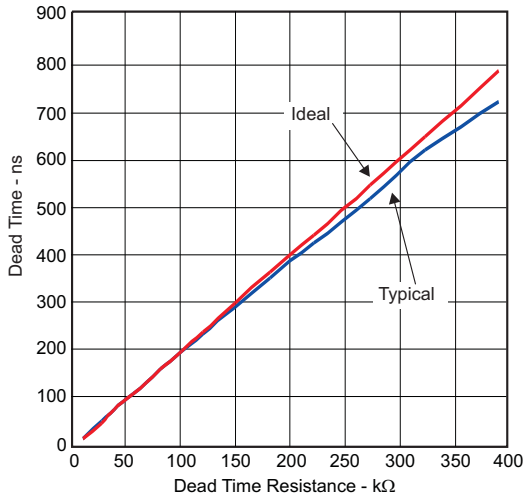


Figure 18. Dead Time vs Dead Time Resistance (R_{DT})

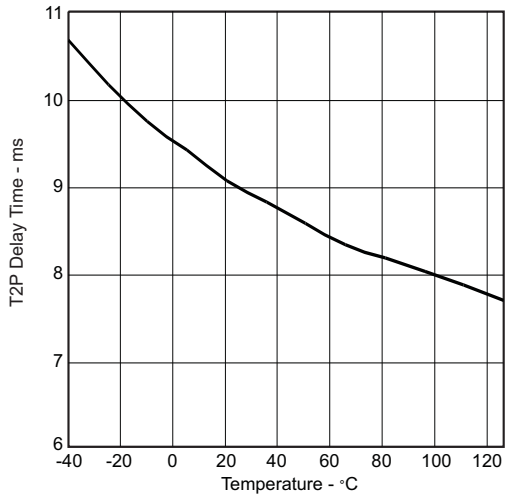


Figure 19. T2P Delay Time vs Temperature

7 Detailed Description

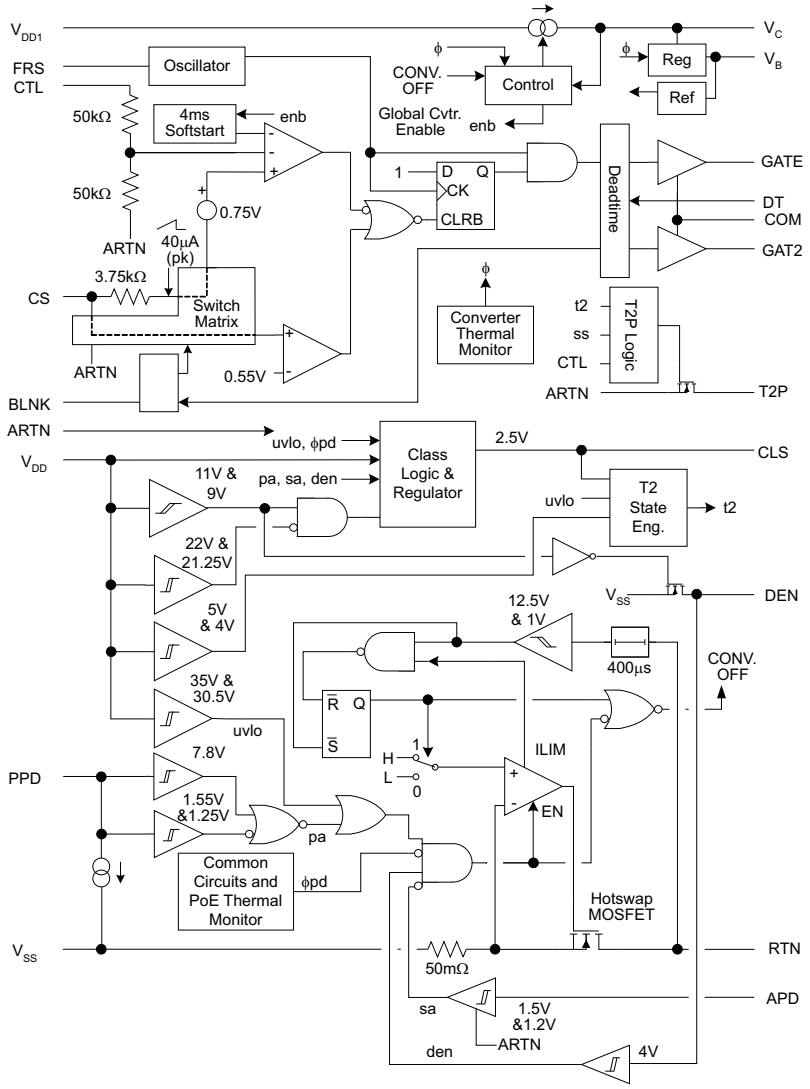
7.1 Overview

The TPS23754 and TPS23756 devices have a PoE that contains all of the features needed to implement an IEEE802.3at type-2 powered device (PD) such as Detection, Classification, Type 2 Hardware Classification, and 140-mA inrush current limit during start-up. It combines a current mode DC-DC controller optimized specifically for isolated converters.

The TPS23754 and TPS23756 devices integrate a low 0.5-Ω internal switch to allow for up to 0.85 A of continuous current through the PD during normal operation.

The TPS23754 and TPS23756 devices contain several protection features such as thermal shutdown, current limit foldback, and a robust 100-V internal switch.

7.2 Functional Block Diagram



7.3 Feature Description

See Figure 27 for component reference designators (R_{CS} for example), and the *Electrical Characteristics* for values denoted by reference (V_{CSMAX} for example). Electrical characteristic values take precedence over any numerical values used in the following sections.

Feature Description (continued)

7.3.1 APD

APD forces power to come from an external adapter connected from V_{DD1} to RTN by opening the hotswap switch, disabling the CLS output (see PPD pin description), and enabling the T2P output. TI recommends a resistor divider on APD when it is connected to an external adapter. The divider provides ESD protection, leakage discharge for the adapter ORing diode, and input voltage qualification. Voltage qualification assures the adapter output voltage is high enough that it can support the PD before the PoE current is cut off.

Select the APD divider resistors per Equation 1 where $V_{ADPTR-ON}$ is the desired adapter voltage that enables the APD function as adapter voltage rises.

$$R_{APD1} = R_{APD2} \times \left(V_{ADPTR\_ON} - V_{APDEN}\right) / V_{APDEN}$$

$$V_{ADPTR\_OFF} = \frac{R_{APD1} + R_{APD2}}{R_{APD2}} \times \left(V_{APDEN} - V_{APDH}\right) \quad (1)$$

Place the APD pulldown resistor adjacent to the APD pin.

APD should be tied to ARTN when not used.

7.3.2 BLNK

Blanking provides an interval between GATE going high and the current-control comparators on CS actively monitoring the input. This delay allows the normal turnon current transient (spike) to subside before the comparators are active, preventing undesired short duty cycles and premature current limiting.

Connect BLNK to ARTN to obtain the internally set blanking period. Connect a resistor from BLNK to ARTN for a more accurate, programmable blanking period. The relationship between the desired blanking period and the programming resistor is defined by Equation 2.

$$R_{BLNK}\left(k\Omega\right) = t_{BLNK}\left(ns\right) \quad (2)$$

Place the resistor adjacent to the BLNK pin when it is used.

7.3.3 CLS

A resistor from CLS to V_{SS} programs the classification current per the IEEE standard. The PD power ranges and corresponding resistor values are listed in Table 1. The power assigned should correspond to the maximum average power drawn by the PD during operation.

High-power PSEs may perform two classification cycles if Class 4 is presented on the first cycle. The TPS23754 device presents the same (resistor programmed) class each cycle per the standard.

Table 1. Class Resistor Selection

CLASS	POWER AT PD		RESISTOR (Ω)	NOTES
	MINIMUM (W)	MAXIMUM (W)		
0	0.44	13	1270	Minimum may be reduced by pulsed loading. Serves as a catch-all default class.
1	0.44	3.84	243	
2	3.84	6.49	137	
3	6.49	13	90.9	
4	13	25.5	63.4	Not allowed before IEEE 802.3at. Use to indicate a Type 2 PD (high power) device per IEEE 802.3at.

7.3.4 Current Sense (CS)

The CS input for the DC-DC converter should be connected to the high side of the switching MOSFET's current sense resistor (R_{CS}). The current limit threshold, V_{CSMAX}, defines the voltage on CS above which the GATE ON time will be terminated regardless of the voltage on CTL.

The TPS23754 device provides internal slope compensation (150 mV, V_{SLOPE}), an output current for additional slope compensation, a peak current limiter, and an off-time pulldown to this pin.

Routing between the current-sense resistor and the CS pin should be short to minimize cross-talk from noisy traces such as the gate drive signal.

7.3.5 Control (CTL)

CTL is the voltage-control loop input to the pulse-width modulator (PWM). Pulling V_{CTL} below V_{ZDC} causes GATE to stop switching. Increasing V_{CTL} above V_{ZDC} (0 duty cycle voltage) raises the switching MOSFET programmed peak current. The maximum (peak) current is requested at approximately V_{ZDC} + (2 × V_{CSMAX}). The AC gain from CTL to the PWM comparator is 0.5. The internal divider from CTL to ARTN is approximately 100 kΩ.

Use V_B as a pullup source for CTL.

7.3.6 Detection and Enable (DEN)

DEN is a multifunction pin for PoE detection and inhibiting operation from PoE power. Connect a 24.9-kΩ resistor from DEN to V_{DD} to provide the PoE detection signature. DEN goes to a high-impedance state when $V_{VDD-VSS}$ is outside of the detection range. Pulling DEN to V_{SS} during powered operation causes the internal hotswap MOSFET and class regulator to turn off, while the reduced detection resistance prevents the PD from properly redetecting.

7.3.7 DT

Dead-time programming sets the delay between GATE and GAT2 to prevent overlap of MOSFET ON times as shown in Figure 1. GAT2 turns the second MOSFET off when it transitions high. Both MOSFETs should be off between GAT2 going high to GATE going high, and GATE going low to GAT2 going low. The maximum GATE ON time is reduced by the programmed dead-time period. The dead time period is specified with 1 nF of capacitance on GATE and GAT2. Different loading on these pins changes the effective dead time.

A resistor connected from DT to ARTN sets the delay between GATE and GAT2 per Equation 3.

$$R_{DT}\left(k\Omega\right) = \frac{t_{DT}\left(ns\right)}{2} \tag{3}$$

Connect DT to V_B to set the dead time to 0 and turn GAT2 off.

7.3.8 Frequency and Synchronization (FRS)

Connect a resistor from FRS to ARTN to program the converter switching frequency. Select the resistor per the following relationship.

$$R_{FRS}(k\Omega) = \frac{17250}{f_{SW}(kHz)} \tag{4}$$

The converter may be synchronized to a frequency above its maximum free-running frequency by applying short AC-coupled pulses into the FRS pin per Figure 30.

The FRS pin is high impedance. Keep the connections short and apart from potential noise sources. Take special care to avoid crosstalk when synchronizing circuits are used.

7.3.9 GATE

Gate drive output for the DC-DC converter's main switching MOSFET. GATE's phase turns the main switch on when it transitions high, and off when it transitions low. GATE is held low when the converter is disabled.

7.3.10 GAT2

GAT2 is the second gate drive output for the DC-DC converter. GAT2's phase turns the second switch off when it transitions high, and on when it transitions low. This drives active-clamp PMOS devices per Figure 27, and driven flyback synchronous rectifiers per Figure 27. See the DT pin description for GATE to GAT2 timing. Connecting DT to V_B disables GAT2 in a high-impedance condition. GAT2 is low when the converter is disabled.

7.3.11 PPD

PPD is a multifunction pin that has two voltage thresholds, PPD1 and PPD2.

PPD1 permits power to come from an external low voltage adapter, that is, 24 V, connected from V_{DD} to V_{SS} by overriding the normal hotswap UVLO. Voltage on PPD more than 1.55 V (V_{PPDEN}) enables the hotswap MOSFET, inhibits class current, and enables T2P. A resistor divider per Figure 34 provides ESD protection, leakage discharge for the adapter ORing diode, reverse adapter protection, and input voltage qualification. Voltage qualification assures the adapter output voltage is high enough that it can support the PD before it begins to draw current.

$$R_{PPD1} = \left(\frac{V_{ADPTR\_ON} - V_{PPDEN}}{\frac{V_{PPDEN}}{R_{PPD2}} + I_{PPD}} \right)$$

$$V_{ADPTR\_OFF} = (V_{PPDEN} - V_{PPDH}) + \left[R_{PPD1} \times \left(\frac{(V_{PPDEN} - V_{PPDH})}{R_{PPD2}} + I_{PPD} \right) \right] \quad (5)$$

PPD2 enables normal class regulator operation when V_{PPD} is more than 8.3 V to permit type 2 classification when APD is used in conjunction with diode D_{VDD} (see Figure 33). Tie PPD to V_{DD} when PPD2 operation is desired.

The PPD pin has a 5-μA internal pulldown current.

Locate the PPD pulldown resistor adjacent to the pin when used.

PPD may be tied to V_{SS} or left open when not used.

7.3.12 RTN, ARTN, COM

RTN is internally connected to the drain of the PoE hotswap MOSFET, while ARTN is the quiet analog reference for the DC-DC controller return. COM serves as the return path for the gate drivers and should be tied to ARTN on the circuit board. The ARTN / COM / RTN net should be treated as a local reference plane (ground plane) for the DC-DC control and converter primary. RTN and (ARTN/COM) may be separated by several volts for special applications.

7.3.13 T2P

T2P is an active low output that indicates [(V_{APD} > 1.5 V) OR (1.55 V ≤ V_{PPD} ≤ 8.3 V) OR (type 2 hardware classification observed)]. T2P is valid after both a delay of t_{T2P} from the start of converter switching, and [V_{CTL} ≤ (V_B – 1 V)]. Once T2P is valid, V_{CTL} does not affect it. T2P becomes invalid if the converter goes back into soft start, overtemperature, or is held off by the PD during C_{IN} recharge (inrush). T2P is referenced to ARTN and is intended to drive the diode side of an optocoupler. T2P should be left open or tied to ARTN if not used.

7.3.14 V_B

V_B is an internal 5.1-V regulated DC-DC controller supply rail that is typically bypassed by a 0.1-μF capacitor to ARTN. V_B should be used to bias the feedback optocoupler.

7.3.15 V_C

V_C is the bias supply for the DC-DC controller. The MOSFET gate drivers run directly from V_C. V_B is regulated down from V_C, and is the bias voltage for the rest of the converter control. A start-up current source from V_{DD1} to V_C is controlled by a comparator with hysteresis to implement the converter bootstrap start-up. V_C must be connected to a bias source, such as a converter auxiliary output, during normal operation.

A minimum 0.47 μF-capacitor, located adjacent to the V_C pin, should be connected from V_C to COM to bypass the gate driver. A larger total capacitance is required for start-up to provide control power between the time the converter starts switching and the availability of the converter auxiliary output voltage.

7.3.16 V_{DD}

V_{DD} is the positive input power rail that is derived from the PoE source (PSE). V_{DD} should be bypassed to V_{SS} with a 0.1-μF capacitor as required by the IEEE standard. A transient suppressor diode (TVS), a special type of Zener diode, such as SMAJ58A should be connected from V_{DD} to V_{SS} to protect against overvoltage transients.

7.3.17 V_{DD1}

V_{DD1} is the DC-DC converter start-up supply. Connect to V_{DD} for many applications. V_{DD1} may be isolated by a diode from V_{DD} to support PoE priority operation.

7.3.18 V_{SS}

V_{SS} is the PoE input-power return side. It is the reference for the PoE interface circuits and has a current limited hotswap switch that connects it to RTN. V_{SS} is clamped to a diode drop above RTN by the hotswap switch.

A local V_{SS} reference plane should be used to connect the input bypass capacitor, TVS, R_{CLS}, and the PowerPAD. This plane becomes the main heatsink for the TPS23754.

V_{SS} is internally connected to the PowerPAD.

7.3.19 PowerPAD

The PowerPAD is internally connected to V_{SS}. It should be tied to a large V_{SS} copper area on the PCB to provide a low-resistance thermal path to the circuit board. TI recommends that a clearance of 0.025” be maintained between V_{SS}, RTN, and various control signals to high-voltage signals such as V_{DD} and V_{DD1}.

7.4 Device Functional Modes

The following text is intended as an aid in understanding the operation of the TPS23754, but not as a substitute for the IEEE 802.3at standard. The IEEE 802.3at standard is an update to IEEE 802.3-2008 clause 33 (PoE), adding high-power options and enhanced classification. Generally speaking, a device compliant to IEEE 802.3-2008 is referred to as a type 1 device, and devices with high power and enhanced classification are referred to as type 2 devices. Standards change and should always be referenced when making design decisions.

7.4.1 PoE Overview

The IEEE 802.3at standard defines a method of safely powering a PD over a cable by power sourcing equipment (PSE), and then removing power if a PD is disconnected. The process proceeds through an idle state and three operational states of detection, classification, and operation. The PSE leaves the cable unpowered (idle state) while it periodically looks to see if something has been plugged in; this is referred to as detection. The low-power levels used during detection are unlikely to damage devices not designed for PoE. If a valid PD signature is present, the PSE my inquire how much power the PD requires; this is referred to as classification. The PSE may then power the PD if it has adequate capacity.

Type 2 PSEs are required to do type 1 hardware classification, plus a (new) data-layer classification, or an enhanced type 2 hardware classification. Type 1 PSEs are not required to do hardware or data link layer (DLL) classification. A type 2 PD must do type 2 hardware classification as well as DLL classification. The PD may return the default, 13W current-encoded class, or one of four other choices. DLL classification occurs after power-on and the ethernet data link has been established.

Once started, the PD must present the maintain power signature (MPS) to assure the PSE that it is still present. The PSE monitors its output for a valid MPS, and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the idle state. Figure 20 shows the operational states as a function of PD input voltage. The upper half is for IEEE 802.3-2008, and the lower half shows specific differences for IEEE 802.3at. The dashed lines in the lower half indicate these are the same (for example, Detect and Class) for both.

Device Functional Modes (continued)

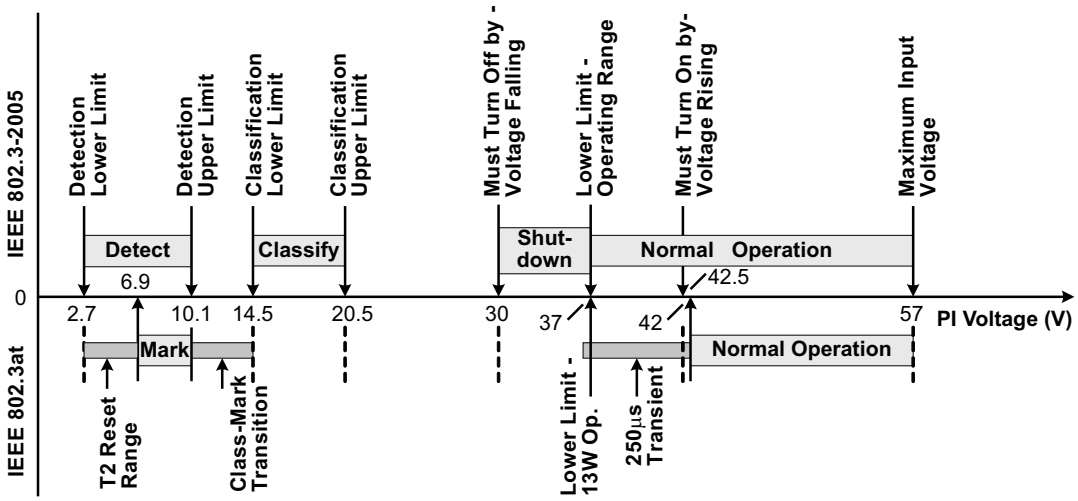


Figure 20. Operational States for PD

The PD input, typically an RJ-45 eight-lead connector, is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops and operating margin. The standard allots the maximum loss to the cable regardless of the actual installation to simplify implementation. IEEE 802.3-2008 was designed to run over infrastructure including ISO/IEC 11801 class C (CAT3 per TIA/EIA-568) that may have had AWG 26 conductors. IEEE 802.3at type 2 cabling power loss allotments and voltage drops have been adjusted for 12.5-Ω power loops per ISO/IEC11801 class D (CAT5 or higher per TIA/EIA-568, typically AWG number 24 conductors). Table 2 shows key operational limits broken out for the two revisions of the standard.

Table 2. Comparison of Operational Limits

STANDARD	POWER LOOP RESISTANCE (max)	PSE OUTPUT POWER (min)	PSE STATIC OUTPUT VOLTAGE (min)	PD INPUT POWER (max)	STATIC PD INPUT VOLTAGE	
					POWER ≤ 13 W	POWER > 13 W
IEEE 802.3-2008 802.3at (Type 1)	20 Ω	15.4 W	44 V	13 W	37 – 57 V	N/A
802.3at (Type 2)	12.5 Ω	30 W	50 V	25.5 W	37 – 57 V	42.5 – 57 V

The PSE can apply voltage either between the RX and TX pairs (pins 1 to 2 and 3 to 6 for 10baseT or 100baseT), or between the two spare pairs (4 to 5 and 7 to 8). Power application to the same pin combinations in 1000baseT systems is recognized in IEEE 802.3at. 1000baseT systems can handle data on all pairs, eliminating the spare pair terminology. The PSE may only apply voltage to one set of pairs at a time. The PD uses input diode bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the standard limits at the PI and the TPS23754 specifications.

A compliant type 2 PD has power management requirements not present with a type 1 PD. These requirements include the following:

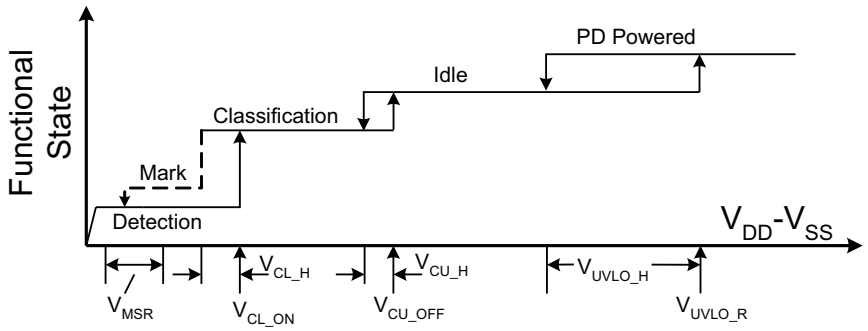
1. Must interpret type 2 hardware classification
2. Must present hardware class 4
3. Must implement DLL negotiation
4. Must behave like a type 1 PD during inrush and start-up
5. Must not draw more than 13 W for 80 ms after PSE applies operating voltage (power up)
6. Must not draw more than 13 W if it has not received a type 2 hardware classification or received permission through DLL
7. Must meet various operating and transient templates

8. Optionally monitor for the presence or absence of an adapter (assume high power)

As a result of these requirements, the PD must be able to dynamically control its loading and monitor T2P for changes. In cases where the design must know specifically if an adapter is plugged in and operational, the adapter should be individually monitored, typically with an optocoupler.

7.4.1.1 Threshold Voltages

The TPS23754 has a number of internal comparators with hysteresis for stable switching between the various states. Figure 21 relates the parameters in the *Electrical Characteristics* to the PoE states. The mode labeled idle between classification and operation implies that the DEN, CLS, and RTN pins are all high impedance. The state labeled Mark, which is drawn in dashed lines, is part of the new type 2 hardware class state machine.



Note: Variable names refer to Electrical Characteristic Table parameters

Figure 21. Threshold Voltages

7.4.1.2 PoE Start-Up Sequence

The waveforms of Figure 22 demonstrate detection, classification, and start-up from a PSE with type 2 hardware classification. The key waveforms shown are V_{VDD}-V_{VSS}, V_{RTN}-V_{VSS}, and I_{PI}. IEEE 802.3at requires a minimum of two detection levels, two class and mark cycles, and start-up from the second mark event. V_{RTN} to V_{SS} falls as the TPS23754 charges C_{IN} following application of full voltage. Subsequently, the converter starts up, drawing current as seen in the I_{PI} waveform.

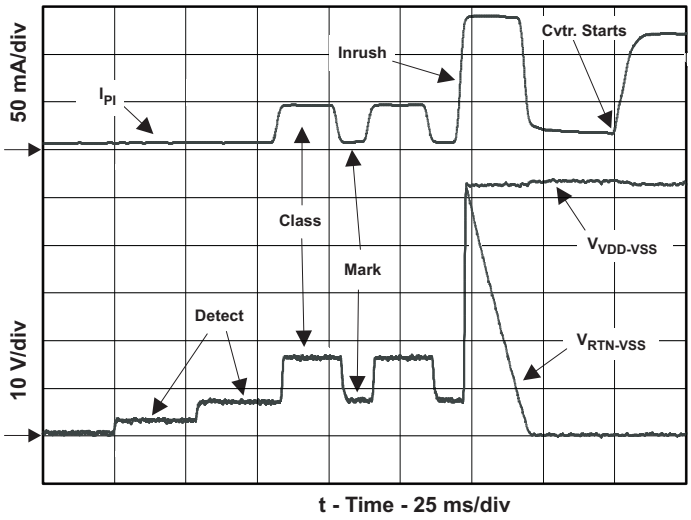


Figure 22. Start-Up

7.4.1.3 Detection

The TPS23754 drives DEN to V_{SS} whenever V_{VDD}-V_{VSS} is below the lower classification threshold. When the input voltage rises above V_{CL-ON}, the DEN pin goes to an open-drain condition to conserve power. While in detection, RTN is high impedance, and almost all the internal circuits are disabled. An R_{DEN} of 24.9 kΩ (1%), presents the correct signature. It may be a small, low-power resistor because it only sees a stress of about 5 mW. A valid PD detection signature is an incremental resistance (ΔV / ΔI) from 23.7 kΩ to 26.3 kΩ at the PI.

The detection resistance seen by the PSE at the PI is the result of the input bridge resistance in series with the parallel combination of R_{DEN} and internal V_{DD} loading. The input diode bridge's incremental resistance may be hundreds of ohms at the very low currents drawn when 2.7 V is applied to the PI. The input bridge resistance is partially cancelled by the TPS23754's effective resistance during detection.

The type 2 hardware classification protocol of IEEE 802.3at specifies that a type 2 PSE drops its output voltage into the detection range during the classification sequence. The PD is required to have an incorrect detection signature in this condition, which is referred to as the mark event (see Figure 22). After the first mark event, the TPS23754 will present a signature less than 12 kΩ until it has experienced a V_{VDD}-V_{VSS} voltage below the mark reset (V_{MSR}). This is explained more fully in *Hardware Classification*.

7.4.1.4 Hardware Classification

Hardware classification allows a PSE to determine a PD's power requirements before powering, and helps with power management once power is applied. Type 2 hardware classification permits high power PSEs and PDs to determine whether the connected device can support high-power operation. A type 2 PD presents class 4 in hardware to indicate it is a high-power device. A type 1 PSE will treat a class 4 device like a class 0 device, allotting 13 W if it chooses to power the PD. A PD that receives a 2 event class understands that it is powered from a high-power PSE and it may draw up to 25.5 W immediately after the 80-ms start-up period completes. A type 2 PD that does not receive a 2-event hardware classification may choose to not start, or must start in a 13 W condition and request more power through the DLL after start-up. The standard requires a type 2 PD to indicate that it is underpowered if this occurs. Start-up of a high-power PD under 13 W implicitly requires some form of powering down sections of the application circuits.

The maximum power entries in Table 1 determine the class the PD must advertise. The PSE may disconnect a PD if it draws more than its stated class power, which may be the hardware class or a lower DLL-derived power level. The standard permits the PD to draw limited current peaks that increase the instantaneous power above the Table 1 limit; however, the average power requirement always applies.

The TPS23754 implements two-event classification. Selecting an R_{CLS} of 63.4 Ω provides a valid type 2 signature. TPS23754 may be used as a compatible type 1 device simply by programming class 0–3 per Table 1. DLL communication is implemented by the ethernet communication system in the PD and is not implemented by the TPS23754.

The TPS23754 disables classification above V_{CU_OFF} to avoid excessive power dissipation. CLS voltage is turned off during PD thermal limit or when APD or $\overline{DEN}$ are active. The CLS output is inherently current limited, but should not be shorted to V_{SS} for long periods of time.

Figure 23 shows how classification works for the TPS23754. Transition from state-to-state occurs when comparator thresholds are crossed (see Figure 20 and Figure 21). These comparators have hysteresis, which adds inherent memory to the machine. Operation begins at idle (unpowered by PSE) and proceeds with increasing voltage from left to right. A 2-event classification follows the (heavy-lined) path towards the bottom, ending up with a latched type 2 decode along the lower branch that is highlighted. This state results in a low T2P during normal operation. Once the valid path to type 2 PSE detection is broken, the input voltage must transition below the mark reset threshold to start anew.

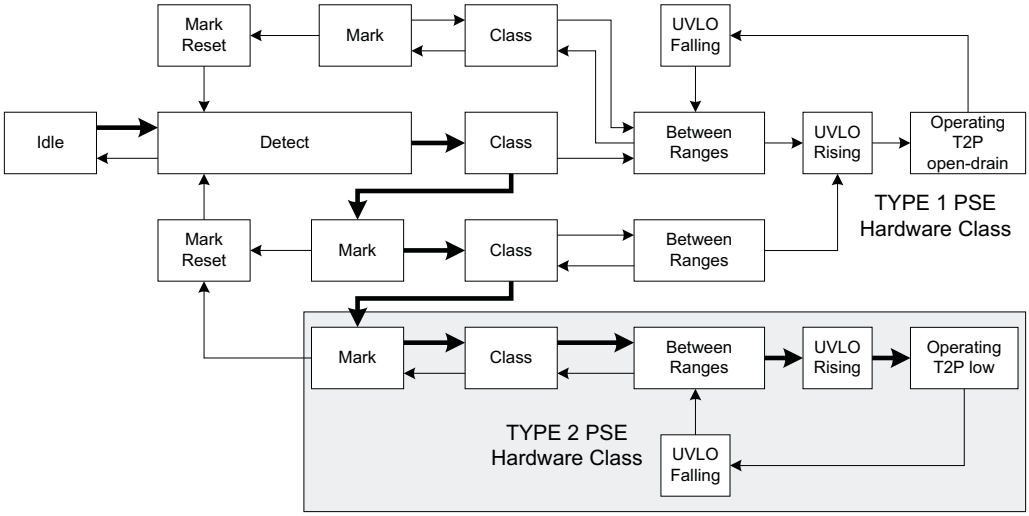


Figure 23. Two-Event Class Internal States

7.4.1.5 Inrush and Start-Up

802.3at has a start-up current and time limitation, providing type 2 PSE compatibility for type 1 PDs. A type 2 PSE limits output current to from 400 mA to 450 mA for up to 75 ms after power up (applying 48 V to the PI) to mirror type 1 PSE functionality. The type 2 PSE supports higher output current after 75 ms. The TPS23754 implements a 140-mA inrush current, which is compatible with all PSE types. A high-power PD must control its converter start-up peak and operational currents drawn to less than 400 mA for 80 ms. The TPS23754 device's internal soft-start permits control of the converter start-up; however, the application circuits must assure that their power draw does not cause the PD to exceed the current/time limitation. This requirement implicitly requires some form of powering down sections of the application circuits. T2P becomes valid within t_{T2P} after switching starts, or if an adapter is plugged in while the PD is operating from a PSE.

7.4.1.6 Maintain Power Signature

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. A valid MPS consists of a minimum DC current of 10 mA (or a 10-mA pulsed current for at least 75 ms every 325 ms) and an AC impedance lower than 26.3 kΩ in parallel with 0.05 µF. The AC impedance is usually accomplished by the minimum operating C_{IN} requirement of 5 µF. When either APD or DEN is used to force the hotswap switch off, the DC MPS will not be met. A PSE that monitors the DC MPS will remove power from the PD when this occurs. A PSE that monitors only the AC MPS may remove power from the PD.

7.4.1.7 Start-Up and Converter Operation

The internal PoE undervoltage lockout (UVLO) circuit holds the hotswap switch off before the PSE provides full voltage to the PD. This prevents the converter circuits from loading the PoE input during detection and classification. The converter circuits discharge C_{IN}, C_{VC}, and C_{VB} while the PD is unpowered. Thus V_{VDD}-V_{RTN} will be a small voltage just after full voltage is applied to the PD, as seen in Figure 22. The PSE drives the PI voltage to the operating range once it has decided to power up the PD. When V_{VDD} rises above the UVLO turnon threshold (V_{UVLO-R}, about 35 V) with RTN high, the TPS23754 device enables the hotswap MOSFET with an approximately 140-mA (inrush) current limit as seen in Figure 24. Converter switching is disabled while C_{IN} charges and V_{RTN} falls from V_{VDD} to nearly V_{VSS}, however the converter start-up circuit is allowed to charge C_{VC} (the bootstrap start-up capacitor). Additional loading applied between V_{VDD} and V_{RTN} during the inrush state may prevent successful PD and subsequent converter start-up. Converter switching is allowed if the PD is not in inrush, OTSD is not active, and the V_C UVLO permits it. Once the inrush current falls about 10% less than the inrush current limit, the PD current limit switches to the operational level (about 970 mA). Continuing the start-up sequence shown in Figure 24, V_{VC} continues to rise until the start-up threshold (V_{CUV}, about 15 V or about 9 V) is exceeded, turning the start-up source off and enabling switching. The V_B regulator is always active, powering the

internal converter circuits as V_{VC} rises. There is a slight delay between the removal of charge current and the start of switching as the soft-start ramp sweeps above the V_{ZDC} threshold. V_{VC} falls as it powers both the internal circuits and the switching MOSFET gates. If the converter control bias output rises to support V_{VC} before it falls to $V_{CUV} – V_{CUVH}$ (about 8.5 V or about 5.5 V), a successful start-up occurs. T2P in Figure 22 (Figure 27, $V_{T2P-OUT}$) becomes active within t_{T2P} from the start of switching, indicating that a type 2 PSE or an adapter is plugged in.

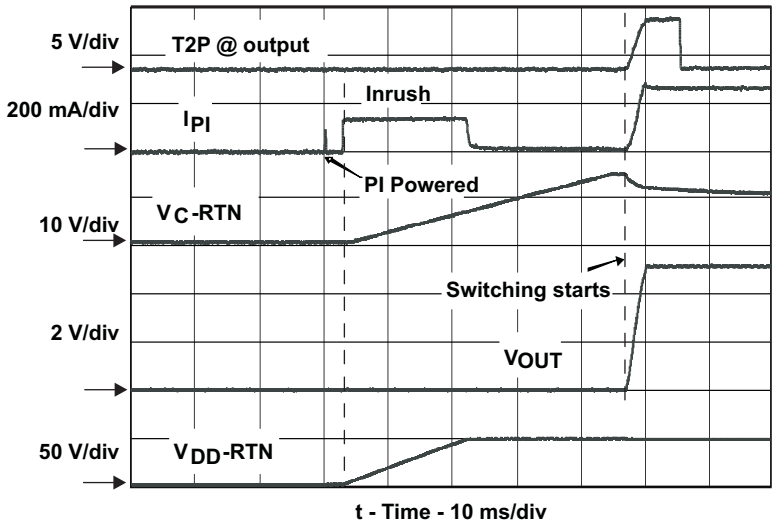


Figure 24. Power Up and Start

If V_{VDD}- V_{VSS} drops below the lower PoE UVLO (V_{UVLO-R} - V_{UVLO-H}, about 30.5 V), the hotswap MOSFET is turned off, but the converter will still run. The converter will stop if V_{VC} falls below the converter UVLO ($V_{CUV} – V_{CUVH}$, about 8.5 V or about 5.5 V), the hotswap is in inrush current limit, 0% duty cycle is demanded by V_{CTL} (V_{CTL} < V_{ZDC}, about 1.5 V), or the converter is in thermal shutdown.

7.4.1.8 PD Hotswap Operation

IEEE 802.3at has taken a new approach to PSE output limiting. A type 2 PSE must meet an output current versus time template with specified minimum and maximum sourcing boundaries. The peak output current may be as high as 50 A for 10 μs or 1.75 A for 75 ms. This makes robust protection of the PD device even more important than it was in IEEE 802.3-2008.

The internal hotswap MOSFET is protected against output faults and input voltage steps with a current limit and deglitched (time-delay filtered) foldback. An overload on the pass MOSFET engages the current limit, with V_{RTN}-V_{VSS} rising as a result. If V_{RTN} rises above about 12 V for longer than about 400 μs, the current limit reverts to the inrush value, and turns the converter off. The 400 μs deglitch feature prevents momentary transients from causing a PD reset, provided that recovery lies within the bounds of the hotswap and PSE protection. Figure 25 shows an example of recovery from a 16 V PSE rising voltage step. The hotswap MOSFET goes into current limit, overshooting to a relatively low current, recovers to about 950-mA full current limit, and charges the input capacitor while the converter continues to run. The MOSFET did not go into foldback because V_{RTN}-V_{VSS} was less than 12 V after the 400 μs deglitch.

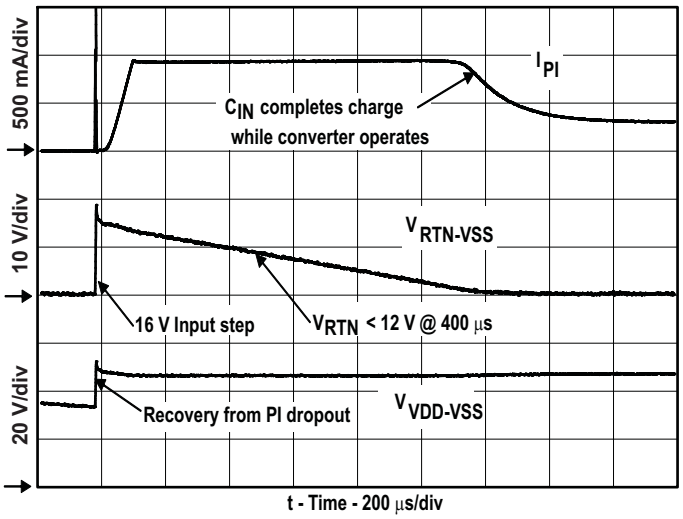


Figure 25. Response to PSE Step Voltage

The PD control has a thermal sensor that protects the internal hotswap MOSFET. Conditions like start-up or operation into a V_{DD} to RTN short cause high power dissipation in the MOSFET. An overtemperature shutdown (OTSD) turns off the hotswap MOSFET and class regulator, which are restarted after the device cools. The hotswap MOSFET will be re-enabled with the inrush current limit when exiting from an overtemperature event.

Pulling DEN to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off. This feature allows a PD with Option three ORing per Figure 26 to achieve adapter priority. Take care with synchronous converter topologies that can deliver power in both directions.

The hotswap switch will be forced off under the following conditions:

1. V_{APD} above V_{APDEN} (about 1.5 V)
2. $V_{DEN} < V_{PD-DIS}$ when $V_{VDD} – V_{VSS}$ is in the operational range
3. PD over-temperature
4. $(V_{VDD} – V_{VSS}) <$ PoE UVLO (about 30.5 V)

7.4.1.9 Converter Controller Features

The TPS23754 DC-DC controller implements a typical current-mode control as shown in the *Functional Block Diagram*. Features include oscillator, overcurrent and PWM comparators, current-sense blanker, dead-time control, soft start, and gate driver. In addition, an internal slope-compensation ramp generator, frequency synchronization logic, thermal shutdown, and start-up current source with control are provided.

The TPS23754 is optimized for isolated converters, and does not provide an internal error amplifier. Instead, the optocoupler feedback is directly fed to the CTL pin which serves as a current-demand control for the PWM. There is an offset of V_{ZDC} (about 1.5 V) and 2:1 resistor divider between the CTL pin and the PWM. A V_{CTL} below V_{ZDC} will stop converter switching, while voltages above $(V_{ZDC} + (2 \times V_{CSMAX}))$ will not increase the requested peak current in the switching MOSFET. Optocoupler biasing design is eased by this limited control range.

7.4.1.10 Bootstrap Topology

The internal start-up current source and control logic implement a bootstrap-type start-up as discussed in Start-Up and Converter Operation. The start-up current source charges C_{VC} from V_{DD1} when the converter is disabled (either by the PD control or the V_C control) to store enough energy to start the converter. Steady-state operating power must come from a converter (bias winding) output or other source. Loading on V_C and V_B must be minimal while C_{VC} charges, otherwise the converter may never start. The optocoupler will not load V_B when the converter is off for most situations; however take care in ORing topologies where the output is powered when PoE is off.

The converter will shut off when V_C falls below its lower UVLO. This can happen when power is removed from the PD, or during a fault on a converter output rail. When one output is shorted, all the output voltages fall including the one that powers V_C. The control circuit discharges V_C until it hits the lower UVLO and turns off. A restart will initiate, as described in *Start-Up and Converter Operation*, if the converter turns off and there is sufficient V_{DD1} voltage. This type of operation is sometimes referred to as *hiccup mode*, which provides robust output short protection by providing time-average heating reduction of the output rectifier.

The bootstrap control logic disables most of the converter controller circuits except the V_B regulator and internal reference. Both GATE and GAT2 (assuming GAT2 is enabled) will be low when the converter is disabled. FRS, BLNK, and DT will be at ARTN while the V_C UVLO disables the converter. While the converter runs, FRS, BLNK, and DT will be about 1.25 V.

The start-up current source transitions to a resistance as (V_{VDD1} – V_{VC}) falls less than 7 V, but will start the converter from adapters within t_{ST}. The lower test voltage for t_{ST} was chosen based on an assumed adapter tolerance, but is not meant to imply a hard cutoff exists. start-up takes longer and eventually will not occur as V_{DD1} decreases below the test voltage. The bootstrap source provides reliable start-up from widely varying input voltages, and eliminates the continual power loss of external resistors. The start-up current source will not charge above the maximum recommended V_{VC} if the converter is disabled and there is sufficient V_{DD1} to charge higher.

7.4.1.11 Current Slope Compensation and Current Limit

Current-mode control requires the addition of a compensation ramp to the sensed inductive (transformer or inductor) current for stability at duty cycles near and over 50%. The TPS23754 device has a maximum duty cycle limit of 78%, permitting the design of wide input-range flyback and active clamp converters with a lower voltage stress on the output rectifiers. While the maximum duty cycle is 78%, converters may be designed that run at duty cycles well below this for a narrower, 36-V to 57-V PI range. The TPS23754 device provides a fixed internal compensation ramp that suffices for most applications.

The TPS23754 device provides internal, frequency independent, slope compensation (150 mV, V_{SLOPE}) to the PWM comparator input for current-mode control-loop stability. This voltage is not applied to the current limit comparator whose threshold is 0.55 V (V_{CSMAX}). If the provided slope is not sufficient, the effective slope may be increased by addition of R_S per Figure 31. The additional slope voltage is provided by (I_{SL-EX} × R_S). There is also a small DC offset caused by the about 2.5-μA pin current. The peak current limit does not have duty cycle dependency unless R_S is used. This makes it easier to design the current limit to a fixed value. See *Current Slope Compensation* for more information.

The internal comparators monitoring CS are isolated from the IC pin by the blanking circuits while GATE is low, and for a short time (blanking period) just after GATE switches high. A 440 Ω (maximum) equivalent pulldown on CS is applied while GATE is low.

7.4.1.12 Blanking – R_{BLNK}

The TPS23754 device provides a choice between internal fixed and programmable blanking periods. The blanking period is specified as an increase in the minimum GATE on time over the inherent gate driver and comparator delays. The default period (see the *Electrical Characteristics*) is selected by connecting BLNK to RTN, and the programmable period is set with R_{BLNK}.

The TPS23754 device blanker timing is precise enough that the traditional R-C filters on CS can be eliminated. This avoids current-sense waveform distortion, which tends to get worse at light output loads. There may be some situations or designers that prefer an R-C approach. The TPS23754 device provides a pulldown on CS during the GATE off time to improve sensing when an R-C filter must be used. The CS input signal should be protected from nearby noisy signals like GATE drive and the switching MOSFET drain.

7.4.1.13 Dead Time

The TPS23754 device features two switching MOSFET gate drivers to ease implementation of high-efficiency topologies. Specifically, these include active (primary) clamp topologies and those with synchronous drivers that are hard-driven by the control circuit. In all cases, there is a need to assure that both driven MOSFETs are not on at the same time. The DT pin programs a fixed time period delay between the turnon of one gate driver until the turnon of the next. This feature is an improvement over the repeatability and accuracy of discrete solutions

while eliminating a number of discrete parts on the board. Converter efficiency is easily tuned with this one repeatable adjustment. The programmed dead time is the same for both GATE-to-GAT2 and GAT2-to-GATE transitions. The dead time is triggered from internal signals that are several stages back in the driver to eliminate the effects of gate loading on the period; however, the observed and actual dead-time will be somewhat dependent on the gate loading. The turnoff of GAT2 coincides with the start of the internal clock period.

DT may be used to disable GAT2, which goes to a high-impedance state.

GATE's phase turns the main switch on when it transitions high, and off when it transitions low. GAT2's phase turns the second switch off when it transitions high, and on when it transitions low. Both switches should be off when GAT2 is high and GATE is low. The signal phasing is shown in Figure 1. Many topologies that use secondary-side synchronous rectifiers also use N-Channel MOSFETs driven through a gate-drive transformer. The proper signal phase for these rectifiers may be achieved by inverting the phasing of the secondary winding (swapping the leads). Use of the two gate drives is shown in Figure 27 and Figure 27.

7.4.1.14 FRS and Synchronization

The FRS pin programs the (free-running) oscillator frequency, and may also be used to synchronize the TPS23754 device converter to a higher frequency. The internal oscillator sets the maximum duty cycle at 78% and controls the slope-compensation ramp circuit. Synchronization may be accomplished by applying a short pulse (T_{SYNC}) of magnitude V_{SYNC} to FRS as shown in Figure 30. The synchronization pulse terminates the potential on-time period, and the off-time period does not begin until the pulse terminates.

7.4.1.15 T2P, Start-Up, and Power Management

T2P (type 2 PSE) is an active-low multifunction pin that indicates if

$$[(\text{PSE} = \text{Type\_2}) + (1.5\ \text{V} < V_{APD}) + (1.55\ \text{V} < V_{PPD} < 8.3\ \text{V})] \times (V_{CTL} < 4\ \text{V}) \times (\text{pd current limit} \neq \text{Inrush}).$$

The term with V_{CTL} prevents an optocoupler connected to the secondary-side from loading V_C before the converter is started. The APD and PPD terms allow the PD to operate from an adapter at high-power if a type 2 PSE is not present, assuming the adapter has sufficient capacity. Applications must monitor the state of T2P to detect power source transitions. Transitions could occur when a local power supply is added or dropped or when a PSE is enabled on the far end. The PD may be required to adjust the load appropriately. The usage of T2P is demonstrated in Figure 27.

For a type 2 PD to operate at less than 13 W the first 80 ms after power application, the various delays must be estimated and used by the application controller to meet the requirement. The bootup time of many applications processors may be long enough to eliminate the need to do any timing.

7.4.1.16 Thermal Shutdown

The DC-DC controller has an OTSD that can be triggered by heat sources including the V_B regulator, GATE driver, bootstrap current source, and bias currents. The controller OTSD turns off V_B, the GATE driver, and forces the V_C control into an undervoltage state.

7.4.1.17 Adapter ORing

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used if PoE is not available in a particular installation. While most applications only require that the PD operate when both sources are present, the TPS23754 device supports forced operation from either of the power sources. Figure 26 illustrates three options for diode ORing external power into a PD. Only one option would be used in any particular design. Option 1 applies power to the TPS23754 device PoE input, option 2 applies power between the TPS23754 device PoE section and the power circuit, and option 3 applies power to the output side of the converter. Each of these options has advantages and disadvantages. Many of the basic ORing configurations and discussion contained in application note, *Advanced Adapter ORing Solutions using the TPS23753* (SLVA306), apply to the TPS23754 device.

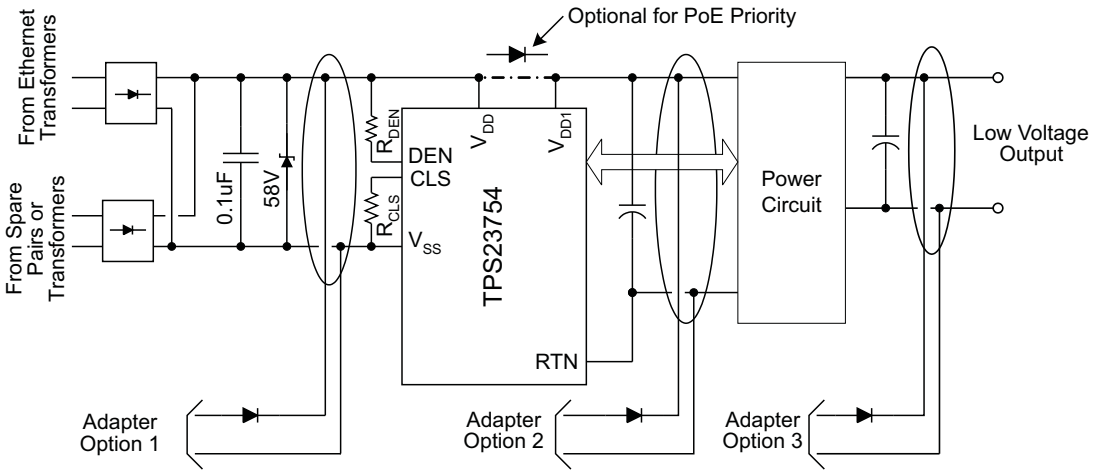


Figure 26. ORing Configurations

The IEEE standards require that the Ethernet cable be isolated from ground and all other system potentials. The adapter must meet a minimum 1500 Vac dielectric withstand test between the output and all other connections for ORing options 1 and 2. The adapter only needs this isolation for option 3 if it is not provided by the converter.

Adapter ORing diodes are shown for all the options to protect against a reverse voltage adapter, a short on the adapter input pins, and damage to a low-voltage adapter. ORing is sometimes accomplished with a MOSFET in option 3.

7.4.1.18 PPD ORing Features

The TPS23754 device provides several additional features to ease ORing based on the multifunction PPD pin (not available on TPS23754-1 device). These include T2P signaling of an option 1 adapter, use of a 24-V adapter (reduced output power) for option 1, and use of PoE as a power backup in conjunction with option 2. See the *Advanced ORing Techniques*.

7.4.1.19 Using DEN to Disable PoE

The DEN pin may be used to turn the PoE hotswap switch OFF by pulling it to V_{SS} while in the operational state, or to prevent detection when in the idle state. A low on DEN forces the hotswap MOSFET OFF during normal operation. Additional information is available in the *Advanced Adapter ORing Solutions using the TPS23753* (SLVA306) application report.

7.4.1.20 ORing Challenges

Preference of one power source presents a number of challenges. Combinations of adapter output voltage (nominal and tolerance), power insertion point, and which source is preferred determine solution complexity. Several factors adding to the complexity are the natural high-voltage selection of diode ORing (the simplest method of combining sources), the current limit implicit in the PSE, and PD inrush and protection circuits (necessary for operation and reliability). Creating simple and seamless solutions is difficult if not impossible for many of the combinations. However, the TPS23754 device offers several built-in features that simplify some combinations.

Several examples will demonstrate the limitations inherent in ORing solutions. Diode ORing, a 48-V adapter with PoE (option 1), presents the problem that either source might be higher. A blocking switch would be required to assure which source was active. A second example is combining a 12-V adapter with PoE using option 2. The converter will draw approximately four times the current at 12 V from the adapter than it does from PoE at 48 V. Transition from adapter power to PoE may demand more current than can be supplied by the PSE. The converter must be turned off while C_{IN} capacitance charges, with a subsequent converter restart at the higher voltage and lower input current. A third example is use of a 12-V adapter with ORing option 1. The PD hotswap would have to handle four times the current, and have 1/16 the resistance (be 16 times larger) to dissipate equal power. A fourth example is that MPS is lost when running from the adapter, causing the PSE to remove power from the PD. If AC power is then lost, the PD will stop operating until the PSE detects and powers the PD.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS23754 device will support many power supply topologies that require a single PWM gate drive or two complementary gate drives and will operate with current-mode control. Figure 27 provides an example of an active clamp forward converter that uses the second gate driver to control M2, the active element in the clamp. GAT2 may also be used to drive a synchronous rectifier as demonstrated in Figure 27. The TPS23754 may be used in topologies that do not require GAT2, which may be disabled to reduce its idling loss.

8.2 Typical Application

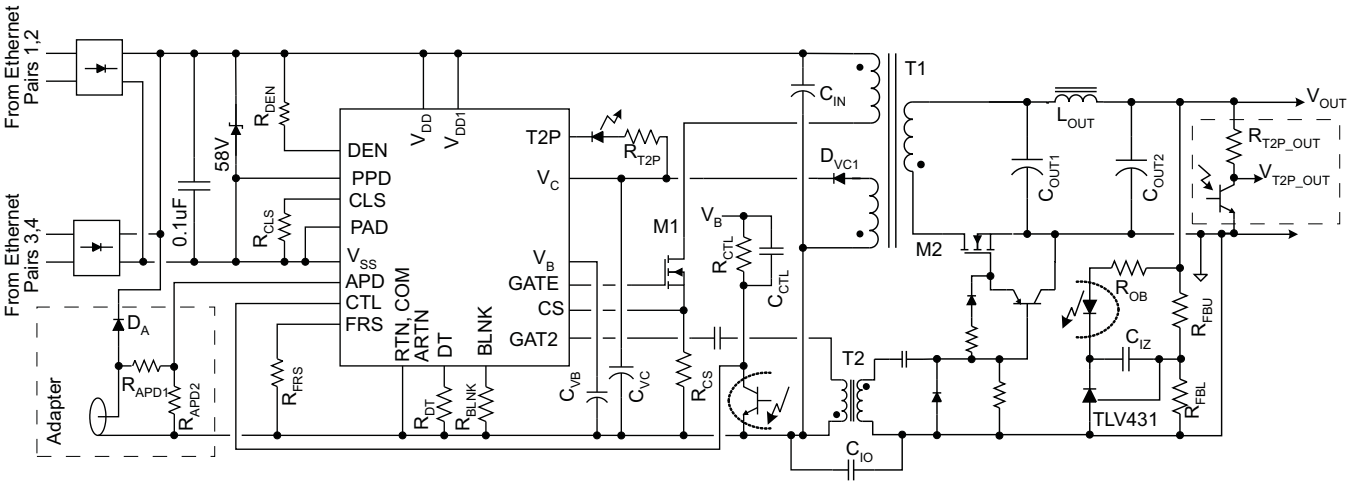


Figure 27. Driven Synchronous Flyback

8.2.1 Design Requirements

Selecting a converter topology along with a design procedure is beyond the scope of this applications section. Examples to help in programming the TPS23754 are shown in *器件和文档支持*. Additional special topics are included to explain the ORing capabilities, frequency dithering, and other design considerations.

8.2.2 Detailed Design Procedure

8.2.2.1 Input Bridges and Schottky Diodes

Using Schottky diodes instead of PN junction diodes for the PoE input bridges and D_{VDD} will reduce the loss of this function by about 30%. However, there are some things to consider when using them.

The IEEE standard specifies a maximum backfeed voltage of 2.8 V. A 100-kΩ resistor is placed between the unpowered pairs and the voltage is measured across the resistor. Schottky diodes often have a higher reverse leakage current than PN diodes, making this a harder requirement to meet. Use conservative design for diode operating temperature, select lower-leakage devices where possible, and match leakage and temperatures by using packaged bridges to help with this.

Schottky diode leakage current and lower dynamic resistance can impact the detection signature. Setting reasonable expectations for the temperature range over which the detection signature is accurate is the simplest solution. Increasing R_{DEN} slightly may also help meet the requirement.

Typical Application (continued)

Schottky diodes have proven less robust to the stresses of ESD transients, failing as a short or becoming leaky. Take care to provide adequate protection in line with the exposure levels. This protection may be as simple as ferrite beads and capacitors.

A general recommendation for the input rectifiers are 1 A or 2 A, 100-V rated discrete or bridge diodes.

8.2.2.2 Protection, D1

A TVS, D_1, across the rectified PoE voltage per Figure 28 must be used. TI recommends a SMAJ58A, or a part with equal to or better performance, for general indoor applications. If an adapter is connected from V_{DD1} to RTN, as in ORing option 2 above, voltage transients caused by the input cable inductance ringing with the internal PD capacitance can occur. Adequate capacitive filtering or a TVS must limit this voltage to be within the absolute maximum ratings. Outdoor transient levels or special applications require additional protection.

Use of diode D_{VDD} for PoE priority may dictate the use of additional protection around the TPS23754. ESD events between the PD power inputs, or the inputs and converter output, cause large stresses in the hotswap MOSFET if D_{VDD} becomes reverse biased and transient current around the TPS23754 is blocked. The use of C_{VDD} and D_{RTN} in Figure 28 provides additional protection should over-stress of the TPS23754 device be an issue. A SMAJ58A would be a good initial selection for D_{RTN}. Individual designs may have to tune the value of C_{VDD}.

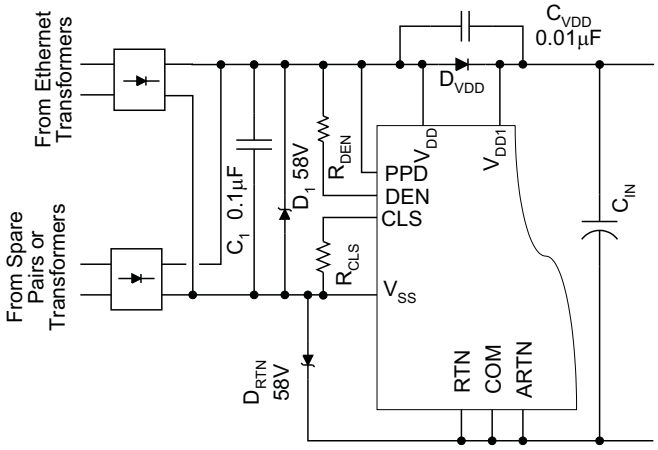


Figure 28. Example of Added ESD Protection for PoE Priority

8.2.2.3 Capacitor, C_1

The IEEE 802.3at standard specifies an input bypass capacitor (from V_{DD} to V_{SS}) of 0.05 µF to 0.12 µF. Typically a 0.1-µF, 100-V, 10% ceramic capacitor is used.

8.2.2.4 Detection Resistor, R_{DEN}

The IEEE 802.3at standard specifies a detection signature resistance, R_{DEN} from 23.7 kΩ to 26.3 kΩ, or 25 kΩ ± 5%. Choose an R_{DEN} of 24.9 kΩ.

8.2.2.5 Classification Resistor, R_{CLS}

Connect a resistor from CLS to V_{SS} to program the classification current according to the IEEE 802.3at standard. The class power assigned should correspond to the maximum average power drawn by the PD during operation. Select R_{CLS} according to Table 1.

For a high-power design, choose class 4 and R_{CLS} = 63.4 Ω.

Typical Application (continued)

8.2.2.6 Dead Time Resistor, R_{DT}

The required dead-time period depends on the specific topology and parasitics. The easiest technique to obtain the optimum timing resistor is to build the supply and tune the dead time to achieve the best efficiency after considering all corners of operation (load, input voltage, and temperature). A good initial value is 100 ns. Program the dead time with a resistor connected from DT to ARTN per Equation 3.

1. Choose R_{DT} as follows assuming a t_{DT} of 100 ns:
   a. $$R_{DT}(k\Omega) = \frac{t_{DT}(ns)}{2} = \frac{100}{2} = 50$$
   b. Choose R_{DT} = 49.9 kΩ

8.2.2.7 Switching Transformer Considerations and R_{VC}

Care in design of the transformer and V_C bias circuit is required to obtain hiccup overload protection. Leading-edge voltage overshoot on the bias winding may cause V_C to peak-charge, preventing the expected tracking with output voltage. Some method of controlling this is usually required. This may be as simple as a series resistor, or an R-C filter in front of D_{VC1}. Good transformer bias-to-output-winding coupling results in reduced overshoot and better voltage tracking.

R_{VC} as shown in Figure 29 helps to reduce peak charging from the bias winding. This becomes especially important when tuning hiccup mode operation during output overload. Typical values for R_{VC} will be from 10 Ω to 100 Ω.

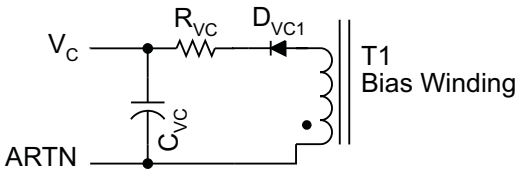


Figure 29. R_{VC} Usage

8.2.2.8 Special Switching MOSFET Considerations

Special care must be used in selecting the converter switching MOSFET. The TPS23756 minimum switching MOSFET V_{GATE} is about 5.5 V, which is due to the V_C lower threshold. This will occur during an output overload, or toward the end of a (failed) bootstrap start-up. The MOSFET must be able to carry the anticipated peak fault current at this gate voltage.

8.2.2.9 Thermal Considerations and OTSD

Sources of nearby local PCB heating should be considered during the thermal design. Typical calculations assume that the TPS23754 device is the only heat source contributing to the PCB temperature rise. It is possible for a normally operating TPS23754 device to experience an OTSD event if it is excessively heated by a nearby device.

8.2.2.10 APD Pin Divider Network, R_{APD1}, R_{APD2}

The APD pin can be used to disable the TPS23754 device internal hotswap MOSFET giving the adapter source priority over the PoE source. An example calculation is provided, see SLVA306.

8.2.2.11 PPD Pin Divider Network, R_{PPD1}, R_{PPD2}

The PPD pin can be used to override the internal hotswap MOSFET UVLO (V_{UVLO_R} and V_{UVLO_H}) when using low voltage adapters connected between V_{DD} and V_{SS}. The PPD pin has an internal 5-µA pulldown current source. As an example, consider the choice of R_{PPD1} and R_{PPD2}, for a 24-V adapter.

1. Select the start-up voltage, $V_{ADPTR\text{-}ON}$ approximately 75% of nominal for a 24-V adapter. Assuming that the adapter output is 24 V ± 10%, this provides 15% margin below the minimum adapter operating voltage.
2. Choose $V_{ADPTR\text{-}ON}$ = 24 V × 0.75 = 18 V.
3. Choose R_{PPD2} = 3.01 kΩ.

Typical Application (continued)

4. Calculate R_{PPD1}.
   a. $$R_{PPD1} = \left(\frac{V_{ADPTR\_ON} - V_{PPDEN}}{\frac{V_{PPDEN}}{R_{PPD2}} + I_{PPD}} \right) = \left(\frac{18\ V - 1.55\ V}{\frac{1.55\ V}{3.01\ k\Omega} + 5\ \mu A} \right) = 31.64\ k\Omega$$
   b. Choose R_{PPD1} = 32.4 kΩ.
5. Check PPD turnon and PPD turnoff voltages.
   a. $$V_{ADPTR\_ON} = V_{PPDEN} + \left[R_{PPD1} \times \left(\frac{V_{PPDEN}}{R_{PPD2}} + I_{PPD} \right) \right] = 18.4\ V$$
   b. $$V_{ADPTR\_OFF} = (V_{PPDEN} - V_{PPDH}) + \left[R_{PPD1} \times \left(\frac{(V_{PPDEN} - V_{PPDH})}{R_{PPD2}} + I_{PPD} \right) \right] = 14.75\ V$$
   c. Voltages look acceptable.
6. Check PPD resistor power consumption.
   a. $$P_{RPPD} = \frac{(V_{DD} - V_{SS})^2}{R_{PPD1} + R_{PPD2}} = \frac{(24\ V \times 1.1)^2}{3.01\ k\Omega + 32.4\ k\Omega} = 19.6\ mW$$
   b. Power is acceptable, but resistor values could be increased to reduce the power loss.

   The PPD pin can also be used to modify the internal MOSFET UVLO for use with a lower output voltage PSE (within certain limits). Connect the R_{PPD1} and R_{PPD2} dividers directly between VDD and VSS with the midpoint connected to PPD. For this case and to allow classification, target the minimum PSE OFF voltage (V_{ADPTR_OFF}) > V_{CU_OFF} = 23 V. Then follow the procedure outlined above to select R_{PPD1}, R_{PPD2}, and determine the PSE ON (V_{ADPTR_ON}) and PSE OFF (V_{ADPTR_OFF}) voltages ensuring that PSE OFF > 23 V. Lastly, because the R_{PPD1} and R_{PPD2} divider is in parallel with R_{DEN} during detection, R_{DEN} must be increased such that the equivalent detection resistance is 25 kΩ nominal.

8.2.2.12 Setting Frequency (R_{FRS}) and Synchronization

The converter switching frequency is set by connecting R_{FRS} from the FRS pin to ARTN. The frequency may be set as high as 1 MHz with some loss in programming accuracy as well as converter efficiency. Synchronization at high duty cycles may become more difficult above 500 kHz due to the internal oscillator delays reducing the available on-time. As an example:

1. Assume a desired switching frequency (f_{SW}) of 250 kHz.
2. Compute R_{FRS}:
   a. $$R_{FRS}(k\Omega) = \frac{17250}{f_{SW}(kHz)} = \frac{17250}{250} = 69$$
   b. Select 69.8 kΩ.

The TPS23754 device may be synchronized to an external clock to eliminate beat frequencies from a sampled system, or to place emission spectrum away from an RF input frequency. Synchronization may be accomplished by applying a short pulse (T_{SYNC}) of magnitude V_{SYNC} to FRS as shown in Figure 30. R_{FRS} should be chosen so that the maximum free-running frequency is just below the desired synchronization frequency. The synchronization pulse terminates the potential on-time period, and the off-time period does not begin until the pulse terminates. The pulse at the FRS pin should reach between 2.5 V and V_B, with a minimum width of 22 ns (above 2.5 V) and rise and fall times less than 10 ns. The FRS node should be protected from noise because it is high-impedance. An R_T on the order of 100 Ω in the isolated example reduces noise sensitivity and jitter.

Typical Application (continued)

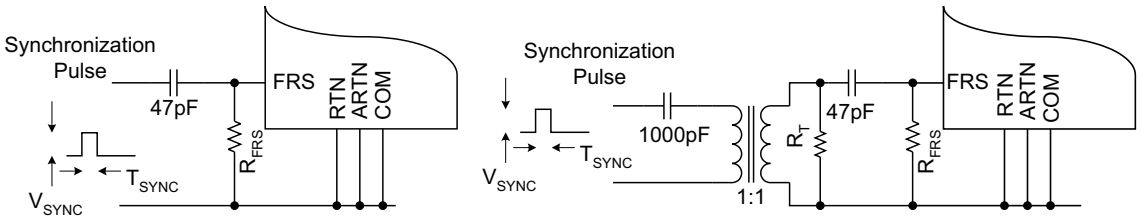


Figure 30. Synchronization

8.2.2.13 Current Slope Compensation

The TPS23754 device provides a fixed internal compensation ramp that suffices for most applications. R_S (see Figure 31) may be used if the internally provided slope compensation is not enough.

Most current-mode control papers and application notes define the slope values in terms of V_{PP} / T_S (peak ramp voltage / switching period). However, the electrical characteristics table specifies the slope peak (V_{SLOPE}) based on the maximum (78%) duty cycle. Assuming that the desired slope, $V_{SLOPE-D}$ (in mV/period), is based on the full period, compute R_S per the following equation where V_{SLOPE}, D_{MAX}, and I_{SL-EX} are from the electrical characteristics table with voltages in mV, current in μA, and the duty cycle is unitless (for example, D_{MAX} = 0.78).

$$R_S(\Omega) = \frac{\left[V_{SLOPE\_D}(mV) - \left(\frac{V_{SLOPE}(mV)}{D_{MAX}}\right)\right]}{I_{SL\_EX}(\mu A)} \times 1000 \quad (6)$$

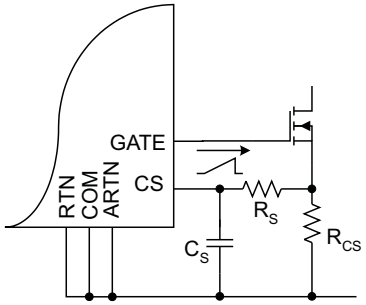


Figure 31. Additional Slope Compensation

C_S may be required if the presence of R_S causes increased noise, due to adjacent signals like the gate drive, to appear at the C_S pin.

8.2.2.14 Blanking Period, R_{BLNK}

Selection of the blanking period is often empirical because it is affected by parasitics and thermal effects of every device between the gate-driver and output capacitors. The minimum blanking period prevents the current limit and PWM comparators from being falsely triggered by the inherent current spike that occurs when the switching MOSFET turns on. The maximum blanking period is bounded by the output rectifier's ability to withstand the currents experienced during a converter output short.

If blanking beyond the internal default is desired choose R_{BLNK} using R_{BLNK} (kΩ) = t_{BLNK} (ns).

1. For a 100 ns blanking interval:
   a. R_{BLNK} (kΩ) = 100
   b. Choose R_{BLNK} = 100 kΩ.

The blanking interval can also be chosen as a percentage of the switching period.

1. Compute R_{BLNK} as follows for 2% blanking interval in a switcher running at 250 kHz.

Typical Application (continued)

a. $$R_{BLNK}(k\Omega) = \frac{Blanking\_Interval(\%)}{f_{SW}(kHz)} \times 10^4 = \frac{2}{250} \times 10^4 = 80$$

b. Select R_{BLNK} = 80.6 kΩ.

8.2.2.15 Estimating Bias Supply Requirements and C_{VC}

The bias supply (V_C) power requirements determine the C_{VC} sizing and frequency of hiccup during a fault. The first step is to determine the power and current requirements of the power supply control, then use this to select C_{VC}. The control current draw will be assumed constant with voltage to simplify the estimate, resulting in an approximate value.

First determine the switching MOSFET gate drive power.

1. Let V_{QG} be the gate voltage swing that the MOSFET Q_G is rated to (often 10 V).

a. $$P_{GATE} = V_C \times f_{SW} \times \left(Q_{GATE} \times \frac{V_C}{V_{QG}}\right) P_{GAT2} = V_C \times f_{SW} \times \left(Q_{GATE2} \times \frac{V_C}{V_{QG}}\right)$$

b. Compute gate drive power if V_C is 12 V, Q_{GATE} is 17 nC, and Q_{GAT2} is 8 nC.

$$P_{GATE} = 12\ V \times 250\ kHz \times 17\ nC \times \frac{12}{10} = 61.2\ mW$$

c. $$P_{GAT2} = 12\ V \times 250\ kHz \times 8\ nC \times \frac{12}{10} = 28.8\ mW$$

P_{DRIVE} = 61.2 mW + 28.8 mW = 90 mW

d. This illustrates why MOSFET Q_G should be an important consideration in selecting the switching MOSFETs.

2. Estimate the required bias current at some intermediate voltage during the C_{VC} discharge. For the TPS23754 device, 12 V provides a reasonable estimate. Add the operating bias current to the gate drive current.

a. $$I_{DRIVE} = \frac{P_{DRIVE}}{V_C} = \frac{90\ mW}{12\ V} = 7.5\ mA$$

b. $I_{TOTAL} = I_{DRIVE} + I_{OPERATING}$ = 7.5 mA + 0.92 mA = 8.42 mA

3. Compute the required C_{VC} based on start-up within the typical soft-start period of 4 ms.

a. $$C_{VC1} + C_{VC2} = \frac{T_{STARTUP} \times I_{TOTAL}}{V_{CUVH}} = \frac{4\ ms \times 8.42\ mA}{6.5\ V} = 5.18\ \mu F$$

b. For this case, a standard 10-μF electrolytic plus a 0.47 μF should be sufficient.

4. Compute the initial time to start the converter when operating from PoE.

a. Using a typical bootstrap current of 4 mA, compute the time to start-up.

b. $$T_{ST} = \frac{C_{VC1} \times V_{CUV}}{I_{VC}} = \frac{10.47\ \mu F \times 15\ V}{4\ mA} = 39\ ms$$

5. Compute the fault duty cycle and hiccup frequency:

a. $$T_{RECHARGE} = \frac{(C_{VC1} + C_{VC2}) \times V_{CUVH}}{I_{VC}} = \frac{(10\ \mu F + 0.47\ \mu F) \times 6.5\ V}{4\ mA} = 17\ ms$$

b. $$T_{DISCHARGE} = \frac{(C_{VC1} + C_{VC2}) \times V_{CUVH}}{I_{TOTAL}} = \frac{(10\ \mu F + 0.47\ \mu F) \times 6.5V}{8.42\ mA} = 8.08\ ms$$

i. The optocoupler current is 0 mA because the output is in current limit.

ii. Also, it is assumed I_{T2P} is 0 mA.

c. $$\text{Duty Cycle: } D = \frac{T_{DISCHARGE}}{T_{DISCHARGE} + T_{RECHARGE}} = \frac{8.08\ ms}{8.08\ ms + 17\ ms} = 32\%$$

Typical Application (continued)

d. Hiccup Frequency: $F = \frac{1}{T_{DISCHARGE} + T_{RECHARGE}} = \frac{1}{8.08\ ms + 17\ ms} = 39.9\ Hz$

6. With the TPS23754 device, the voltage rating of C_{VC1} and C_{VC2} should be 25 V minimum while with the TPS23756 rating can be 16 V.

8.2.2.16 T2P Pin Interface

The T2P pin is an active low, open-drain output indicating a high-power source is available. An optocoupler is typically used to interface with the T2P pin to signal equipment on the secondary side of the converter of T2P status. Optocoupler current-gain is referred to as current transfer ratio (CTR), which is the ratio of transistor collector current to LED current. To preserve efficiency, TI recommends a high-gain optocoupler (250% ≤ CTR ≤ 500%, or 300% ≤ CTR ≤ 600%) along with a high-impedance (for example, CMOS) receiver. Design of the T2P optocoupler interface can be accomplished as follows:

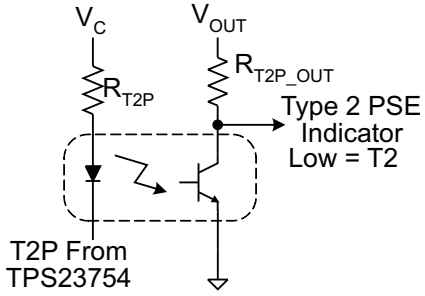


Figure 32. T2P Interface

1. T2P ON characteristic: I_{T2P} = 2 mA minimum, V_{T2P} = 1 V
2. Let V_C = 12 V, V_{OUT} = 5 V, $R_{T2P\text{-}OUT}$ = 10 kΩ, $V_{T2P\text{-}OUT}$ (low) = 400 mV maximum

   a. $I_{RT2P\text{-}OUT} = \frac{V_{OUT} - V_{T2P\text{-}OUT}(low)}{R_{T2P\text{-}OUT}} = \frac{5 - 0.4}{10000} = 0.46\ mA$

3. The optocoupler CTR will be needed to determine R_{T2P}. A device with a minimum CTR of 300% at 5-mA LED bias current is selected. CTR will also vary with temperature and LED bias current. The strong variation of CTR with diode current makes this a problem that requires some iteration using the CTR versus I_{DIODE} curve on the optocoupler data sheet.
   a. Using the (normalized) curves, a current of 0.4 to 0.5 mA is required to support the output current at the minimum CTR at 25°C.
      i. Pick an I_{DIODE}. For example one around the desired load current.
      ii. Use the optocoupler data sheet curve to determine the effective CTR at this operating current. It is usually necessary to apply the normalized curve value to the minimum specified CTR. It might be necessary to ratio or offset the curve readings to obtain a value that is relative to the current that the CTR is specified at.
      iii. If $I_{DIODE} \times CTR_{I\_DIODE}$ is substantially different from I_{RT2P_OUT}, choose another I_{DIODE} and repeat.
   b. This manufacturer's curves also indicate a –20% variation of CTR with temperature. The approximate forward voltage of the optocoupler diode is 1.1 V from the data sheet.

      $I_{RT2P} \cong I_{MIN} \times \frac{100}{100 - \Delta CTR_{TEMP}} = 0.5\ mA \times \frac{100}{100 - 20} = 0.625\ mA$

   c. $V_{FLED} \neq 1.1$ V

      $R_{T2P} = \frac{V_C - V_{T2P} - V_{FLED}}{I_{RT2P}} = \frac{12 - 1 - 1.1}{0.625\ mA} = 15.48\ k\Omega$

   d. Select a 15.4-kΩ resistor. Even though the minimum CTR and temperature variation were considered, the designer might choose a smaller resistor for a little more margin.

Typical Application (continued)

8.2.2.17 Advanced ORing Techniques

See *Advanced Adapter ORing Solutions using the TSP23753*, TI document number SLVA306A for ORing applications that also work with the TPS23754 device. The material in sections *Adapter ORing* and *Protection, D1* are important to consider as well. The following applications are unique to the TPS23754 device with the introduction of PPD.

Option 2 ORing with PoE acting as a hot backup is eased by connecting PPD to V_{DD} per Figure 33. This PPD connection enables the class regulator even when APD is high. The R-Zener network (1.8 kΩ – 24 V) is the simplest circuit that will satisfy MPS requirements, keeping the PSE online. This network may be switched out when the APD is not powered with an optocoupler. This works best with a 48-V adapter and the APD-programmed threshold as high as possible. An example of an adapter priority application with smooth switchover between a 48-V adapter and PoE is shown on the right side of Figure 33. D_{APD} is used to reduce the effective APD hysteresis, allowing the PSE to power the load before V_{VDD1}-V_{RTN} falls too low and causes a hotswap foldback.

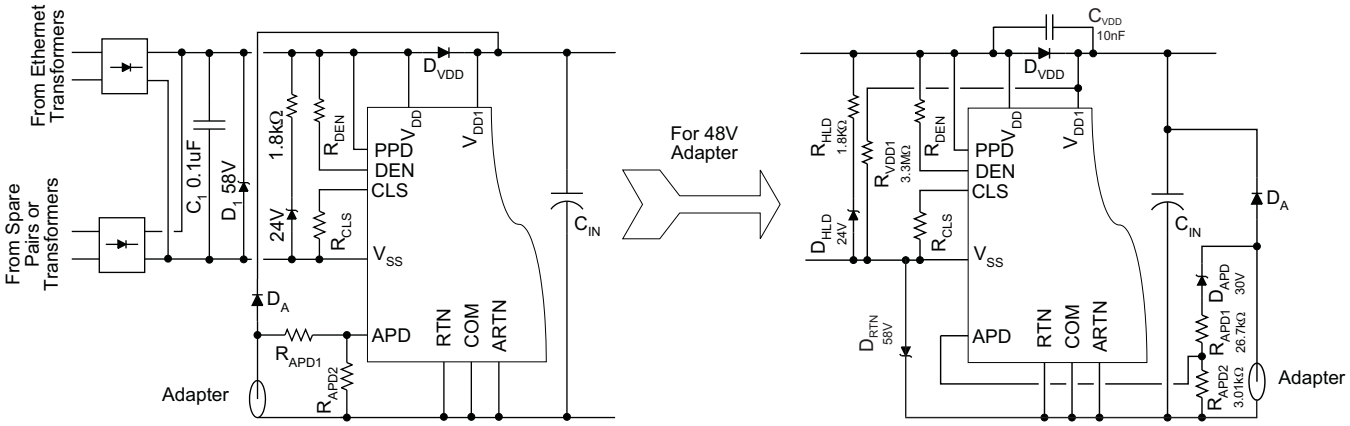


Figure 33. Option 2 PoE Backup ORing

Option 1 ORing of a low voltage adapter (for example, 24 V) is possible by connecting a resistor divider to PPD as in Figure 34. When 1.55 V ≤ V_{PPD} ≤ 8.3 V, the hotswap MOSFET is enabled, T2P is activated, and the class feature is disabled. The hotswap current limit is unaffected, limiting the available power. For example, the maximum input power from a 24-V adapter would be 19.3 W [(24 V – 0.6 V) × 0.825 A].

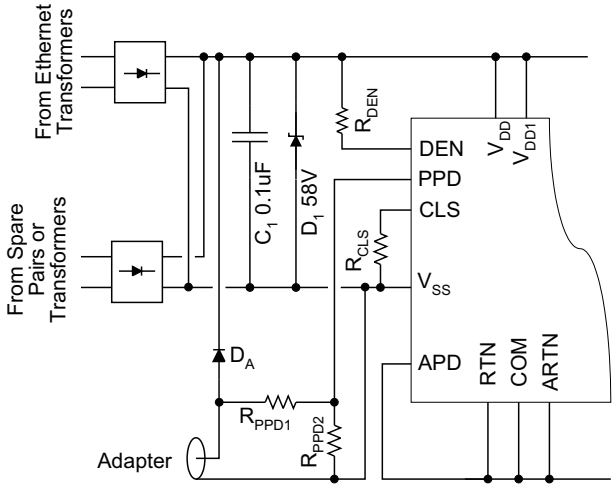


Figure 34. Low-Voltage Option 1 ORing

Typical Application (continued)

8.2.2.18 Soft Start

Converters require a soft start on the voltage error amplifier to prevent output overshoot on start-up. Figure 35 shows a common implementation of a secondary-side soft start that works with the typical TL431 error amplifier. The soft-start components consist of D_{SS}, R_{SS}, and C_{SS}. They serve to control the output rate-of-rise by pulling V_{CTL} down as C_{SS} charges through R_{OB}, the optocoupler, and D_{SS}. This has the added advantage that the TL431 output and C_{IZ} are preset to the proper value as the output voltage reaches the regulated value, preventing voltage overshoot due to the error amplifier recovery. The secondary-side error amplifier will not become active until there is sufficient voltage on the secondary. The TPS23754 device provides a primary-side soft start, which persists long enough (about 4 ms) for secondary side voltage-loop soft start to take over. The primary-side current-loop soft start controls the switching MOSFET peak current by applying a slowly rising ramp voltage to a second PWM control input. The PWM is controlled by the lower of the soft-start ramp or the CTL-derived current demand. The actual output voltage rise time is usually much shorter than the internal soft-start period. Initially the internal soft-start ramp limits the maximum current demand as a function of time. Either the current limit, secondary-side soft start, or output regulation assume control of the PWM before the internal soft-start period is over. Figure 24 shows a smooth handoff between the primary and secondary-side soft start with minimal output voltage overshoot.

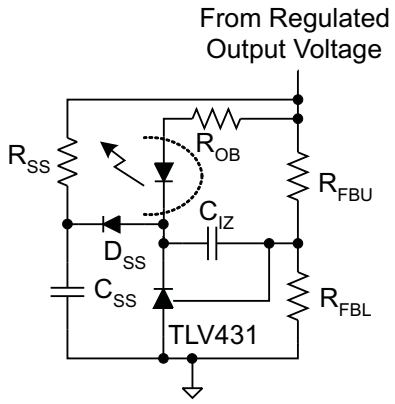


Figure 35. Error Amplifier Soft Start

8.2.2.19 Frequency Dithering for Conducted Emissions Control

The international standard CISPR 22 (and adopted versions) are often used as a requirement for conducted emissions. Ethernet cables are covered as a telecommunication port in section 5.2 for conducted emissions. Meeting EMI requirements is often a challenge, with the lower limits of Class B being especially hard. Circuit board layout, filtering, and snubbing various nodes in the power circuit are the first layer of control techniques. A more detailed discussion of EMI control is presented in *Practical Guidelines to Designing an EMI Compliant PoE Powered Device With Isolated Flyback,* (SLUA469). Additionally, IEEE802.3at sections 33.3 and 33.4 have requirements for noise injected onto the Ethernet cable based on compatibility with data transmission.

Occasionally, a technique referred to as frequency dithering is used to provide additional EMI measurement reduction. The switching frequency is modulated to spread the narrowband individual harmonics across a wider bandwidth, thus lowering peak measurements. The circuit of Figure 36 modulates the switching frequency by feeding a small AC signal into the FRS pin. These values may be adapted to suit individual needs.

Typical Application (continued)

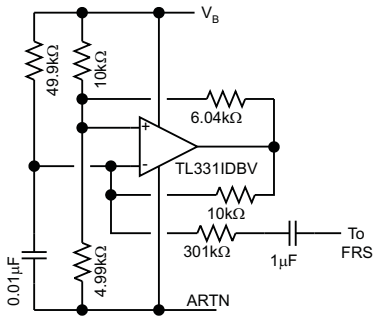


Figure 36. Frequency Dithering

8.2.3 Application Curves

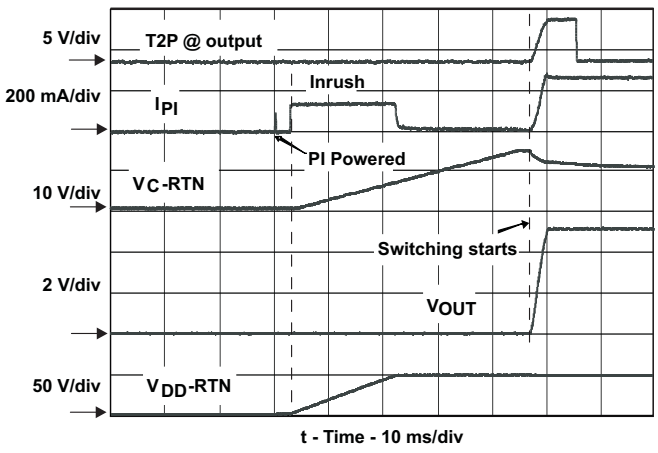


Figure 37. Power Up and Start

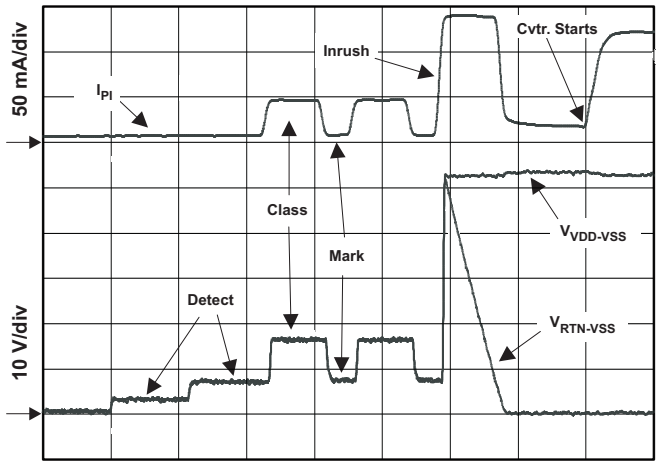


Figure 38. Start-Up

9 Power Supply Recommendations

The TPS23754/TPS23756 converter should be designed such that the input voltage of the converter is capable of operating within the IEEE802.3at recommended input voltage as shown in Table 2 and the minimum operating voltage of the adapter if applicable.

10 Layout

10.1 Layout Guidelines

Printed-circuit-board layout recommendations are provided in the evaluation module (EVM) documentation available for these devices.

10.2 Layout Example

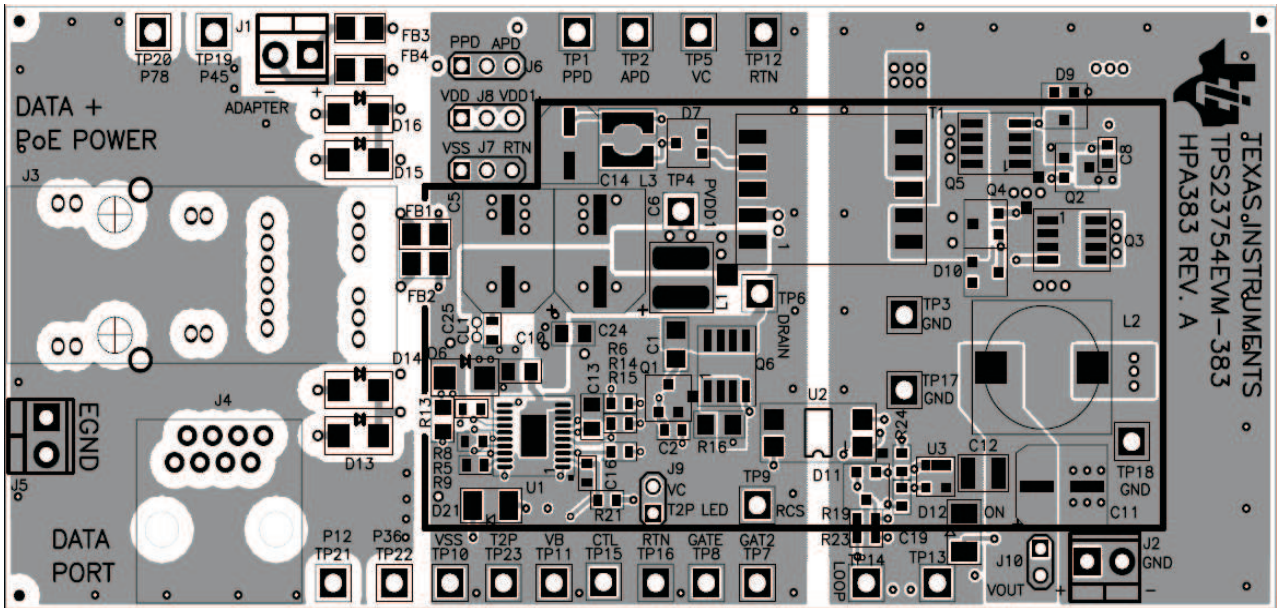


Figure 39. TPS23754EVM-383 EVM Parts Placement and Example Layout

10.3 ESD

The TPS23754 device has been tested to EN61000-4-2 using a power supply based on Figure 27. The levels used were 8-kV contact discharge and 15-kV air discharge. Surges were applied between the PoE input and the DC output, between the adapter input and the DC output, between the adapter and the PoE inputs, and to the DC output with respect to earth. Tests were done both powered and unpowered. No TPS23754 device failures were observed and operation was continuous. See Figure 28 for additional protection for some test configurations.

ESD requirements for a unit that incorporates the TPS23754 have a much broader scope and operational implications than are used in TI's testing. Unit-level requirements should not be confused with reference design testing that only validates the ruggedness of the TPS23754.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

有关更多具体的转换器设计示例，请参阅以下应用手册：

- 《采用 TPS23753 用电器件和电源控制器进行设计》，SLVA305
- 《了解和设计有源钳位电流模式控制的转换器（使用 UCC2897A）》，SLUA535
- 《采用 TPS23753 的高级适配器 ORing 解决方案》，SLVA306
- 《TPS23754EVM-420 EVM：TPS23754 的评估模块》，SLVU301
- 《TPS23754EVM-383 EVM：TPS23754 的评估模块》，SLVU304

11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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11.3 商标

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All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS23754PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS23754	Samples
TPS23754PWP-1	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	23754-1	Samples
TPS23754PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS23754	Samples
TPS23754PWPR-1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	23754-1	Samples
TPS23756PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS23756	Samples
TPS23756PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS23756	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

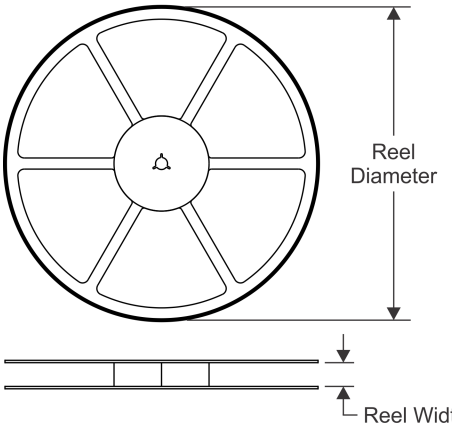
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

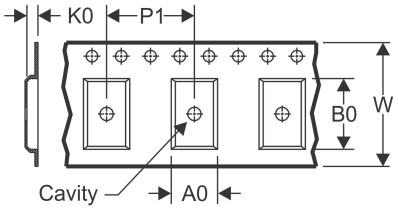
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

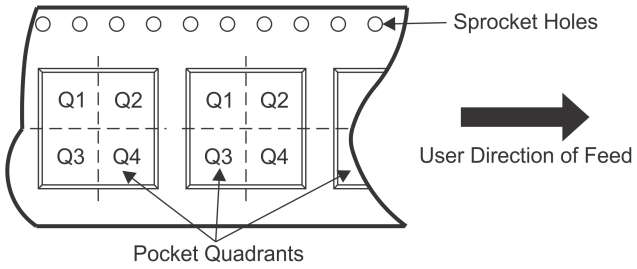


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

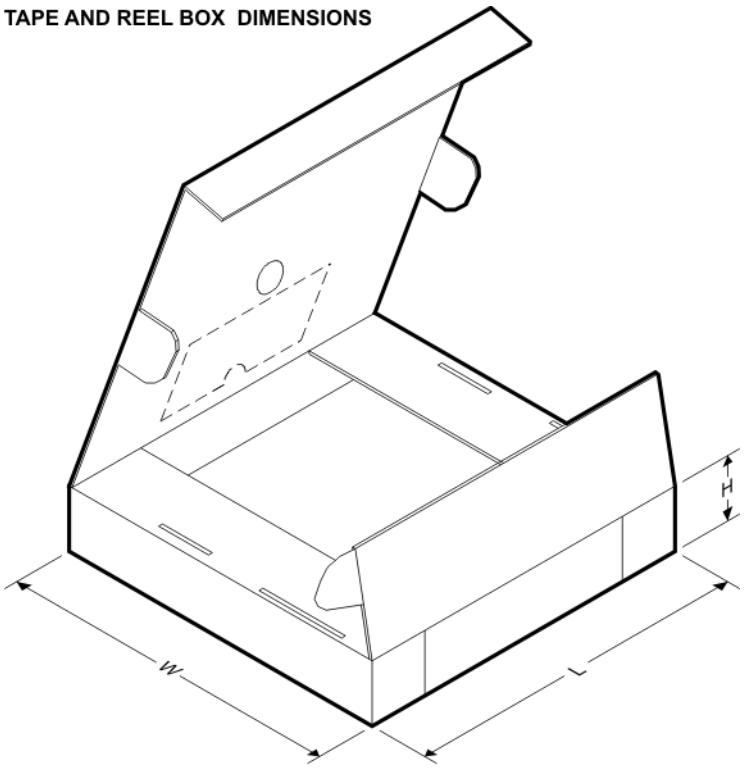
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23754PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS23754PWPR-1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS23756PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

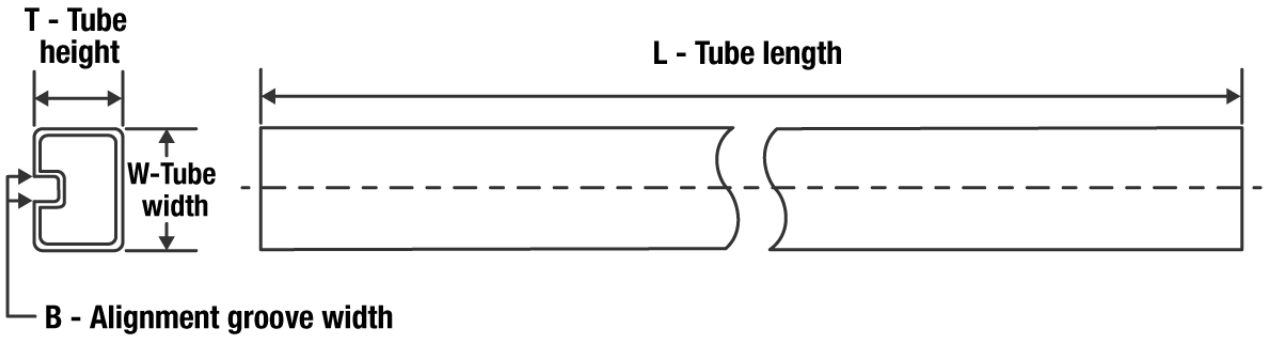
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23754PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS23754PWPR-1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS23756PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

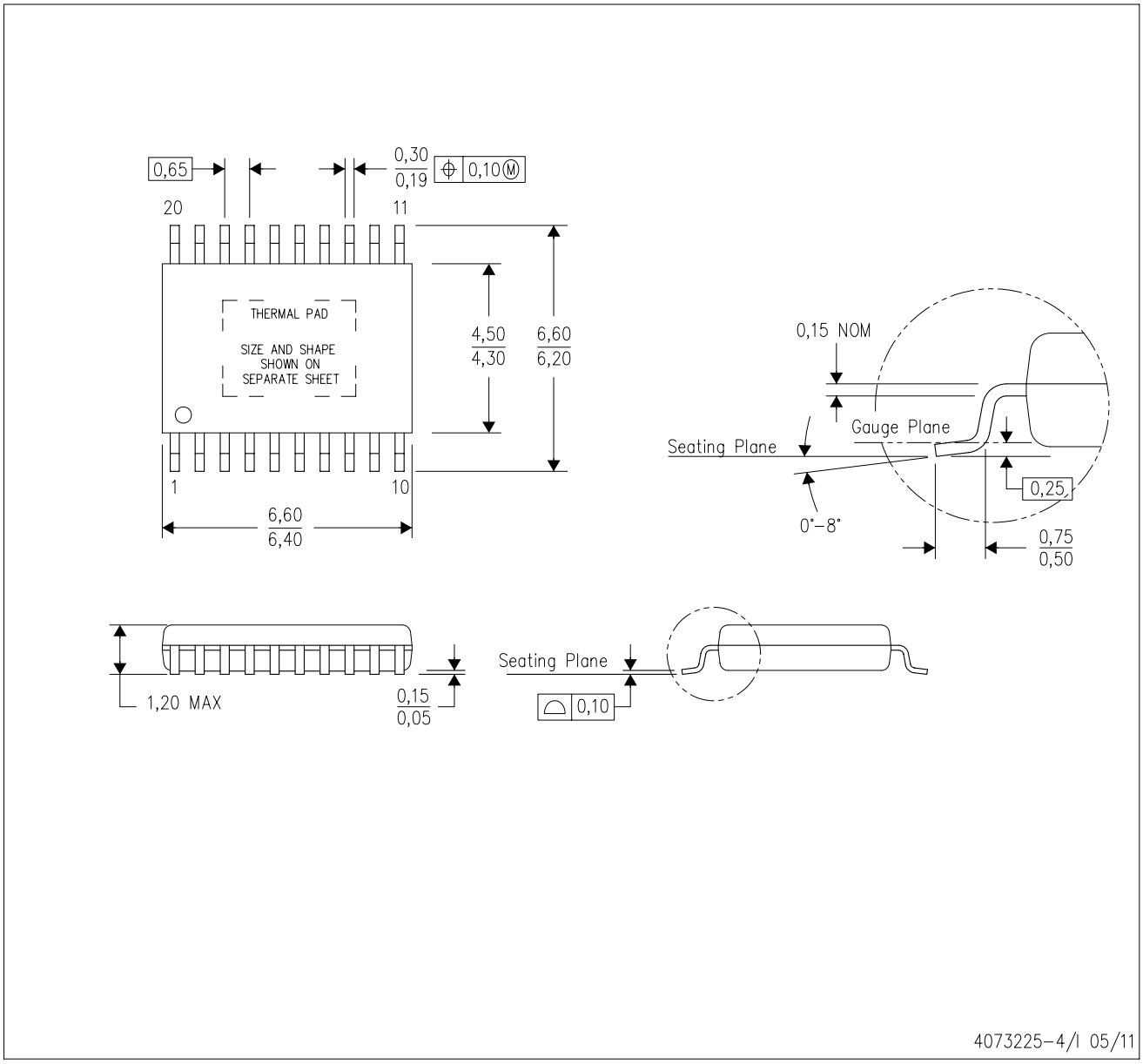
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS23754PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS23754PWP-1	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS23756PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

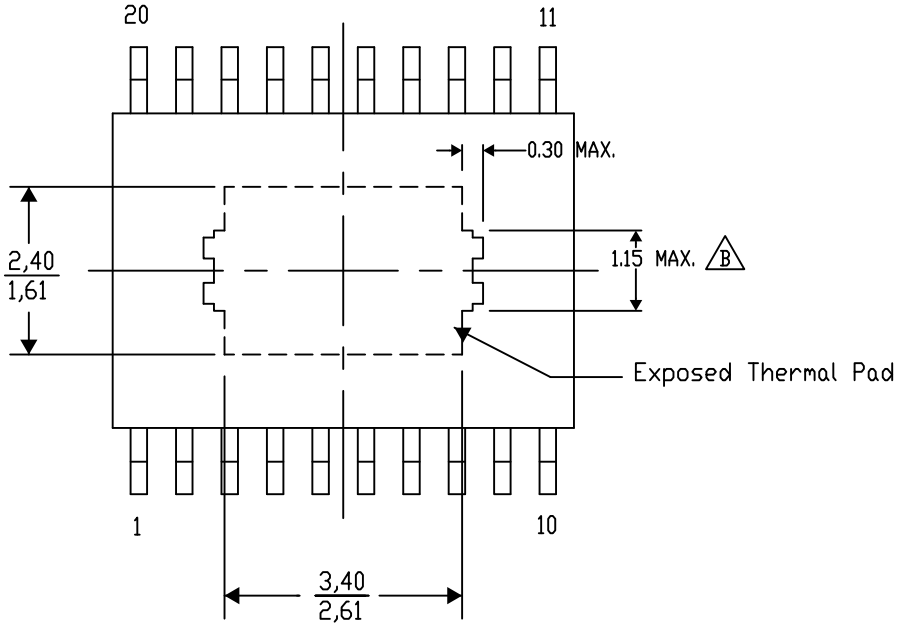
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

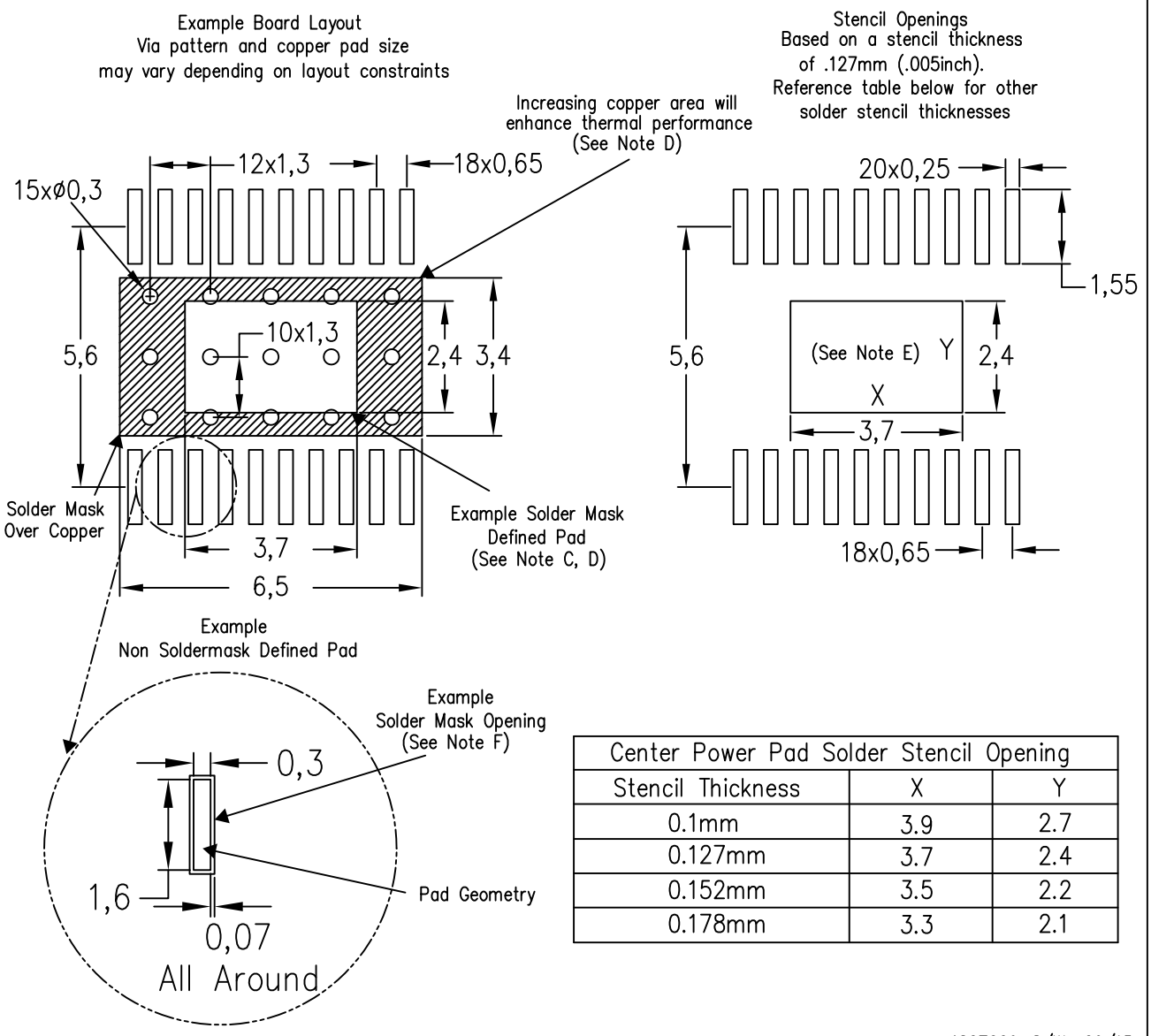
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

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