

Data Lane 2:1 MIPI Switch

Features

- 10-Channel 2:1 Switch
- Signal Types: MIPI, D-PHY & C-PHY
- Supply Voltage Range(V_{CC}): 1.65V to 5.0V
- Input Signals: 0V to 1.3V
- R_{ON} : 7.5 Ω Typical
- ΔR_{ON} : 0.2 Ω Typical
- I_{CC} : 17 μ A Typical
- -3dB Bandwidth: 3.5 GHz Typical
- Low Crosstalk: -30 dB Typical
- Low Off Isolation: -24 dB Typical
- C_{ON} : 1.5 pF Typical

Applications

- Smartphones
- Tablets
- Laptops
- Displays

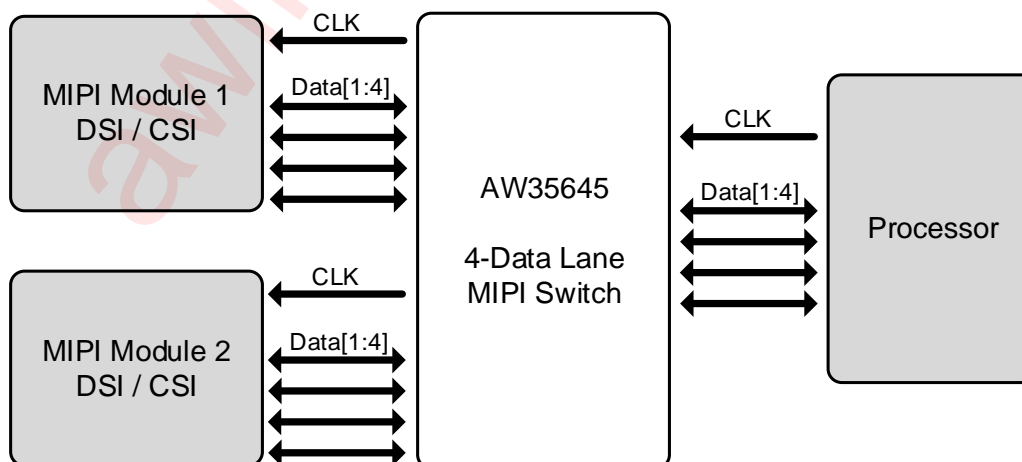
General Description

The AW35645 is a four-data-lane MIPI D-PHY switch. The AW35645 can also be configured as three-data-lane MIPI C-PHY switch.

This 10 channel single-pole double-throw switch is optimized for high speed MIPI applications. The AW35645 is designed to facilitate multiple MIPI compliant devices to connect to a CSI or DSI module.

The AW35645 is available in a FCBGA 2.4mmX2.4mmX0.6mm-36B package.

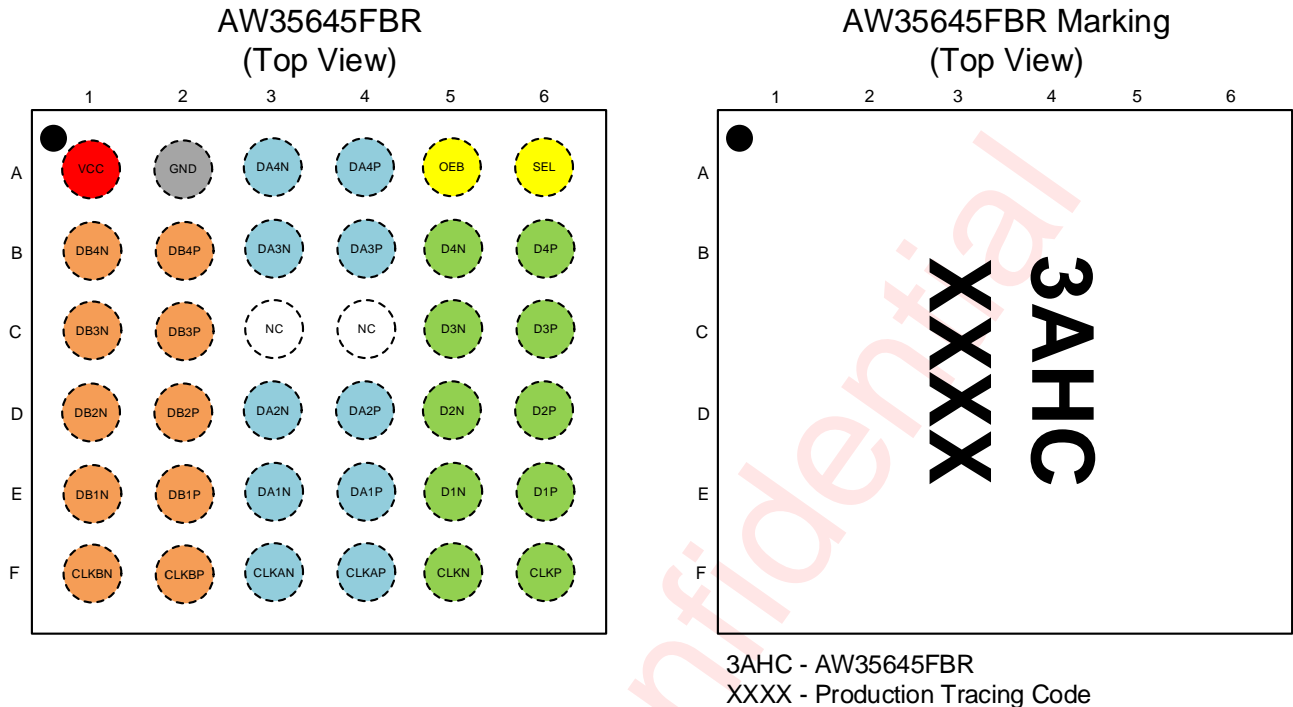
Typical Application Circuit



Typical Application Circuit of AW35645

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Pin Configuration And Top Mark



Pin Configuration and Top Mark

Pin Definition

PIN	NAME	DESCRIPTION
A1	VCC	Power supply input
A2	GND	Ground
A3	DA4N	A side data port 4, differential -
A4	DA4P	A side data port 4, differential +
A5	OEB	Output enable, active low
A6	SEL	Channel select
B1	DB4N	B side data port 4, differential -
B2	DB4P	B side data port 4, differential +
B3	DA3N	A side data port 3, differential -
B4	DA3P	A side data port 3, differential +
B5	D4N	Common data port 4, differential -
B6	D4P	Common data port 4, differential +

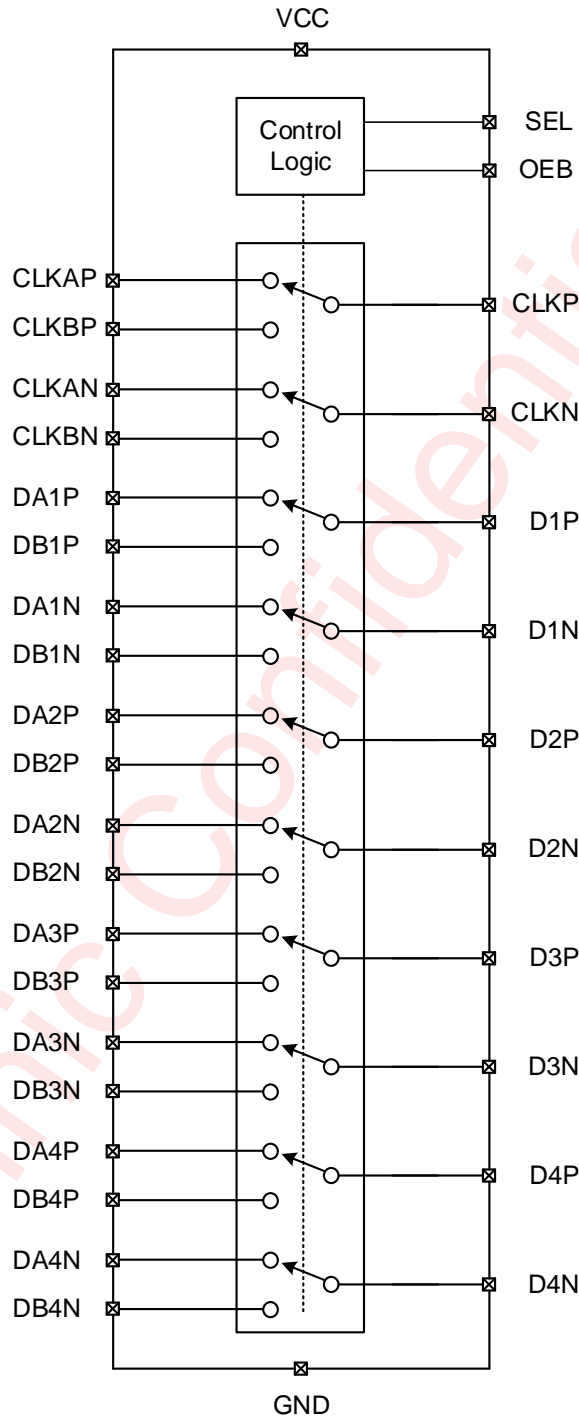
Pin Definition (Continued)

PIN	NAME	DESCRIPTION
C1	DB3N	B side data port 3, differential -
C2	DB3P	B side data port 3, differential +
C3	NC	No connect
C4	NC	No connect
C5	D3N	Common data port 3, differential -
C6	D3P	Common data port 3, differential +
D1	DB2N	B side data port 2, differential -
D2	DB2P	B side data port 2, differential +
D3	DA2N	A side data port 2, differential -
D4	DA2P	A side data port 2, differential +
D5	D2N	Common data port 2, differential -
D6	D2P	Common data port 2, differential +
E1	DB1N	B side data port 1, differential -
E2	DB1P	B side data port 1, differential +
E3	DA1N	A side data port 1, differential -
E4	DA1P	A side data port 1, differential +
E5	D1N	Common data port 1, differential -
E6	D1P	Common data port 1, differential +
F1	CLKBN	B side clock port, differential -
F2	CLKBP	B side clock port, differential +
F3	CLKAN	A side clock port, differential -
F4	CLKAP	A side clock port, differential +
F5	CLKN	Common clock port, differential -
F6	CLKP	Common clock port, differential +

Pin Functions

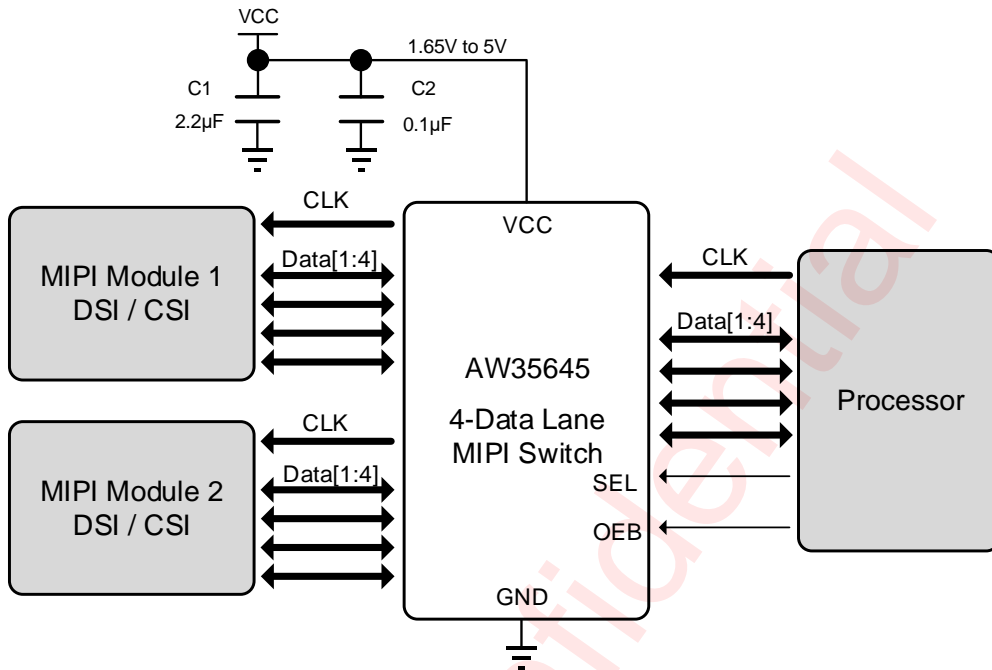
OEB	SEL	Function
H	X	Clock and Data ports High Impedance
L	L	CLKP/N=CLKAP/N, DnP/N=DAnP/N
L	H	CLKP/N=CLKBP/N, DnP/N=DBnP/N

Functional Block Diagram

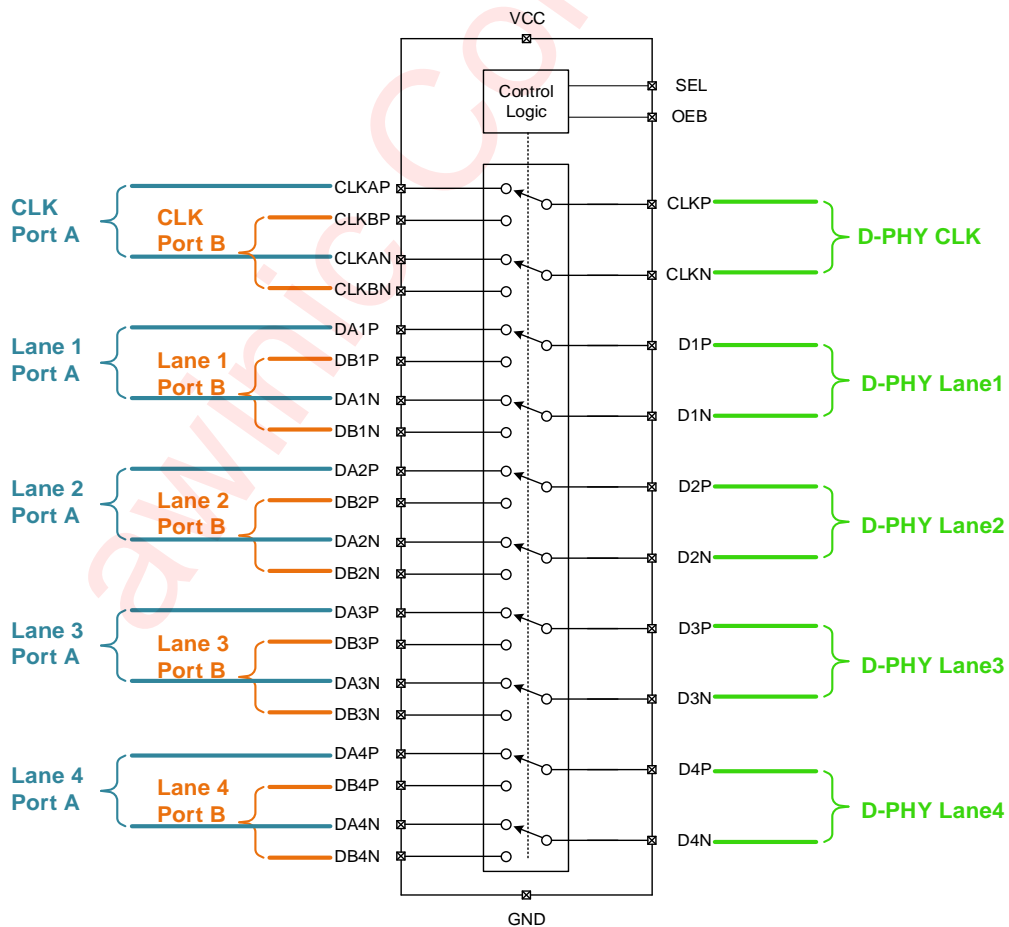


Functional Block Diagram

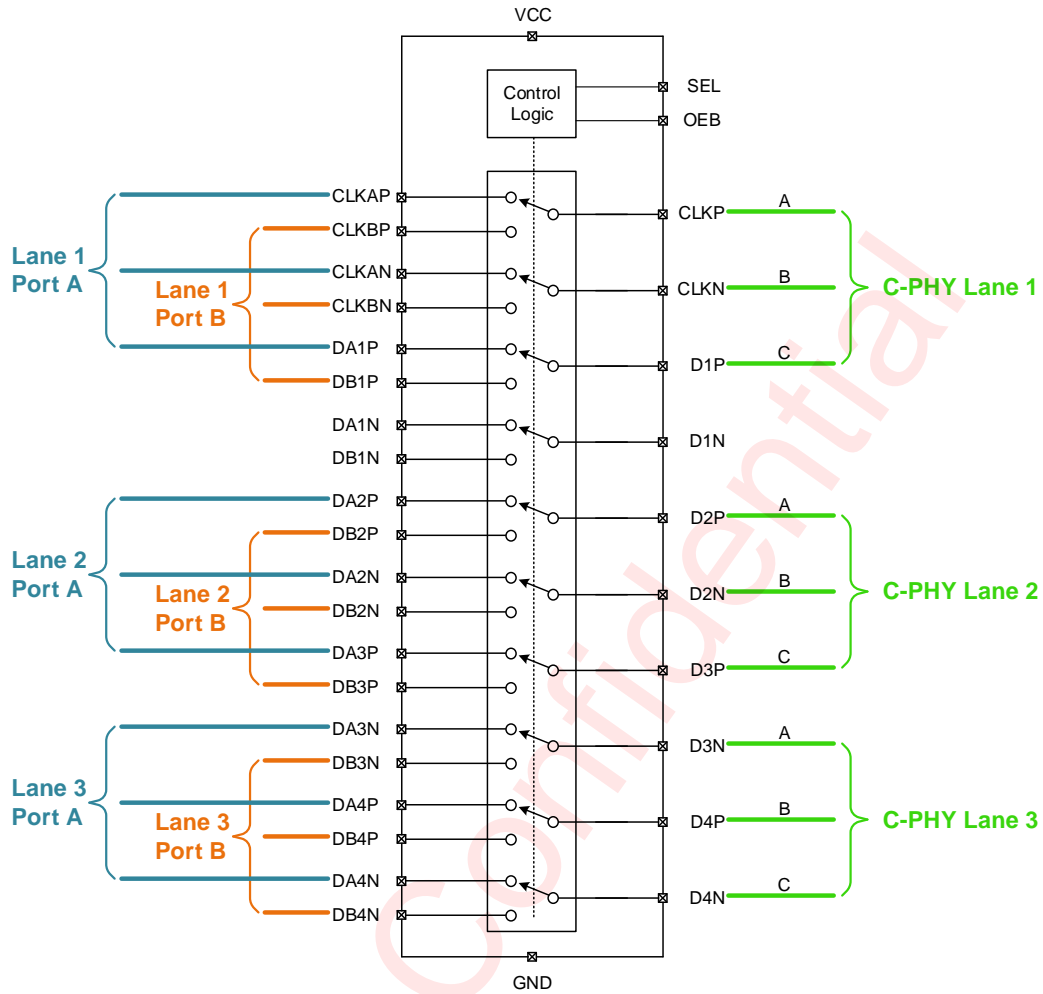
Typical Application Circuits



Typical Application Circuit of AW35645



Recommended D-PHY Configuration of AW35645



Recommended C-PHY Configuration of AW35645

The control inputs OEB,SEL must be held HIGH or LOW, and cannot be left floating

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35645FBR	-40°C~85°C	FCBGA 2.4mmX2.4mmX 0.6mm-36B	3AHC	MSL3	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS	RANGE
Supply voltage range V_{CC}	-0.3V to 6V
Input/Output DC switch voltage $V_{I/O}$ ^(NOTE2)	-0.3V to 6V
Input voltage range	SEL, OEB
Junction-to-ambient thermal resistance θ_{JA}	80°C/W
Maximum operating junction temperature T_{JMAX}	150°C
Operating free-air temperature range	-40°C to 85°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
Human Body Model (All pins, per ESDA/JEDEC JS-001-2017)	±2kV
Charged Device Model (All pins, per ESDA/JEDEC JS-002-2018)	±1kV
Latch-Up	
Test condition: JESD78E	±200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: $V_{I/O}$ refers to analog data/clock switch ports

Electrical Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise noted. Typical values are guaranteed for $V_{CC}=3.3\text{V}$ $T_A = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.3	5.0	V
I_{CC}	Active supply current	OEB=0V, SEL=0V or V_{CC}		17	30	μA
I_{CC_PD}	Standby supply current	OEB= V_{CC} , SEL=0V or V_{CC}			1.2	μA
$I_{CC_PD_1.5}$	Standby supply current	$V_{CC}=5\text{V}$, OEB=1.5V, SEL=0V or V_{CC}		1		μA
DC Characteristics						
R_{ON_HS}	On-state resistance for high speed MIPI mode	$V_{IO}=0.2\text{V}$, $I_{ON}=8\text{mA}$ $V_{CC}=1.65\text{V}$ to 1.8V		7.8	13	Ω
		$V_{IO}=0.2\text{V}$, $I_{ON}=8\text{mA}$ $V_{CC}=1.8\text{V}$ to 5.0V		7.5	13	Ω
R_{ON_LP}	On-state resistance for low power MIPI mode	$V_{IO}=1.2\text{V}$, $I_{ON}=8\text{mA}$ $V_{CC}=1.65\text{V}$ to 1.8V		9.2	14	Ω
		$V_{IO}=1.2\text{V}$, $I_{ON}=8\text{mA}$ $V_{CC}=1.8\text{V}$ to 5.0V		8.3	14	Ω
ΔR_{ON_HS}	On-state resistance match between channels for high speed MIPI mode	$V_{IO}=0.2\text{V}$, $I_{ON}=8\text{mA}$		0.2		Ω
ΔR_{ON_LP}	On-state resistance match between channels for low power MIPI mode	$V_{IO}=1.2\text{V}$, $I_{ON}=8\text{mA}$		0.2		Ω
$R_{ON_FLAT_HS}$	ON-state resistance flatness for high speed MIPI mode	$V_{IO}=0\text{V}$ to 0.3V , $I_{ON}=8\text{mA}$		0.1		Ω
$R_{ON_FLAT_LP}$	ON-state resistance flatness for low power MIPI mode	$V_{IO}=0\text{V}$ to 1.3V , $I_{ON}=8\text{mA}$		0.2		Ω
I_{OFF}	Switch off leakage current	$V_{CC}=1.65\text{V}$ to 5.0V OEB, SEL=0V or 5.0V Dn,CLKn,DAn,CLKAn,DBn, CLKBn=0V to 1.3V	-0.5		0.5	μA
I_{ON}	Switch on leakage current	$V_{CC}=1.65\text{V}$ to 5.0V OEB=0V, SEL=0V or 5.0V Dn,CLKn,DAn,CLKAn,DBn, CLKBn=0V to 1.3V	-0.5		0.5	μA

Electrical Characteristics (Continued)

$T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise noted. Typical values are guaranteed for $V_{CC}=3.3\text{V}$ $T_A = 25^{\circ}\text{C}$.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Digital Characteristics					
V_{IH}	Input logic high (SEL, OEB)	$V_{CC}=1.65\text{V}$ to 5.0V	1.3		V
V_{IL}	Input logic low (SEL, OEB)	$V_{CC}=1.65\text{V}$ to 5.0V		0.5	V
I_{LEAK_IN}	Input leakage (SEL, OEB)	SEL,OEB=0V to 5.0V	-0.5	0.5	μA
C_{IN}	Digital Input capacitance (SEL, OEB)	f=1MHz		5	pF
Dynamic Characteristics					
C_{ON}	ON capacitance ^(NOTE3)	OEB=0V, Dn,CLKn,DAn,DBn,CLKAn, CLKBn=0V or 0.2V f = 750 MHz, switch ON		1.5	pF
C_{OFF}	OFF capacitance ^(NOTE3)	OEB= V_{CC} , Dn,CLKn,DAn,DBn,CLKAn, CLKBn=0V or 0.2V f = 750MHz, switch OFF		1.2	pF
O_{ISO}	Differential off isolation ^(NOTE3)	$R_L = 50\Omega$, $C_L = 0\text{pF}$ $V_{IO}=200\text{mV}+200\text{mV}_{PP}$ (differential) f = 750MHz, switch OFF		-24	dB
X_{TALK}	Differential Channel to channel crosstalk ^(NOTE3)	$R_L = 50\Omega$, $C_L = 0\text{pF}$ $V_{IO}=200\text{mV}+200\text{mV}_{PP}$ (differential) f = 750MHz, switch ON		-30	dB
BW	-3dB bandwidth ^(NOTE3)	$R_L = 50\Omega$, $C_L = 0\text{pF}$ $V_{IO}=200\text{mV}+200\text{mV}_{PP}$ (differential), switch ON	3	3.5	GHz

NOTE3: Guaranteed by characterization

Electrical Characteristics (Continued)

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{CC}=3.3V T_A = 25°C.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
Dynamic Characteristics						
t _{INIT}	Initialization time (V _{CC} to output)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R _L = 50Ω, C _L = 0pF		1.7	200	μs
t _{EN}	Device turn on time (OEB to output)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R _L = 50Ω, C _L = 0pF		1.3	200	μs
t _{DIS}	Device turn off time (OEB to output)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R _L = 50Ω, C _L = 0pF		100	250	ns
t _{ON}	Switch turn on time (SEL to output)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R _L = 50Ω, C _L = 0pF		1200	2500	ns
t _{OFF}	Switch turn off time (SEL to output)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R _L = 50Ω, C _L = 0pF		1000	2000	ns
t _{BBM}	Break before make time	Dn,CLKn: R _L = 50Ω, C _L = 0pF DAn,DBn,CLKAn,CLKBn =0.6V		350		ns
t _{PD}	Propagation delay ^(NOTE4)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R _L = 50Ω, C _L = 0pF		100		ps
t _{SKREW(INTRA)}	Intrapair skew ^(NOTE4)	Dn,CLKn=0.3V DAn,DBn,CLKAn,CLKBn: R _L = 50Ω, C _L = 0pF		6		ps
t _{SKREW(INTER)}	Interpair skew ^(NOTE4)	Dn,CLKn=0.3V DAn,DBn,CLKAn,CLKBn: R _L = 50Ω, C _L = 0pF		6		ps

NOTE4: Guaranteed by characterization

Detailed Functional Description

The AW35645 is a four-data-lane MIPI D-PHY switch. This device is an optimized 10-channel (5 differential) single-pole, double-throw switch for use in high speed applications. The AW35645 can also be configured as three-data-lane MIPI C-PHY switch. The AW35645 is designed to facilitate multiple MIPI compliant devices to connect to a single CSI/DSI, C-PHY/D-PHY module.

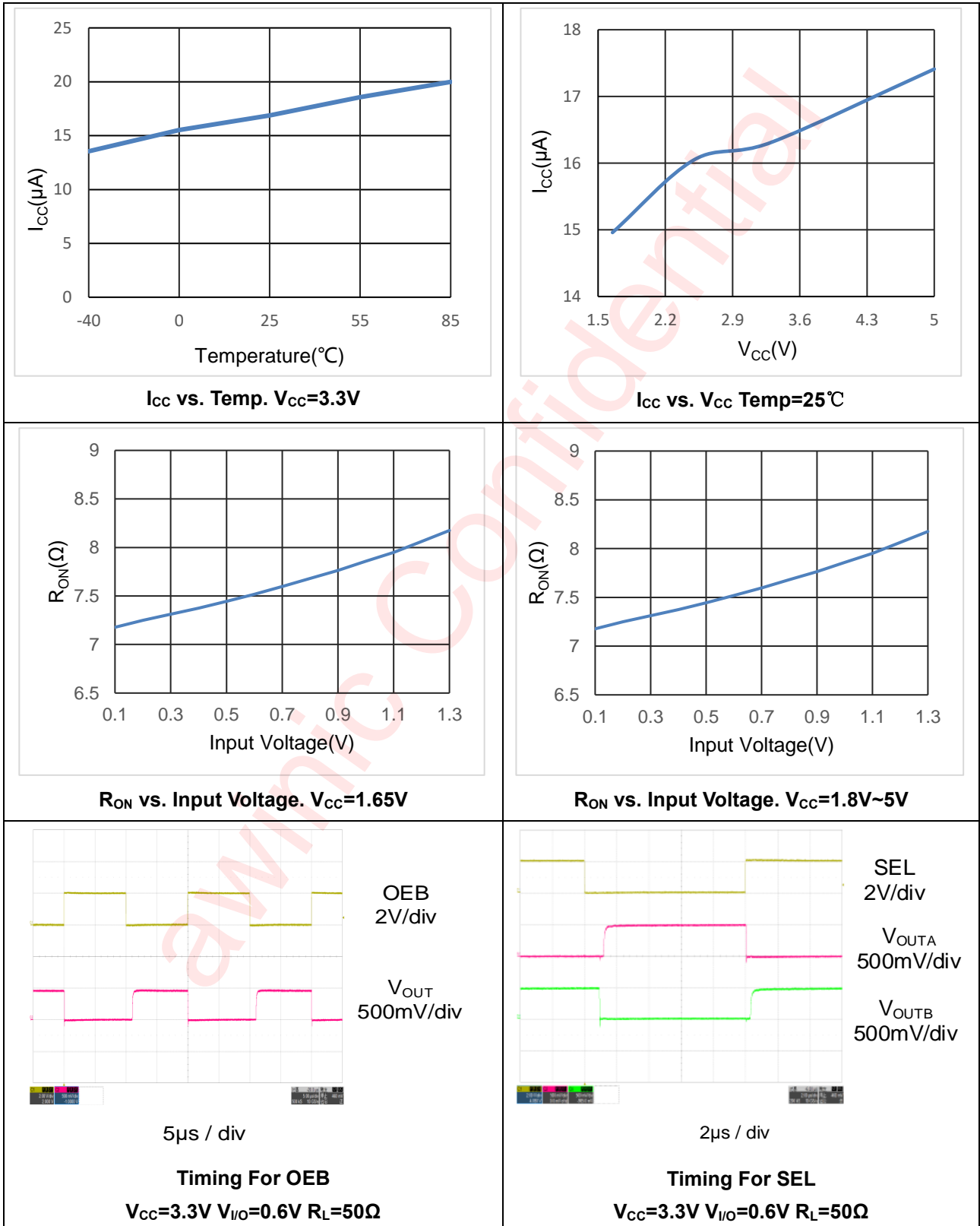
High Impedance Mode

When OEB is logic high, the AW35645 is in high impedance mode, all the clock and data ports are in Hi-Z state.

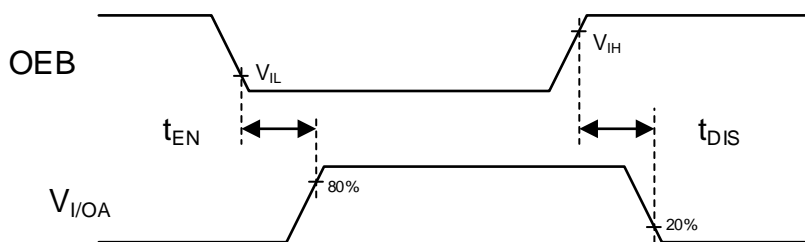
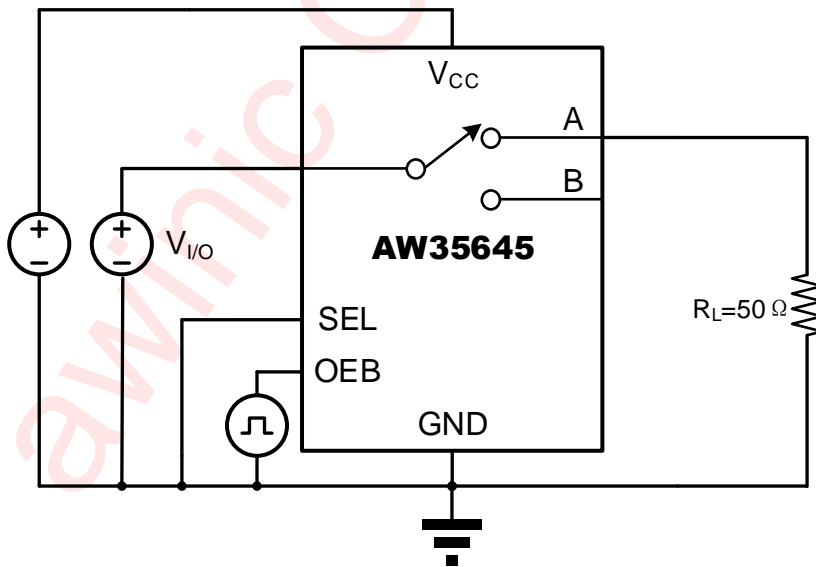
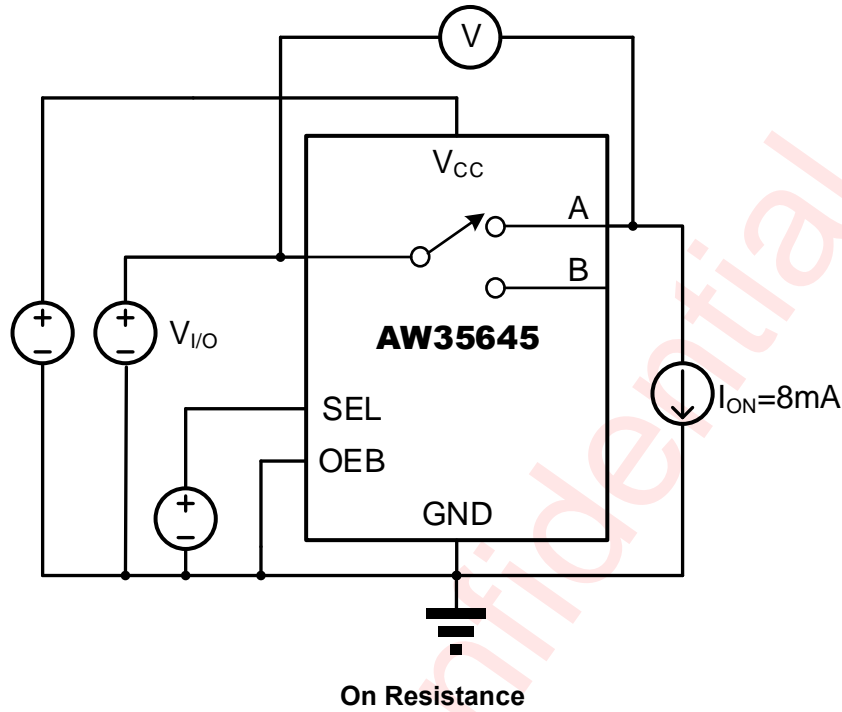
OEB	SEL	Function
H	X	Clock and Data ports High Impedance
L	L	CLKP/N=CLKAP/N, DnP/N=DAnP/N
L	H	CLKP/N=CLKBP/N, DnP/N=DBnP/N

Typical characteristics

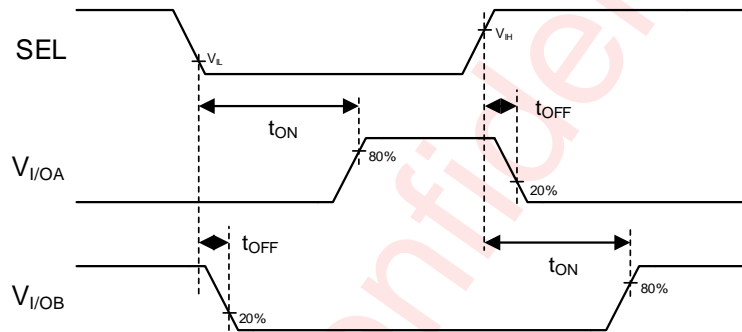
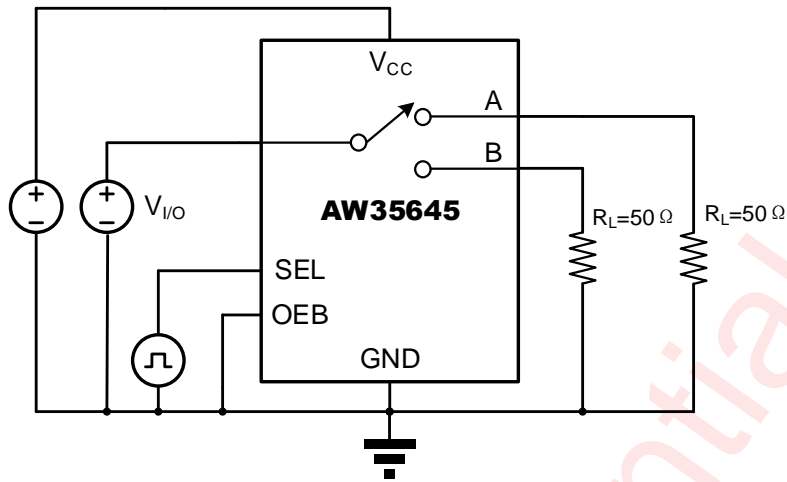
$V_{CC}=3.3V$, $T_A=25^\circ C$, unless other noted.



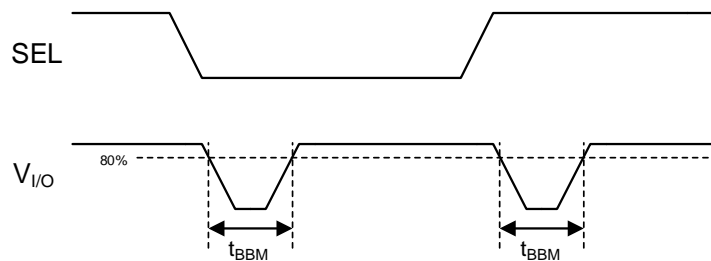
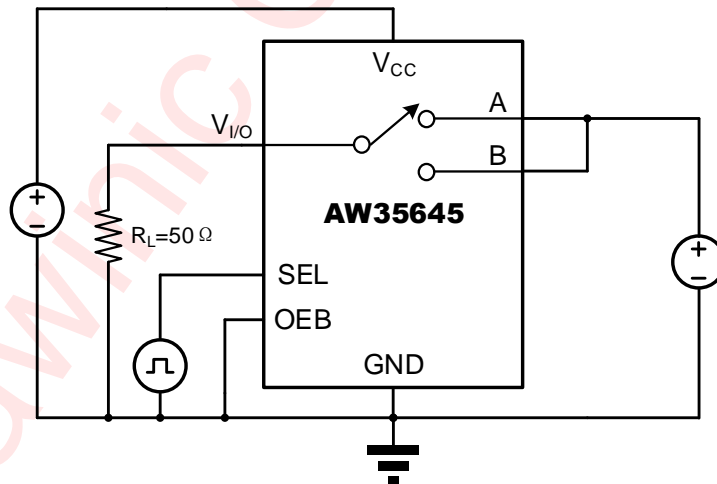
Parameter Measurement Information



t_{EN} and t_{DIS} Timing For OEB



t_{ON} and t_{OFF} Timing For SEL



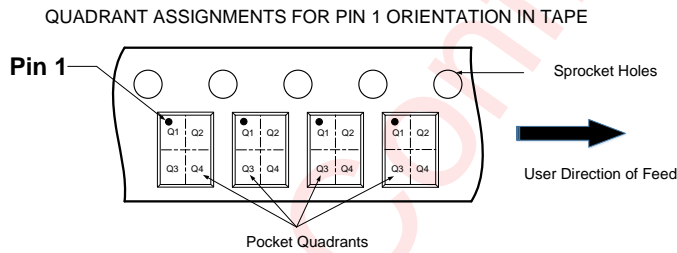
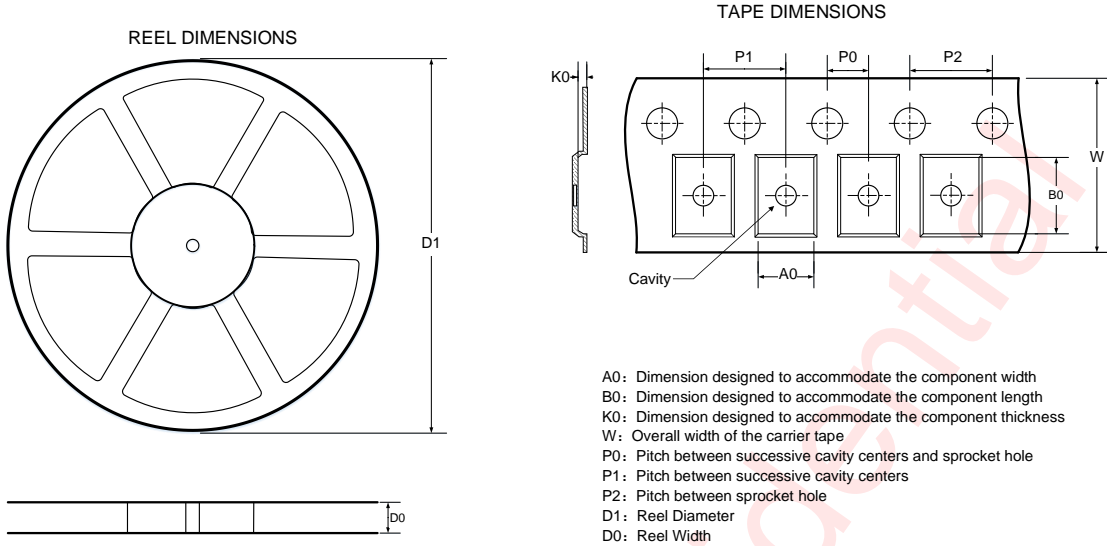
t_{BBM} For SEL

PCB Layout Consideration

To obtain the optimal performance of AW35645, PCB layout should be considered carefully. Here are some guidelines:

1. Place supply bypass capacitors as close to V_{CC} and GND pin as possible and avoid placing the bypass capacitors near the high-speed traces.
2. The characteristic impedance of the traces must match that of the receiver and transmitter to maintain signal integrity.
3. Route the high-speed signals using a minimum amount of vias and corners which reduces signal reflections and impedance changes. When it becomes necessary to make the traces turn 90° , use an arc instead of making a single 90° turn.
4. Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed signal lines because they cause signal reflections.
6. Route all high-speed signal traces over continuous GND planes, with no interruptions.
7. High speed signal traces must be length matched as much as possible to minimize skew between data and clock lines. Width and spacing between differential traces must be equal line width and line spacing

Tape And Reel Information

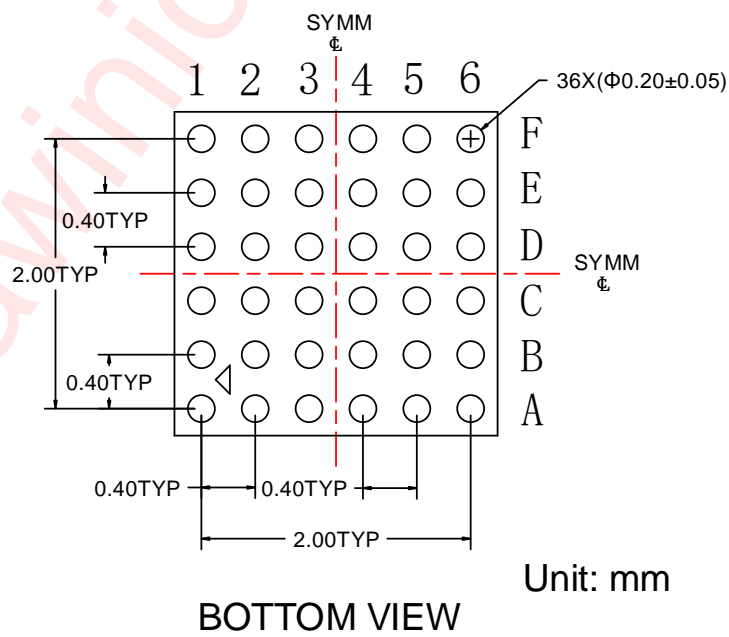
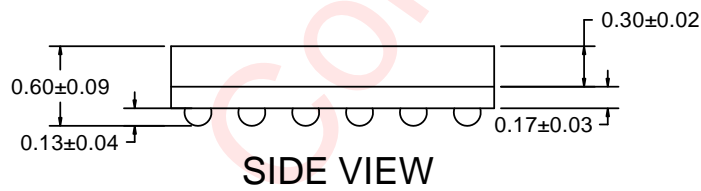
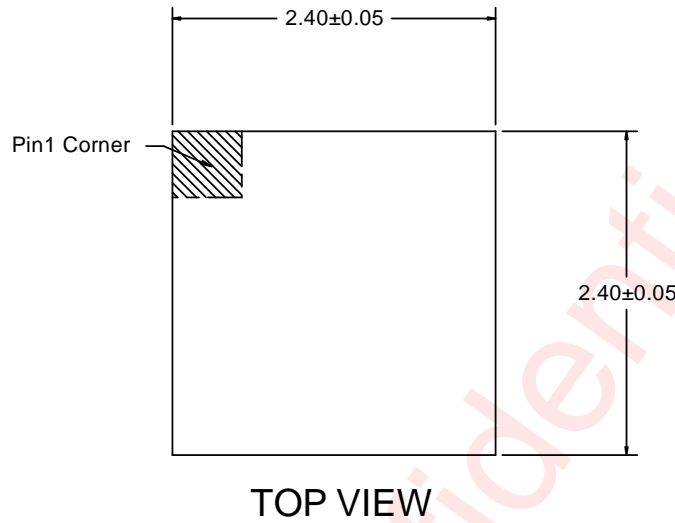


DIMENSIONS AND PIN1 ORIENTATION

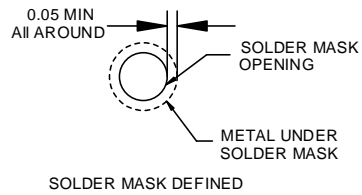
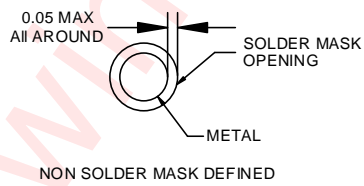
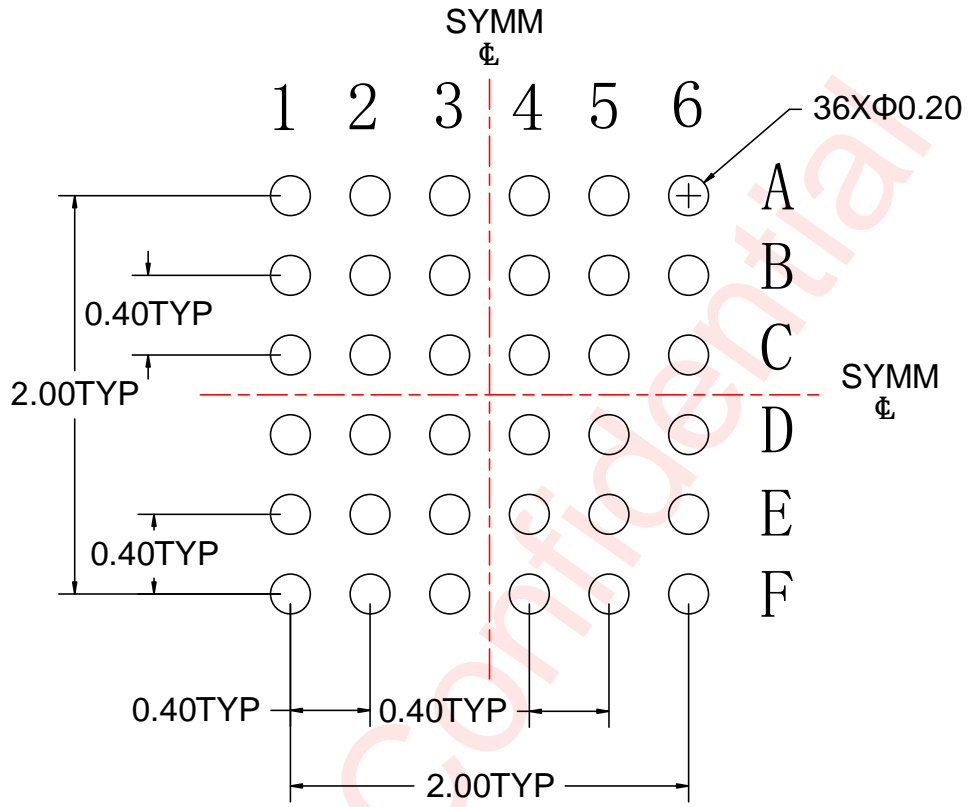
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.65	2.65	0.85	2	4	4	8	Q1

All dimensions are nominal

Package Description



Land Pattern Data



Unit: mm

Revision History

Version	Date	Change Record
V1.0	November 2020	Datasheet V1.0 released
V1.1	December 2021	Modify the maximum value of I _{CC_PD}

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