ES8327

Low Power Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I^2S/PCM/TDM master or slave serial data port
- 256/384Fs, USB 12/24 MHz and other non standard audio system clocks
- I^2C interface

Stereo DMIC

- Support 2-ch digital microphone
- 24-bit, 8 to 96 kHz sampling frequency
- 110 dB signal to noise ratio, -100 dB THD+N

Mono ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 102 dB signal to noise ratio, -90 dB THD+N
- Two pairs of analog input with differential input option
- Low noise pre-amplifier
- Auto level control (ALC) and noise gate
- Noise reduction filter

Stereo DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 100 dB signal to noise ratio, -85 dB THD+N
- Ground centered headphone driver
- Dynamic range compression
- Headset detection
- OMTP and CTIA auto switch
- Pop and click noise suppression

APPLICATIONS

- Notebook
- Tablet
- PC

ORDERING INFORMATION

ES8327 -40°C ~ +105°C
QFN-32

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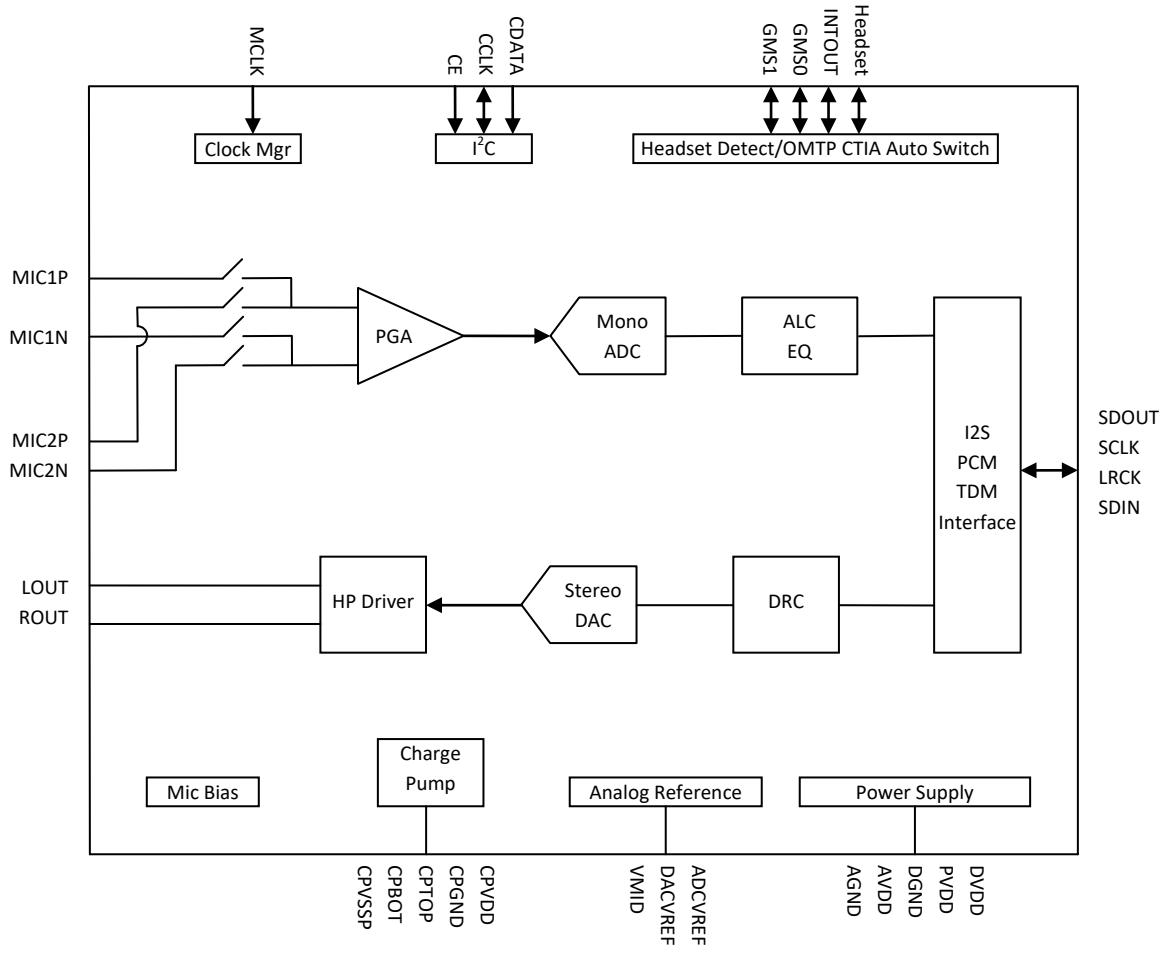
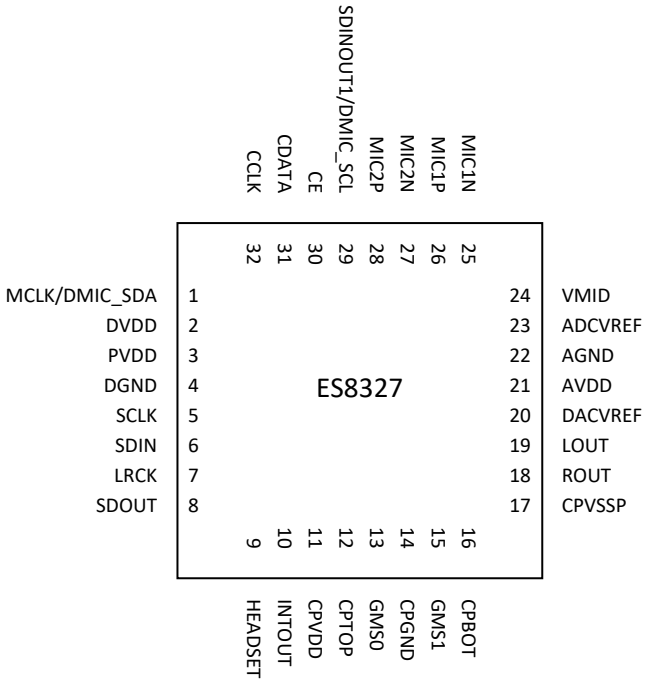
1. BLOCK DIAGRAM

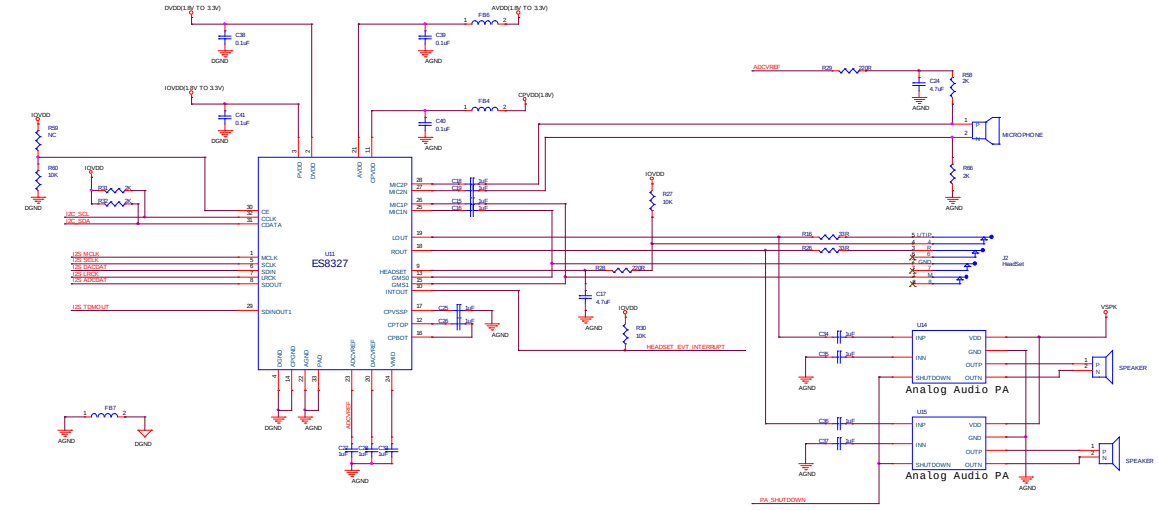


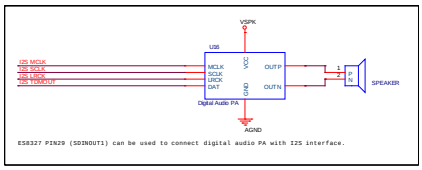
2. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA, CE	32, 31, 30	I, I/O, I	I^2C clock, data, address
MCLK/DMIC_SDA	1	I	Master clock or DMIC input
SCLK	5	I/O	Serial data bit clock
SDIN	6	I	DAC serial data input
LRCK	7	I/O	Serial data left and right channel frame clock
SDOUT	8	O	ADC serial data output
SDINOUT1/DMIC_SCL	29	O	SDOUT1 from SDIN (TDM) or DMIC bit clock
MIC2P MIC2N	28 27	I	Analog mic 2 input P Analog mic 2 input N
MIC1P MIC1N	26 25	I	Analog mic 1 input P Analog mic 1 input N
HEADSET, INTOUT GMS0, GMS1	9, 10 13, 15	I/O	Headset detect and interrupt OMTP and CTIA auto switch
LOUT, ROUT	19, 18	O	DAC stereo analog output
PVDD	3	Analog	Power supply for the digital input and output
DVDD, DGND	2, 4	Analog	Digital power supply
AVDD, AGND	21, 22	Analog	Analog power supply
CPVDD, CPGND	11, 14	Analog	Charge pump power supply
CPTOP, CPBOT	12, 16	Analog	Charge pump capacitor top and bottom
CPVSSP	17	Analog	Charge pump filtering capacitor connection
VMID	24	Analog	Filtering capacitor connection
ADCVREF, DACVREF	23, 20	Analog	Filtering capacitor connection

3. TYPICAL APPLICATION CIRCUIT





IOVDD	IO Power Supply, 1.8V to 3.3V. Please refer to ES8327 Datasheet
DVDD	Digital Power Supply, 1.8V to 3.3V. Please refer to ES8327 Datasheet
AVDD	Analog Power Supply, 1.8V to 3.3V. Please refer to ES8327 Datasheet
CPVDD	Charge Pump Power Supply, must be 1.8V. One 1.8V LDO is recommended for CPVDD power supply Please refer to ES8327 Datasheet

CE	I2C Chip Address.	pulled up to PVDD, I2C Chip Address = 0x19
		pulled down to GND, I2C Chip Address = 0x18
HEADSET_EVT_INTERRUPT	An Interrupt Signal to Host SOC / CPU	
ADCVREF	ADCVREF can be used as Microphone Power Supply.	

4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (32Fs, 64Fs, 128Fs, 256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and some common non standard audio clocks (16 MHz, 25 MHz, 26 MHz, etc).

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 0011 00x, where x equals CE. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^2C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I^{2}C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	0011 00 CE	0	ACK	RAM	ACK	DATA	ACK	Stop

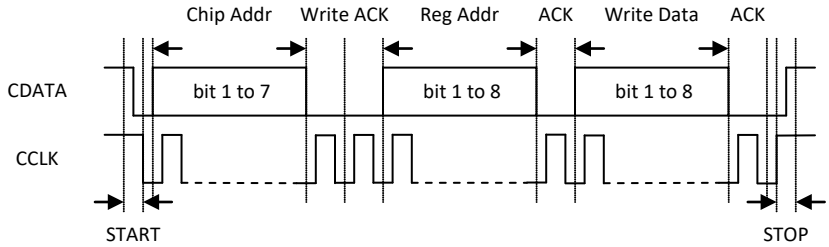


Figure 1a I^{2}C Write Timing

Table 2 Read Data from Register in I^{2}C Interface Mode

	Chip Address	R/W		Register Address		
Start	0011 00 CE	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	0011 00 CE	1	ACK	Data	NACK	Stop

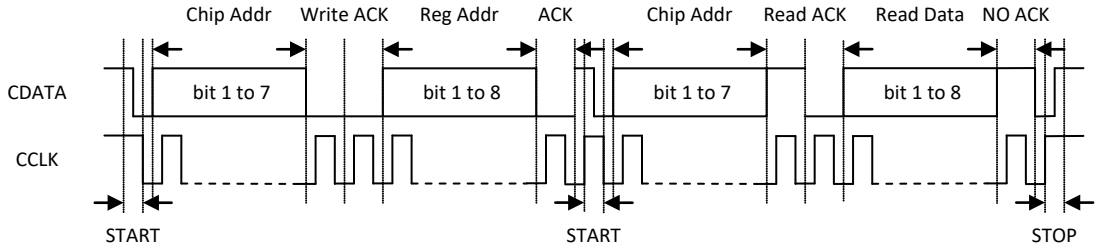


Figure 1b I^{2}C Read Timing

6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, SCLK and SDIN or SDOUT pins. These formats are I^2S, left justified, DSP/PCM and TDM. DAC input SDIN is sampled by the device on the rising edge of SCLK. ADC data is out at SDOUT on the falling edge of SCLK. The relationship of SDATA (SDIN/SDOUT), SCLK and LRCK with these formats are shown through Figure 2a to Figure 2h.

SDIN 6-ch TDM data can directly output to 2-ch SDINOUT1, 2-ch SDINOUT2 and 2-ch SDINOUT3.

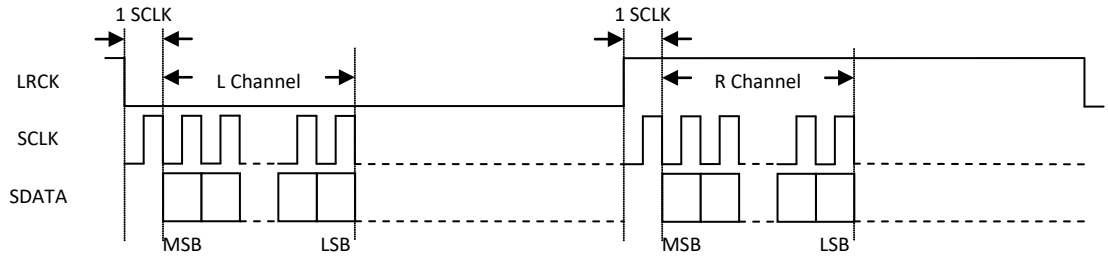


Figure 2a I^2S Serial Audio Data Format

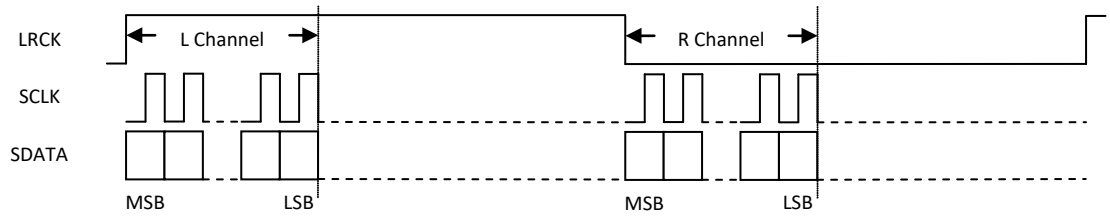


Figure 2b Left Justified Serial Audio Data Format

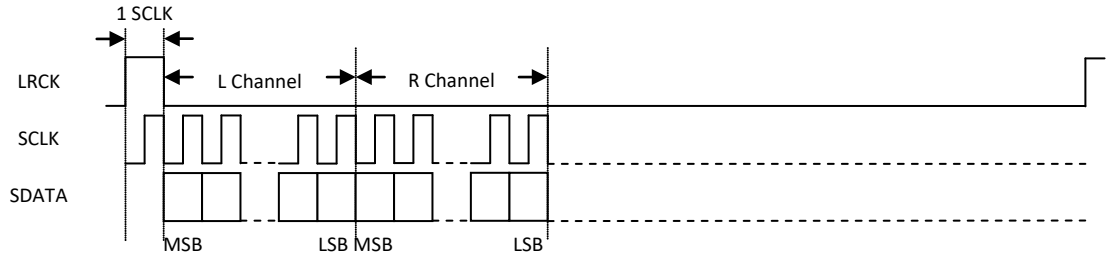


Figure 2c DSP/PCM Mode A Serial Audio Data Format

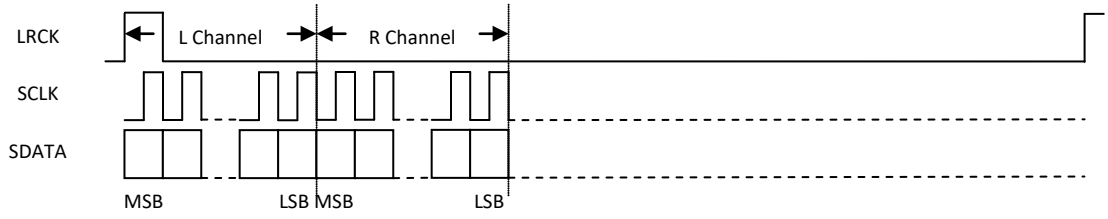


Figure 2d DSP/PCM Mode B Serial Audio Data Format

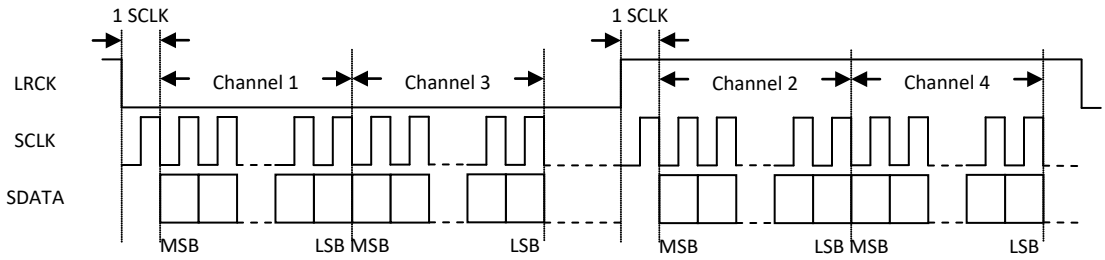


Figure 2e TDM I^{2}S Serial Audio Data Format

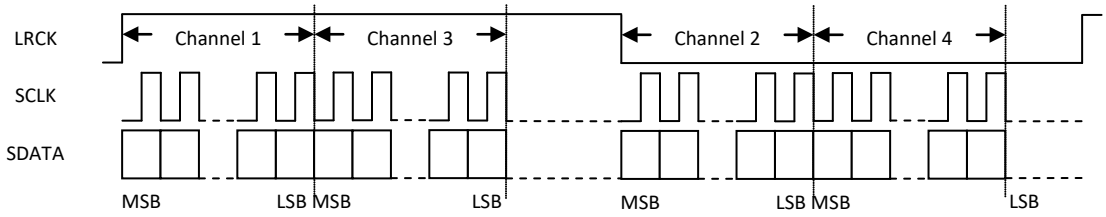


Figure 2f TDM Left Justified Serial Audio Data Format

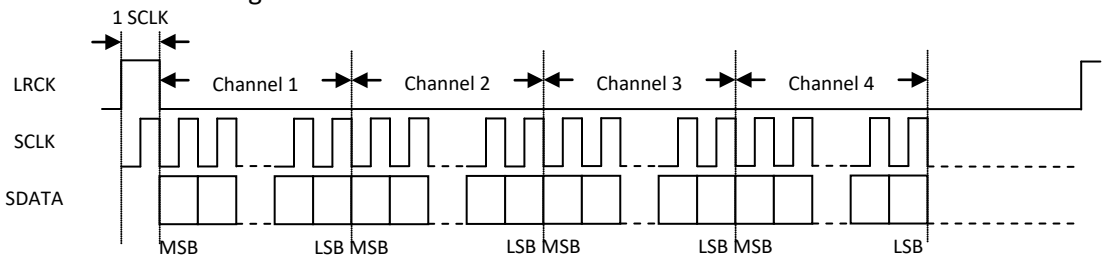


Figure 2g TDM DSP/PCM Mode A Serial Audio Data Format

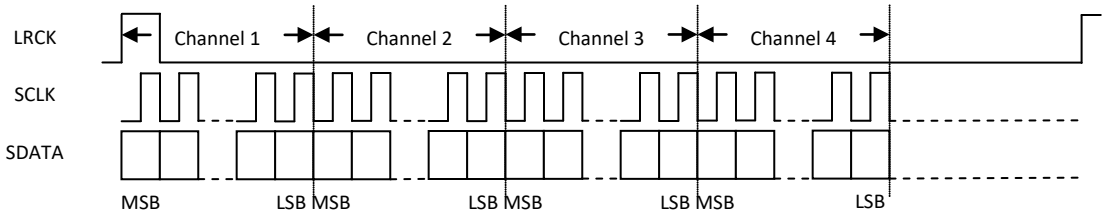


Figure 2h TDM DSP/PCM Mode B Serial Audio Data Format

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+105°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
AVDD	1.7	1.8/3.3	3.6	V
CPVDD (Note 1)	1.6	1.8	2.0	V
DVDD (Note 2)	1.6	1.8/3.3	3.6	V
PVDD	1.6	1.8/3.3	3.6	V

Note 1: recommend an option to add a LDO in PCB for CPVDD, in case CPVDD supply is noisy.

Note 2: for 96 kHz sampling frequency, DVDD must be 3.3V (±10%).

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	97	102	104	dB
THD+N	-93	-90	-87	dB
Gain Error			±5	%
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input Level (±: differential P/N)		±AVDD/3.3		±Vrms
Input Impedance		6		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	95	100	102	dB
THD+N	-88	-85	-82	dB
Gain Error			±5	%
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	53			dB
Analog Output				
Full Scale Output Level		AVDD/3.3		Vrms

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V DVDD=1.8V, PVDD=1.8V, AVDD=1.8V		TBD		mW
Power Down Mode (Note 3)				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V DVDD=1.8V, PVDD=1.8V, AVDD=1.8V		0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*PVDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		PVDD		V
Output Low-level Voltage		0		V

Note 3: recommend all power supply on, entering low power through control register setting, then stopping input clock.

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			49.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			100	KHz
LRCK duty cycle (Note 4)		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SLKL}	16		ns
SCLK Pulse width high	T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)	T_{SLR}		10	ns
LRCK edge to SCLK rising (slave mode only)	T_{LSR}	10		ns
SCLK falling to SDOUT valid VDDD=3.3V VDDD=1.8V	T_{SDO}		16 39	ns
LRCK edge to SDOUT valid (Note 5) VDDD=3.3V VDDD=1.8V	T_{LDO}		11 25	ns
SDIN valid to SCLK rising setup time	T_{SDIS}	10		ns
SCLK rising to SDIN hold time	T_{SDIH}	10		ns

Note 4: one SCLK period of high time in DSP/PCM modes.

Note 5: only apply to MSB of Left Justified or DSP/PCM mode B.

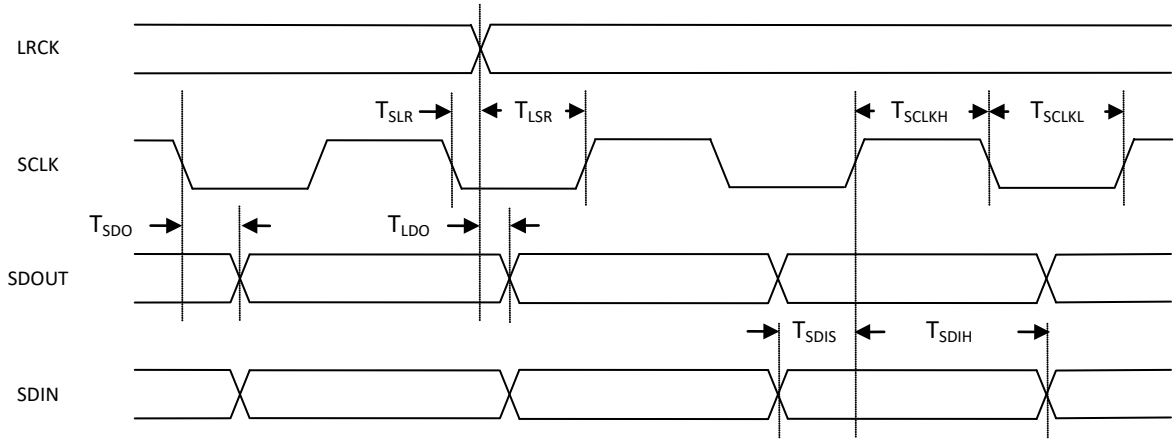


Figure 3 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

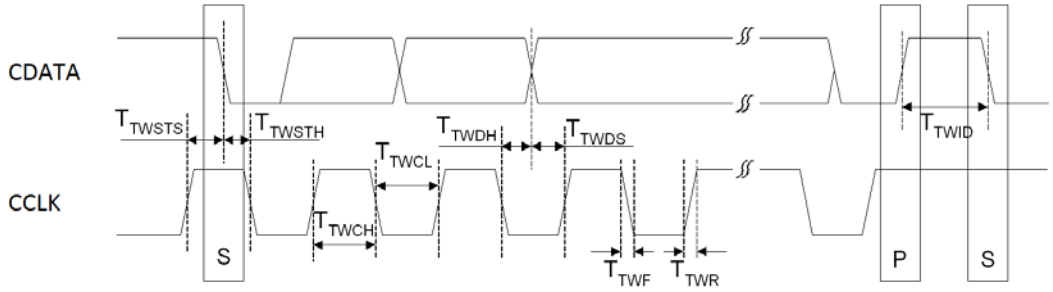


Figure 4 I²C Timing

8. CONFIGURATION REGISTER DEFINITION

REGISTER 0X00 -RESET, DEFAULT 00011111

Bit Name	Bit	Description
CSM_ON	7	Chip Current State Machine ON/OFF control 0 - CSM power down(default) 1 - CSM power up
MSC	6	Master/Slave select for SDP 0 - Slave mode(default) 1 - Master mode
SEQ_DIS	5	Power up sequence enable control 0 - Power up sequence enable(default) 1 - Power up sequence disable
RST_DIG	4	Digital circuits reset (except control port) 0 - Not reset 1 - Reset(default)
RST_CMG	3	Clock manager circuit reset 0 - Not reset 1 - Reset(default)
RST_MST	2	Master circuit reset 0 - Not reset 1 - Reset(default)
RST_ADCDIG	1	ADC digital circuit reset 0 - Not reset 1 - Reset(default)
RST_DACDIG	0	DAC digital circuit reset 0 - Not reset 1 - Reset(default)

REGISTER 0X01 -CLOCK MANAGER, DEFAULT 00000000

Bit Name	Bit	Description
CPCLK_ON	6	Charge Pump clock CPCLK control 0 - CPCLK off(default) 1 - CPCLK on
MCLK_ON	5	MCLK in ON/OFF control 0 - MCLK off (default) 1 - MCLK on
BCLK_ON	4	BCLK in ON/OFF control 0 - BCLK off (default) 1 - BCLK on
CLK1_ON	3	clk1 ON/OFF control 0 - clk1 off (default) 1 - clk1 on
CLK3_ON	2	clk3 ON/OFF control 0 - clk3 off (default) 1 - clk3 on
CLK8_ON	1	clk8 ON/OFF control 0 - clk8 off (default) 1 - clk8 on
CLK9_ON	0	clk9 ON/OFF control

		0 - clk9 off (default) 1 - clk9 on

REGISTER 0X02-CLOCK MANAGER, DEFAULT 00000000

Bit Name	Bit	Description
MSTCLK_SEL	7:6	Master BCLK/LRCK divider source clock selection 0 - from main_clk(main_clk refer to MAINCLK_SEL)(default) 1 - from adc_cfclk(adc_cfclk refer to ADC_CFCLK_SEL) 2 - from adc_mclk(adc_mclk refer to ADC_MCLK_SEL) 3 - from dac_mclk (dac_mclk refer to DAC_MCLK_SEL)
DMIC_SCL_SEL	4	DMIC clock select 0 - from ADC OSR clock， ES8327 provides DMIC_SCL to DMIC. (default) 1 - from MCLK in, system provides DMIC clock from DMIC_SCL to ES8327, and ES8327 synchronize with DMIC_SCL as ADC OSR clock. “adc_mclk” should be 4 times frequency of DMIC_SCL.
MAINCLK_SEL	3	Internalclock “main_clk”select 0 - from MCLK PAD(default) 1 - from BCLK PAD
BITCLK_SEL	2	Slave bit clock “bit_clk”select 0 - from BCLK PAD(default) 1 - from MCLK PAD
MAINCLK_INV	1	Main clock“main_clk”invert 0 - normal(default) 1 - invert
BITCLK_INV	0	Bit clock “bit_clk”invert 0 - normal(default) 1 - invert

REGISTER 0X03-CLOCK MANAGER, DEFAULT 00000010

Bit Name	Bit	Description
RATIO_RESAMPLE	6:4	Clock cycles justify for ratio sync. 0 -no sync（default） 1 - 1/512，sync 1 cycle per 512 cycles for adc_ratio<ADC_OSR*16+1 case 2 - 1/256，sync 1 cycle per 256 cycles for adc_ratio<ADC_OSR*16+2 case 3 - 1/128，sync 1 cycle per 128 cycles for adc_ratio<ADC_OSR*16+4 case 4 - 1/64，sync 1 cycle per 64 cycles for adc_ratio<ADC_OSR*16+8 case 5 - 1/32，sync 1 cycle per 32 cycles for adc_ratio<ADC_OSR*16+16 case 6 - 1/16，sync 1 cycle per 16 cycles for adc_ratio<ADC_OSR*16+32 case 7 - 1/8，sync 1 cycle per 8 cycles for adc_ratio<ADC_OSR*16+64 case This register works at non-standard ratio case.
INTCLK_SEL	3:2	Interrupt and hp detection clock select 0 - main_clk (default) 1 - Internal oscillator (when OSC_EN enable oscillator) 2 - Master BCLK_OUT 3 - Master LRCK_OUT
OSC_EN	1:0	Internal oscillator control 0 - auto mode, HP DETECT controls oscillator automatically. Any HP plug in/out or any button will wake up oscillator, and turn off automatically when operation finish。 1 - oscillator always on 2 - oscillator always off, and output a low level(default) 3 - oscillator always off, and output a high level. Note: INTCLK_SEL should be ‘1’ when this register be configured 0 or 1

REGISTER 0X04-CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
DIV_CLK6	7:5	clk6 divider clk6=clk in /(DIV_CLK6+1) 0 - divide by 1(default)
DIV_CLK1	4:0	clk1 divider clk1=clk in/(DIV1_CLK+1) 0 - divide by 1(default)

REGISTER 0X05-CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
DIV_CLK7	7:5	clk7 divider clk7=clk in /(DIV_CLK7+1) 0 - divide by 1(default)
DIV_CLK3	4:0	clk3 divider clk3=clk in /(DIV_CLK3+1) 0 - divide by 1(default)

REGISTER 0X06-CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
CLK_DOUBLE	5:4	clock doubler control 0 - clock bypass(default) 1 - clock x2 with delay 5ns cell 2 - clock x2 with delay 10ns cell 3 - clock x2 with delay 15ns cell
DLL1_MODE	3:2	DLL1 mode control 0 - DLL1 bypass and power down(default) 1 - DLL1 multiply x4 2 - DLL1 multiply x6 3 - DLL1 multiply x8
DLL2_MODE	1:0	DLL2 mode control 0 - DLL2 bypass and power down(default) 1 - DLL2 multiply x4 2 - DLL2 multiply x6 3 - DLL2 multiply x8

REGISTER 0X07-CLOCK MANAGER, DEFAULT 0010 1101

Bit Name	Bit	Description
CLK1_MUX	7	mux for DIV_CLK1 clock 0 - main_clk (default) 1 - clk4
CLK3_MUX	6	mux for DIV_CLK3 clock 0 - main_clk (default) 1 - clk2
CLK8_MUX	5:3	clk8 mux 0 - from main_clk 1 - from clk1 2 - from clk2 3 - from clk3 4 - from clk4

		5 - from clk5(default) 6 - from clk6 7 - from clk7
CLK9_MUX	2:0	clk9 mux 0 - from main_clk 1 - from clk1 2 - from clk2 3 - from clk3 4 - from clk4 5 - from clk5(default) 6 - from clk6 7 - from clk7

REGISTER 0X08-CLOCK MANAGER, DEFAULT 0000 1010

Bit Name	Bit	Description
ANACLK_ADC_SEL	6:4	ADC OSR clock anaclk_adc selection 0 -clk8/4(default) 1 -clk9/4 2 - from clk1 3 - from clk3 4 - from clk6 5 - from clk7 6 - 0 7 - 1
ADC_MCLK_SEL	3:0	ADC main clock adc_mclk selection 0 - from main_clk 1 - from clk1 … 10 - from clk10 (default) … 15 - from clk15

REGISTER 0X09-CLOCK MANAGER, DEFAULT 0000 1010

Bit Name	Bit	Description
ANACLK_DAC_SEL	6:4	DAC OSR clock anaclk_dac selection 0 -clk8/4(default) 1 -clk9/4 2 - from clk1 3 - from clk3 4 - from clk6 5 - from clk7 6 - 0 7 - 1
DAC_MCLK_SEL	3:0	DAC main clock dac_mclk selection 0 - from main_clk 1 - from clk1 … 10 - from clk10(default) … 15 - from clk15

REGISTER 0X0A-CLOCK MANAGER, DEFAULT 00011111

Bit Name	Bit	Description
DAC_DSMCLK_SEL	7	DAC dsm clock dac_dsmclk selection 0 - dac_mclk(default) 1 - dac_mclk/2 This bit select lower dsm/dem/analog clocks and normal DAC_OSR (for example: 64FS, but DAC_OSR should be configured 0x1F)
ADC_CFCLK_SEL	6	ADC Comb filter clock adc_cfclk selection 0 - adc_mclk(default) 1 - adc_mclk/2 This bit select lower analog/dem/cf clocks and half ADC_OSR (for example: 64FS, but ADC_OSR should be configured 0x0F)
ADC_OSR	5:0	ADC Over Sample Rate control OSR frequency = 4*(ADC_OSR+1)*fs 0~14 - not use 15 - 64*fs 16 - 68*fs 17 - 72*fs ... 30 - 124*fs 31 - 128*fs(default) 32 - 132*fs 33 - 136*fs ... 62 - 252*fs 63 - 256*fs Note: mute configure ADC_CFCLK_SEL =1 when ADC_OSR <31

REGISTER 0X0B-CLOCK MANAGER, DEFAULT 00011111

Bit Name	Bit	Description
DAC_OSR	6:0	DAC Over Sample Rate control OSR frequency =4*(DAC_OSR+1)*fs 0~30: not use 31- 128*fs(default) 32 - 132*fs 33 - 136*fs ... 62 - 252*fs 63 - 256*fs 64 - 260*fs … 94 - 380*fs 95 - 384*fs 96 - 388*fs … 126 - 508*fs 127 - 512*fs

REGISTER 0X0C-CLOCK MANAGER, DEFAULT 00011111

Bit Name	Bit	Description
DIV_CPCLK	6:0	Charge pump clock CPCLK divider control

		CPCLK = mstclk/(DIV_CPCLK+1), mstclk selection reference to MSTCLK_SEL[1:0] 31 - divide by 32(default) “mstclk” is selected by register MSTCLK_SEL

REGISTER 0X0D-CLOCK MANAGER, DEFAULT 0000 0011

Bit Name	Bit	Description
DIV_BCLK	6:0	Master BCLK divider bclk_out=mstclk/(DIV_BCLK+1), mstclk reference to MSTCLK_SEL 3 - divide by 4(default)

REGISTER 0X0E-CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
TRI_BCLK	7	BCLK Tri-state control 0 - normal(default) 1 - Tri-state
TRI_LRCK	6	LRCK Tri-state 0 - normal(default) 1 - Tri-state
TRI_SDOUT	5:4	SDOUT Tri-state 0 - normal(default) 1 - Tri-state 2 - output 'low' 3 - output 'high'
DIV_LRCK[11:8]	3:0	Master LRCK divider bit 11 to bit 8 LRCK(master)=mstclk/(LRCK_DIV+1), mstclk reference to MSTCLK_SEL

REGISTER 0X0F-CLOCK MANAGER, DEFAULT 11111111

Bit Name	Bit	Description
DIV_LRCK[7:0]	7:0	Master LRCK divider bit 7 to bit 0 LRCK(master)=mstclk/(LRCK_DIV+1), mstclk reference to MSTCLK_SEL 255 - divide by 256(default)

REGISTER 0X10 -CLOCK MANAGER, DEFAULT 1110 0000

Bit Name	Bit	Description
VMIDS1	7:6	VMIDSEL at “CSM==3” state 0 - vmidSel=0 1 - vmidSel=1 2 - vmidSel=2 3 - vmidSel=3(default)
VMIDS1_TIME	5:0	The counter3 at “CSM==3” state. Counter3 = 256*VMIDS1_TIME[5:1] + 4*VMIDS1_TIME[0] + 1 Total time at “CSM==3”： counter3*T(LRCK timer) For example at master LRCK=48KHz: 0 - 21us 1 - 104us 2 - 5ms … 32- 86ms(default) … 63 - 167ms(max)

		LRCK=16KHz: 0 - 63us 1 - 312us … 32- 258ms(default) … 63 - 500ms(max) LRCK=8KHz: 0 - 125us 1 - 625us … 32 - 512ms(default) … 63 - 1000ms(max)

REGISTER 0X11-CLOCK MANAGER, DEFAULT 1010 0000

Bit Name	Bit	Description
VMIDS2	7:6	VMIDSEL at “CSM==2” state 0 - vmidSel=0 1 - vmidSel=1 2 - vmidSel=2(default) 3 - vmidSel=3
VMIDS2_TIME	5:0	The counter at “CSM==2” state. Counter2 = 256*VMIDS2_TIME[5:1] + 4*VMIDS2_TIME[0] + 1 Total time at S3： counter*T(LRCK timer) For example at master LRCK=48KHz: 0 - 21us 1 - 104us 2 - 5ms … 32- 86ms(default) … 63 - 167ms(max) For example at master LRCK=16KHz: 0 - 63us 1 - 312us … 32- 258ms(default) … 63 - 500ms(max) For example at master LRCK=8KHz: 0 - 125us 1 - 625us … 32 - 512ms(default) … 63 - 1000ms(max)

REGISTER 0X12-CLOCK MANAGER, DEFAULT 0100 0000

Bit Name	Bit	Description
CAL_TIME	7:0	counter = 128*CAL_TIME[7:1] + 4*CAL_TIME[0] + 1 total calibration time： counter*T(LRCK timer) For example at master LRCK=48KHz: 0 - 21us 1 - 104us 2 - 5ms … 64 - 86ms (default) … 255 - 341ms(max) For example at master LRCK=16KHz: 0 - 63us 1 - 312us … 64 - 258ms(default) … 255 - 1024ms(max) For example at master LRCK=8KHz: 0 - 125 1 - 625us … 64 - 512ms(default) … 255 - 2033ms(max)

REGISTER 0X13-SDP, DEFAULT 00000000

Bit Name	Bit	Description
MSTBCLK_FITBIT	6	BCLK out control when master mode 0 - continual bclk(default) 1 - master bclk stop after data transfer out Note: don't configure MSTBCLK_FITBIT as ‘1’ when TDM mode.
SDP_LRP	5	I2S/Left Justify case: 0 - L/R normal polarity(default) Left/Right=High/Low (LJ) Left/Right=Low/High (I2S) 1 - L/R invert polarity Left/Right=Low/High (LJ) Left/Right=High/Low (I2S) DSP mode case: 0 - Mode A, MSB is available on 2nd BCLK rising edge after LRCK rising edge(default) 1 - Mode B, MSB is available on 1st BCLK rising edge after LRCK rising edge
SDP_WL	4:2	SDP word length 0 - 24-bit(default) 1 - 20-bit 2 - 18-bit 3 - 16-bit 4 - 32-bit

		others - 24-bit
SDP_FMT	1:0	SDP format 0 - I2S(default) 1 - LJ 2 - reserve 3 - DSP

REGISTER 0X14-SDP, DEFAULT 00000000

Bit Name	Bit	Description
S2P_SLOT	6:4	DAC data slot selection from SDIN TDM 0 - from SDIN slot0 data (default) 1 - from SDIN slot1 data … 7 - from SDIN slot7 data
S2P_MUTE_R	1	DAC S2P right channel mute control 0 – unmute (default) 1 - mute
S2P_MUTE_L	0	DAC S2P left channel mute control 0 – unmute (default) 1 - mute

REGISTER 0X15-SDP, DEFAULT 00011111

Bit Name	Bit	Description
P2S_TDM_MODE	4	P2S TDM mode control for SDOUT 0 - Normal 2-channel SDP 1 - TDM mode 4-channel data output(default)
P2S_MUTE_4	3	ADC P2S channel 4mute control 0 – unmute 1 –Mute (default)
P2S_MUTE_3	2	ADC P2S channel 3mute control 0 – unmute 1 –Mute (default)
P2S_MUTE_2	1	ADC P2S channel 2mute control 0 – unmute 1 –Mute (default)
P2S_MUTE_1	0	ADC P2S channel 1mute control 0 – unmute 1 –Mute (default)

REGISTER 0X16-ANALOG, DEFAULT 11111011

Bit Name	Bit	Description
PDN_ANA	7	0 - Power upoverallanalog circuits 1 - Power down overall analog circuits(default)
PDN_IBIASGEN	6	0 - Power up system bias circuits 1 - Power down system bias circuits(default)
PDN_ADCVREFGEN	5	0 - Power up ADC reference circuits 1 - Power down ADC reference circuits(default)
PDN_DACVREFGEN	4	0 – PowerupDAC reference circuits 1 - Power down DAC reference circuits(default)
PDN_VRP	3	0 - Power up ADC reference voltage

		1 - Power down ADC reference voltage(default)
LP_DAC	2	0 - DAC at normal power mode (default) 1 - DAC at low power mode
PDN_DACL	1	0 - Power up DACL 1 - Power down DACL(default)
PDN_DACR	0	0 - Power up DACR 1 - Power down DACR(default)

REGISTER 0X17-ANALOG,DEFAULT11111000

Bit Name	Bit	Description
MODTOP_RST	5	0 - normal 1 - reset ADC to power down state(default)
PDN_MOD	4	0 - normal 1 - ADC power down(default)
PDN_PGA	3	0 - normal 1 - PGA power down(default)

REGISTER 0X18-ANALOG, DEFAULT 00000000

Bit Name	Bit	Description
VMIDSEL	1:0	0 - vmid power down(default) 1 - start up vmid normal speed charge 2 - normal vmid operation 3 - start up vmid fast speed charge

REGISTER 0X19-ANALOG,DEFAULT 00000000

Bit Name	Bit	Description
LP_ADCVRP	7	0 - Normal power mode ADC reference(default) 1 - Low power mode ADC reference
LP_DACVRP	6	0 - Normal power mode DAC reference(default) 1 - Low power mode DAC reference
LP_PGAOUT1	5	0 - Normal power level1 mode PGAoutput(default) 1 - Low power level1 mode PGAoutput
LP_PGAOUT2	4	0 - Normal power level2 modePGAoutput(default) 1 - Low power level2 mode PGAoutput
LP_FLASH	3	0 - Normal power mode ADC flash(default) 1 - Low power mode ADC flash
LP_INT1	2	0 - Normal power mode ADC modulator(default) 1 - Low power mode ADC modulator
LP_VCMMOD	1	0 - Normal power mode ADC modulator reference(default) 1 - Low power mode ADC modulator reference
LP_PGA	0	0 - Normal power mode PGA(default) 1 - Low power mode PGA

REGISTER 0X1A-ANALOG, DEFAULT 00000000

Bit Name	Bit	Description
DITHERSEL10	7:6	00 - DSM dither level0(default) 01 - DSM dither level1 10 - DSM dither level2 11 - DSM dither level3
OFFSETL1	5	0 - no offset(default)

		1 - offset enabled
OFFSET0	4	0 - no offset(default) 1 - offset enabled
DELAYDAC	1	0 - no delay(default) 1 - delay DAC turn on
ENDITHER	0	0 - close DSM dither(default) 1 - open DSM dither

REGISTER 0X1B-ANALOG, DEFAULT 01000000

Bit Name	Bit	Description
RES_MICBIAS	6:4	Micbias resistor select 0 - R_SCALE + 4.2K 1 - R_SCALE + 3K 2 - R_SCALE + 2.2K 3 - R_SCALE + 1.4K 4 - R_SCALE + 1K（default） 5 - R_SCALE + 0.6K 6 - R_SCALE + 0.3K 7 - R_SCALE + 0K “R_SCALE” is decided by register HP_SCALE
ENHPDETECT	3:2	0x - automatic mode: headphone plugged in, micbias turned on headphone unplugged, micbias turned off(default) 10 - force micbias turn off 11 - force micbias turn on
HPSCALE	1:0	HP SCALE internal resister selection 0 - 1000 ohm(default) 1 - 800 ohm 2 - 600 ohm 3 - 200 ohm

REGISTER 0X1C-ANALOG, DEFAULT 01111100

Bit Name	Bit	Description
VSEL	6:0	01111100 - normal (default)

REGISTER 0X1D-ANALOG, DEFAULT 00001010

Bit Name	Bit	Description
DAC_IBIAS_SW	4	0 - set DAC bias level normal(default) 1 - set DAC bias level high
IBIASGEN_SEL	3:2	00 - set system bias level0 01 - set system bias level1 10 - set system bias level2(default) 11 - set system bias level3(highest bias)
ADCBIAS_SW	1:0	00 - set ADC bias level0 01 - set ADC bias level1 10 - set ADC bias level2(default) 11 - set ADC bias level3(highest bias)

REGISTER 0X1E-ANALOG, DEFAULT 10001000

Bit Name	Bit	Description

MODFLBIAS_SW	7:4	0000 - not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8(default) 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
PGABIAS_SW	3:0	0000 - not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8(default) 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X1F-ANALOG, DEFAULT 10001000

Bit Name	Bit	Description
MODI1BIAS_SW	7:4	0000 - not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8(default) 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
MODI2BIAS_SW	3:0	0000 - not allowed

		0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8(default) 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X20 -ANALOG, DEFAULT 10001000

Bit Name	Bit	Description
MODSMBIAS_SW	7:4	0000 - not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8(default) 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
MODVMBIAS_SW	3:0	0000 - not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8(default) 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X21-ANALOG, DEFAULT 10001000

Bit Name	Bit	Description
VREFPBIAS_SW	7:4	0000 - not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8(default) 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
MODCPBIAS_SW	3:0	0000 - not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8(default) 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X22-ANALOG, DEFAULT 00001100

Bit Name	Bit	Description
MICBIAS2VRP	5:4	0x : auto, when pdn_vrp=1 biased at VDDA， otherwise biased at internal reference level 10 : force micbias to vdda 11 : force micbias to vrp Note: MICBIAS2VRP will be forced to '0' when in automatic HPmic detection mode
VX2OFF	3	1 - disable vx2
VX1SEL	2	Vx1 selection 0 - level low 1 - level high
VMIDLOW	1:0	Vmid selection 00 - vdda/2 01 - vdda/2-50mv 10 - vdda/2-100mv 11 - vdda/2-150mv

REGISTER 0X23-ANALOG, DEFAULT 00000000

Bit Name	Bit	Description
ADCREFSEL	7	1 - SE mode, raise MicGain 6dB
MIC2SEL	5	1 - select Mic2 as PGA input pair
MIC1SEL	4	1 - select Mic1 as PGA input pair
MICGAIN_SETTING	3:0	PGA gain setting 0 - 0dB (default) 1 - 3dB 2 - 6dB 3 - 9dB 4 - 12dB 5 - 15dB 6 - 18dB 7 - 21dB 8 - 24dB 9 - 27dB others - 30dB

REGISTER 0X24-ANALOG, DEFAULT 00001111

Bit Name	Bit	Description
LP_HP	6	0 - set HP output driver to normal power mode (default) 1 - set HP output driver to low power mode
LP_HPMIX	5	0 - set HPmixerto normal power mode(default) 1 - set HPmixer to low power mode
LP_CPNLDO	4	0 - set CPNLDOto normal power mode (default) 1 - set CPNLDOto low power mode
PDN_CP	3	0 - not power up charge pump 1 - power down charge pump (default)
PDN_CPHP	2	0 - power up HP output driver bias 1 - power down HP output driver bias (default)
PDN_CPNLDO	1	0 - power up CPN LDO 1 - power down CPN LDO(default)
ENREFR_HP	0	0 - Disable HP reference 1 - Enable HP reference(default)

REGISTER 0X25-ANALOG, DEFAULT 00010001

Bit Name	Bit	Description
LD2LHPMIX	7	0 - disable LDAC signal to LHPmixer(default) 1 - enable LDAC signal to LHPmixer
LHPMIX_MUTE	6	0 - unmute LHPmixer(default) 1 - mute LHPmixer
LHPMIXVOL	5:4	LMIX volume 00 - -3.5dB 01 - 0dB (default) 10 - 1dB
RD2RHPMIX	3	0 - disable RDAC signal to RHPmixer(default) 1 - enable RDAC signal to RHPmixer
RHPMIX_MUTE	2	0 - unmute RHPmixer(default) 1 - mute RHPmixer
RHPMIXVOL	1:0	RMIX volume

		0 - -3.5dB 1 - 0dB (default) 2 - 1dB

REGISTER 0X26-ANALOG, DEFAULT 00000000

Bit Name	Bit	Description
HPLVOL	6:4	HPL volume 0 –'0dB' (default) 1 –'-6dB' 2 –'-24dB' 4 –'+3.5dB' 5 –'-3.5dB' 6 –'-18dB' Other: not use
HPLVOR	2:0	HPR volume 0 –'0dB' (default) 1 –'-6dB' 2 –'-24dB' 4 –'+3.5dB' 5 –'-3.5dB' 6 –'-18dB' Other: not use

REGISTER 0X27-ANALOG, DEFAULT 00000000

Bit Name	Bit	Description
HPL_CAL	7	force HPL calibration 0 - normal (default) 1 - force calibration When Force calibration, output set to 0
ENHPL	6	Enable LHP output driver 0 - disable(default) 1 - enable
HPL_OUTEN	5	Enable LHP output 0 - disable(default) 1 - enable
LMIX2LOUT	4	Enable LMIX to output 0 - disable(default) 1 - enable
HPR_CAL	3	force HPR calibration 0 - normal (default) 1 - force calibration When Force calibration, output set to 0
ENHPR	2	Enable RHP output driver 0 - disable(default) 1 - enable
HPR_OUTEN	1	Enable RHP output 0 - disable(default) 1 - enable
RMIX2ROUT	0	Enable RMIX to output 0 - disable(default) 1 - enable

REGISTER 0X28-ANALOG, DEFAULT 10000111

Bit Name	Bit	Description
CP_HIPWR	4	0 - normal(default) 1 - CP power level
HP_REF1	3	HP output driver 0 - light load(default) 1 - heavy load; this bit work together with hp_ref2
HP_REF2	2	HP output driver ref 0 - light load 1 - heavy load; this bit work together with hp_ref1(default)
CPN_LDOLVL	1:0	HP output driver supply voltage select 00 - -1.35v 01 - -1.45v 10 - -1.55v 11 - -1.65v(default)

REGISTER 0X29-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC12_SCALE	6:4	ADC Channel 1/2 gain scale up 0 - 0dB (ADC_OSR=0x1B~0x1F)(default) 1 - 6dB(ADC_OSR=0x17~0x1A) 2 - 12dB (ADC_OSR=0x13~0x16) 3 - 18dB (ADC_OSR=0x10~0x12) 4 - 24dB (ADC_OSR=0x0F) 5 - 30dB 6 - Reserved 7 - Reserved
DMIC_POL	3	DMIC channel select 0 - L=left channel, H=right channel(default) 1 - L=right channel, H=left channel
ADC34_SCALE	2:0	ADC Channel 3/4 gain scale up 0 - 0dB (ADC_OSR=0x1B~0x1F)(default) 1 - 6dB (ADC_OSR=0x17~0x1A) 2 - 12dB (ADC_OSR=0x13~0x16) 3 - 18dB (ADC_OSR=0x10~0x12) 4 - 24dB (ADC_OSR=0x0F) 5 - 30dB 6 - Reserved 7 - Reserved

REGISTER 0X2A-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC1_INV	7	ADC Channel 1 inverter 0 - normal (default) 1 - inverted
ADC1_SRC	5:4	ADC1 data source switch 0 - Analog MIC data(default) 1 - Analog MIC data, invert when HPSW=0 2 - Analog MIC data, invert when HPSW=1 3 - DMIC data from MCLK left channel
ADC2_INV	3	ADC Channel 2 inverter

		0 - normal (default) 1 - inverted
ADC2_SRC	1:0	ADC2 data source switch 0 - Analog MIC data(default) 1 - Analog MIC data, invert when HPSW=0 2 - Analog MIC data, invert when HPSW=1 3 - DMIC data from MCLK right channel

REGISTER 0X2B-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC3_INV	7	ADC Channel 3 inverter 0 - normal (default) 1 - inverted
ADC3_SRC	5:4	ADC3 data source switch 0 - Analog MIC data(default) 1 - Analog MIC data, invert when HPSW=0 2 - Analog MIC data, invert when HPSW=1 3 - DMIC data from MCLK left channel
ADC4_INV	3	ADC Channel 4 inverter 0 - normal (default) 1 - inverted
ADC4_SRC	1:0	ADC4 data source switch 0 - Analog MIC data(default) 1 - Analog MIC data, invert when HPSW=0 2 - Analog MIC data, invert when HPSW=1 3 - DMIC data from MCLK right channel

REGISTER 0X2C-ADC CONTROL, DEFAULT 10111111

Bit Name	Bit	Description
ADC_VOLUME1	7:0	ADC volume control 0x00 - '-95.5dB' 0x01 - '-95dB' ⋯ 0.5dB/step 0xBE - '-0.5dB' 0xBF - '0dB' (default) 0xC0 - '+0.5dB' ⋯ 0xFF - '+32dB' Note: ADC_VOLUME1 is “max gain” when ALC enable.

REGISTER 0X2D-ADC CONTROL, DEFAULT 1011 1111

Bit Name	Bit	Description
ADC_VOLUME2	7:0	ADC channel3/4 volume control when VOL2_SEL=1 0x00 - '-95.5dB' 0x01 - '-95dB' ⋯ 0.5dB/step 0xBE - '-0.5dB' 0xBF - '0dB' (default) 0xC0 - '+0.5dB' ⋯ 0xFF - '+32dB'

REGISTER 0X2E-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC_RAMCLR	6	ADC ram clear when lrck/adc_mclk active Note: freezed HPF '-offset' will be cleared
VOL2_SEL	5	ADC channel3/4 volume select 0 - channel3/4 volume is ADC_VOLUME1(default) 1 - channel3/4 volume is ADC_VOLUME2
ADC12_ZEROCROSS	4	ADC volume control zerocross from ADC_VOLUME1 0 - normal(default) 1 - zerocross on
ADC_RAMPRATE	3:0	ADC Volume Control ramp rate 0 - disable softramp(default) 1 - 0.25dB/4LRCK 2 - 0.25dB/8LRCK 3 - 0.25dB/16LRCK 4 - 0.25dB/32LRCK 5 - 0.25dB/64LRCK 6 - 0.25dB/128LRCK 7 - 0.25dB/256LRCK 8 - 0.25dB/512LRCK 9 - 0.25dB/1024LRCK 10 - 0.25dB/2048LRCK 11 - 0.25dB/4096LRCK 12 - 0.25dB/8192LRCK 13 - 0.25dB/16384LRCK 14 - 0.25dB/32768LRCK 15 - 0.25dB/65536LRCK Note: ALC ramp down use ADC_RAMPRATE; ramp up use ALC_WINSIZE

REGISTER 0X2F –NOT USED, DEFAULT 00000000

Bit Name	Bit	Description

REGISTER 0X30 - NOT USED, DEFAULT 00000000

Bit Name	Bit	Description

REGISTER 0X31- NOT USED, DEFAULT 00000000

Bit Name	Bit	Description

REGISTER 0X32-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ALC_EN	3	ADC auto level control 0 - ALC disable(default) 1 - ALC enable
ALC_LIMIT	2	ADC limit mode when ALC enable 0 - ALC normal mode(default) 1 - limit mode, fast gain down with LRCK when over target
ALC_RECOVERY	1:0	ALC fast gain recovery control(at gain up only) 0 -0.125dB/alc_winsize (default) 1 -0.375dB/alc_winsize 2 -0.625dB/alc_winsize

		3 -0.875dB/alc_winsize

REGISTER 0X33-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ALC_WINSIZE	7:4	ALC winsize selection cnt_timer[ALC_WINSIZE] 0 - 0.25dB/2LRCK(default) 1 - 0.25dB/4LRCK ... 15 - 0.25dB/65536LRCK Note: ALC ramp down use ADC_RAMPRATE; ramp up use ALC_WINSIZE
ALC_LEVEL	3:0	ALC target level 0 - '-30.0dB' (default) 1 - '-27.0dB' 2 - '-24.0dB' 3 - '-21.0dB' 4 - '-19.0dB' 5 - '-17.0dB' 6 - '-15.0dB' 7 - '-13.5dB' 8 - '-12.0dB' 9 - '-10.5dB' 10 - '-9.0 dB' 11 - '-7.5 dB' 12 - '-6.0 dB' 13 - '-4.5 dB' 14 - '-3.0 dB' 15 - '-1.5 dB'

REGISTER 0X34-ADC CONTROL, DEFAULT 00101100

Bit Name	Bit	Description
ADC_HPF	5	ADC offset freeze 0 - freeze offset(default) 1 - dynamic HPF
ADC_HPFS1	4:0	ADCHPF stage1 coeff 0x1F,0x0F is disable HPF 0x0C (default)

REGISTER 0X35-ADC CONTROL, DEFAULT 00001100

Bit Name	Bit	Description
ADC_HPFS2	4:0	ADCHPF stage2 coefficient 0x1F,0x0F is disable HPF 0x0C (default)

REGISTER 0X36-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC_EQEN	6	ADC EQ enable 0 - Disable(default) 1 - Enable
ADCEQ_B0[29:24]	5:0	30-bit B0 coefficient for ADCEQ

REGISTER 0X37-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B0[23:16]	7:0	30-bit B0 coefficient for ADCEQ

REGISTER 0X38-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B0[15:8]	7:0	30-bit B0 coefficient for ADCEQ

REGISTER 0X39-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B0[7:0]	7:0	30-bit B0 coefficient for ADCEQ

REGISTER 0X3A-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B1[29:24]	5:0	30-bit B1 coefficient for ADCEQ

REGISTER 0X3B-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B1[23:16]	7:0	30-bit B1 coefficient for ADCEQ

REGISTER 0X3C-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B1[15:8]	7:0	30-bit B1 coefficient for ADCEQ

REGISTER 0X3D-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B1[7:0]	7:0	30-bit B1 coefficient for ADCEQ

REGISTER 0X3E-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B2[29:24]	5:0	30-bit B2 coefficient for ADCEQ

REGISTER 0X3F-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B2[23:16]	7:0	30-bit B2 coefficient for ADCEQ

REGISTER 0X40 -ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B2[15:8]	7:0	30-bit B2 coefficient for ADCEQ

REGISTER 0X41-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_B2[7:0]	7:0	30-bit B2 coefficient for ADCEQ

REGISTER 0X42-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description

ADCEQ_A1[29:24]	5:0	30-bit A1 coefficient for ADCEQ

REGISTER 0X43-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_A1[23:16]	7:0	30-bit A1 coefficient for ADCEQ

REGISTER 0X44-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_A1[15:8]	7:0	30-bit A1 coefficient for ADCEQ

REGISTER 0X45-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_A1[7:0]	7:0	30-bit A1 coefficient for ADCEQ

REGISTER 0X46-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_A2[29:24]	5:0	30-bit A2 coefficient for ADCEQ

REGISTER 0X47-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_A2[23:16]	7:0	30-bit A2 coefficient for ADCEQ

REGISTER 0X48-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_A2[15:8]	7:0	30-bit A2 coefficient for ADCEQ

REGISTER 0X49-ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADCEQ_A2[7:0]	7:0	30-bit A2 coefficient for ADCEQ

REGISTER 0X4A-DAC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
CAL_DIS	7	DAC offset calibration control 0 - calibration enable(default) 1 - calibration disable Keep offset to HPL_OFFSET_INI and HPR_OFFSET_INIwhen calibration disable
CAL_TIMER	6:4	Calibration timer selection 0 - 127*fs(default) 1 - 255*fs 2 - 511*fs 3 - 1023*fs 4 - 2047*fs 5 - 4095*fs 6 - 8191*fs 7 - 16383*fs
OFFSET_FORCEL	3	Force left offset as HPL_OFFSET_INI 0 - auto (default) 1 - force left output to HPL_OFFSET_INI

OFFSET_FORCER	2	Force right offset as HPR_OFFSET_INI 0 - auto (default) 1 - force right output to HPR_OFFSET_INI
CAL_WAIT	1:0	Calibrationwaitcycles 0 - 31*fs(default) 1 - 63*fs 2 - 127*fs 3 - 255*fs Note: the time of CAL_TIMER should longer than CAL_WAIT

REGISTER 0X4B-DAC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
HPL_OFFSET_INI	7:0	DAC left channel offset initial 0 - no offset (default) ... HPL_OFFSET_INI * 2^(-12) Note: 0.3mv/step at 3.3v and 0.15mv/step at 1.8v

REGISTER 0X4C-DAC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
HPR_OFFSET_INI	7:0	DAC right channel offset initial 0 - no offset (default) ... HPR_OFFSET_INI * 2^(-12) Note: 0.3mv/step at 3.3v and 0.15mv/step at 1.8v

REGISTER 0X4D-DAC CONTROL, DEFAULT 00001000

Bit Name	Bit	Description
DAC_DATASEL	7:6	DAC data select 0 - output L - R(default) 1 - output L - L 2 - output R - R 3 - output R - L
DAC_INV	5:4	dac data invert 0 - normal (default) 1 - right invert 2 - left invert 3 - 2 channels invert
DAC_DSMCLIP	3	DSM clip when dsm overflow 0 - no clip 1 - clip (default)
DAC_DSMMUTE	2	dacdsm mute control 0: dacdsm unmute(default) 1: dacdsm mute
DAC_DEMMUTE	1	dac dem mute control 0 :dac dem unmute(default) 1 : dac dem mute
DAC_RAMCLR	0	dac ram clear when lrck/dac_mclk active

REGISTER 0X4E-DAC CONTROL, DEFAULT 00100000

Bit Name	Bit	Description
CROSSTALK1[4]	5	anti-crosstalk bit4, sign bit of CROSSTALK1[4:0]

CROSSTALK2[4]	4	anti-crosstalk bit4,sign bit of CROSSTALK2[4:0]
DAC_RAMPRATE	3:0	DAC Volume Control ramp rate 0 - disable softramp(default) 1 - 0.25dB/4LRCK 2 - 0.25dB/8LRCK 3 - 0.25dB/16LRCK 4 - 0.25dB/32LRCK 5 - 0.25dB/64LRCK 6 - 0.25dB/128LRCK 7 - 0.25dB/256LRCK 8 - 0.25dB/512LRCK 9 - 0.25dB/1024LRCK 10 - 0.25dB/2048LRCK 11 - 0.25dB/4096LRCK 12 - 0.25dB/8192LRCK 13 - 0.25dB/16384LRCK 14 - 0.25dB/32768LRCK 15 - 0.25dB/65536LRCK Note: DRC ramp down use DAC_RAMPRATE; ramp up use DRC_WINSIZE

REGISTER 0X4F-DAC CONTROL, DEFAULT 00010101

Bit Name	Bit	Description
DAC_DITHER_OFF	7	DAC dsm dither control 0 - Dither on (default) 1 - Dither off
DAC_PHASE	6:5	DAC phase delay 0 - sync with LRCK(default) 1 - 1/4 delay of LRCK 2 - 2/4 before of LRCK 3 - 1/4 before of LRCK
DAC_VPPSCALE	4:0	DAC output scale out = out +/- out>> DAC_VPPSCALE[3:0] DAC_VPPSCALE[4]=1 : - DAC_VPPSCALE[4]=1 : + 0x0,0x10 - not use 0x01 - +3.5dB 0x02 - +1.94dB 0x03 - +1.02dB 0x04 - +0.53dB 0x05 - +0.27dB 0x06 - +0.13dB 0x07 - +0.07dB 0x08 - +0.034dB 0x09 - +0.017dB 0x0A - +0.0085dB 0x0B - +0.0042dB 0x0C - +0.0021dB 0x0D - +0.0011dB 0x0E - +0.0005dB 0x0F - +0.0003dB 0x11 - -6dB 0x12 - -2.5dB

		0x13 - -1.16dB 0x14 - -0.56dB 0x15 - -0.28dB(default) 0x16 - -0.14dB 0x17 - -0.07dB 0x18 - -0.034dB 0x19 - -0.017dB 0x1A - -0.0085dB 0x1B - -0.0042dB 0x1C - -0.0021dB 0x1D - -0.0011dB 0x1E - -0.0005dB 0x1F - -0.0003dB

REGISTER 0X50 -DAC CONTROL,DEFAULT10111111

Bit Name	Bit	Description
DAC_VOLUME	7:0	DAC left/right channel volume control 0x00 - '-95.5dB' (default) 0x01 - '-95dB' … 0.5dB/step 0xBE - '-0.5dB' 0xBF - '0dB' 0xC0 - '+0.5dB' … 0xFF - '+32dB' Note: DAC_VOLUME is max gain when DRC enable

REGISTER 0X53-DAC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
DRC_EN	3	DAC data range control 0: DRC disable(default) 1: DRC enable
DRC_LIMIT	2	DAC limit mode when ALC enable 0 - DRC normal mode(default) 1 - limit mode, fast gain down with LRCK when over target
DRC_RECOVERY	1:0	DRC fast gain recovery control(at gain up only) 0 -0.125dB/drc_winsize (default) 1 -0.375dB/drc_winsize 2 -0.625dB/drc_winsize 3 -0.875dB/drc_winsize

REGISTER 0X54-DAC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
DRC_WINSIZE	7:4	DRC winsize selection cnt_timer[DRC_WINSIZE] 0 - 0.25dB/2LRCK(default) 1 - 0.25dB/4LRCK ... 15 - 0.25dB/65536LRCK Note: DRC ramp down use DAC_RAMPRATE; ramp up use DRC_WINSIZE
DRC_LEVEL	3:0	DRC target level

		0 - '-30.0dB' (default) 1 - '-27.0dB' 2 - '-24.0dB' 3 - '-21.0dB' 4 - '-19.0dB' 5 - '-17.0dB' 6 - '-15.0dB' 7 - '-13.5dB' 8 - '-12.0dB' 9 - '-10.5dB' 10 - '-9.0 dB' 11 - '-7.5 dB' 12 - '-6.0 dB' 13 - '-4.5 dB' 14 - '-3.0 dB' 15 - '-1.5 dB'

REGISTER 0X56-GPIO, DEFAULT 00000000

Bit Name	Bit	Description
HPJACK_TIMER	7:4	HP plug in/out detect timer, timer=intclk*2^(HPJACK_TIMER+1) A plug in/out de-bounce is 32timers 0 -intclk *2（default） … 15 -intclk * 65536
BUTTON_TIMER	3:0	HP button detect timer, timer=intclk*2^(BUTTON_TIMER+1) A button de-bounce is 32 timers 0 -intclk *2（default） … 15 -intclk * 65536

REGISTER 0X57-GPIO, DEFAULT 01010100

Bit Name	Bit	Description
HPINSERT_CSM	7	CSM Jump to calibration when headphone insert 0 - jump to calibration (default) 1 - keep csm.
HPINSERT_AUTOMUTE	6	Automute HPL_OUTEN/HPR_OUTEN when HP inserted 0 - disable automute 1 - enable automute(default)
HPINSERT_SEL	5:4	HeadPhone INSERT detect source 0 – HPINSERT detect disable 1 – HPINSERT detect by pin9/HEADSET (default) 2 – HPINSERT detect by pin27/SDINOUT3 3 – HPINSERT detect by pin9 or pin27: any of the plug in will detect as an inserting; all of the pull out will detect as a release inserting.
HPJACK_POL	3	Define the level of HP plug in/out 0 -plug in = ‘high level’; plug out = ‘low level’ (default) 1 -plug in = ‘low level’; plug out = ‘high level’
BUTTON_POL	2	Define the level of button 0 -button on = ‘high level’; button off = ‘low level’ 1 -button on = ‘low level’; button off = ‘high level’ (default)
HP_TYPE	1:0	Headphone type select

		0 -auto, select high impedance configure(default) 1-Not use 2 -force HP_SW=0: GMS0=GND; GMS1=MIC 3-force HP_SW=1: GMS0=MIC; GMS1=GND

REGISTER 0X58-GPIO, DEFAULT 00000000

Bit Name	Bit	Description
INT_SOURCE	6:0	interrupt source bit6 - PIN27 Jack (after MIC detect) bit5 - PIN9 Jack (after MIC detect) bit4 - PIN27 Jack (don't care MIC detect) bit3 - PIN9 Jack (don't care MIC detect) bit2 - BUTTON bit1 - ADC_MOZ bit0 - DAC_MOZ default: 0000000

REGISTER 0X59-GPIO, DEFAULT 01000000

Bit Name	Bit	Description
HPDET_KEYOFF	6	Detect HP type after a button release 0 - not detection 1 - detect after button release(default)
HPDET_AGAIN	5	Detect HP type again 0 - not detect again 1 - detect HP type again when this bit switch to 1 from 0.
INTOUT_INV	4	Invert INTOUT 0 - normal(default) 1 - invert
INTOUT_IO	3:0	INTOUT I/O control 0 - interrupt pulse out with 512*intclk (default) 1 - interrupt pulse out with 1024*intclk 2 - interrupt pulse out with 2048*intclk 3 - interrupt pulse out with 4096*intclk 4 - interrupt pulse out with 8192*intclk 5 - interrupt pulse out with 16384*intclk 6 - interrupt pulse out with 32768*intclk 7 - interrupt pulse out with 65536*intclk 8 - mute PA out 9 - mute PA + dacmoz out 10 - DMIC clock out 11 - button flag out 12 - adcmoz flag out 13 - dacmoz flag out 14 - 0 15 - HiZ

REGISTER 0X5A-GPIO, DEFAULT 10010000

Bit Name	Bit	Description
SDINOUT1_IO	7:4	SDINOUT1 control(PIN29) 0 - 0 1 - SDIN slot0 out

		... 8 - SDIN slot7 out 9 - DMIC clock out (default) 10 - invert of DMIC clock out 11 - SDOUT2 out 12 - MUTE PA out 13 - MUTE PA + DAC_MOZ out 14 - 0 15 - 1
ADC2DAC_SEL	3	ADC data to DAC 0 - disable (default) 1 - ADC to DAC
MCLK_IO	2:0	MCLK I/O control 0 - input (default) 1 - DMIC clock out 2 - SDOUT2 out 3 - MUTE_PA out when hpjack 4 - '0' 5 - '1' 6 - MUTE_PA + FLAG_DAC_MOZ out 7 - osc_out

REGISTER 0X5B-N/A, DEFAULT 00000000

Bit Name	Bit	Description

REGISTER 0X5C-GPIO, DEFAULT 00000000

Bit Name	Bit	Description
JACK_PDN_PGA	7	Control PDN_PGA when HPJACK 0 -Not control PDN_PGA (default) 1 -force a pulse to PDN_PGA
JACK_PDN_MOD	6	Control PDN_MOD when HPJACK 0 -Not control PDN_MOD (default) 1 -force a pulse to PDN_MOD
JACK_RST_MOD	5	Control RST_MOD when HPJACK 0 -Not control RST_MOD (default) 1 -force a pulse to RST_MOD
JACK_RST_DIG	4	Control RST_DIG when HPJACK 0 -Not control RST_DIG (default) 1 -force a reset pulse to RST_DIG
JACKMUTE_SEL	3	Jack mute control selection 0 - mute without de-bounce(default) 1 - mute with de-bounce
JM_SDINOUT1	2	Mute SDINOUT1 output when jack in 0 - unmute(default) 1 - mute with jack in

REGISTER 0XF9-TEST MODE, DEFAULT 11111010

Bit Name	Bit	Description
PULLUP_BCLK	7	BCLK pull up control, the falling edge of this bit enable pullup, the rising edge of this bit disable pullup.
PULLUP_LRCK	6	LRCK pull up control, the falling edge of this bit enable pullup, the rising edge of this bit disable pullup.
PULLUP_MCLK	5	MCLK pull up control, the falling edge of this bit enable pullup, the rising edge of this bit disable pullup.
ISO_VDDA	3	Isolate VDDA at VDDD domain 0 - release isolate 1 - isolate VDDA(default)
ADC34_OFF	1	ADC3/ADC4 not use, close the 2 channels 0 - normal 1 - channel3/4 off(default)

REGISTER 0XFD-CHIP ID, DEFAULT 10000011

Bit Name	Bit	Description
CHIP_ID1	7:0	CHIP ID “1000 0011”, read only

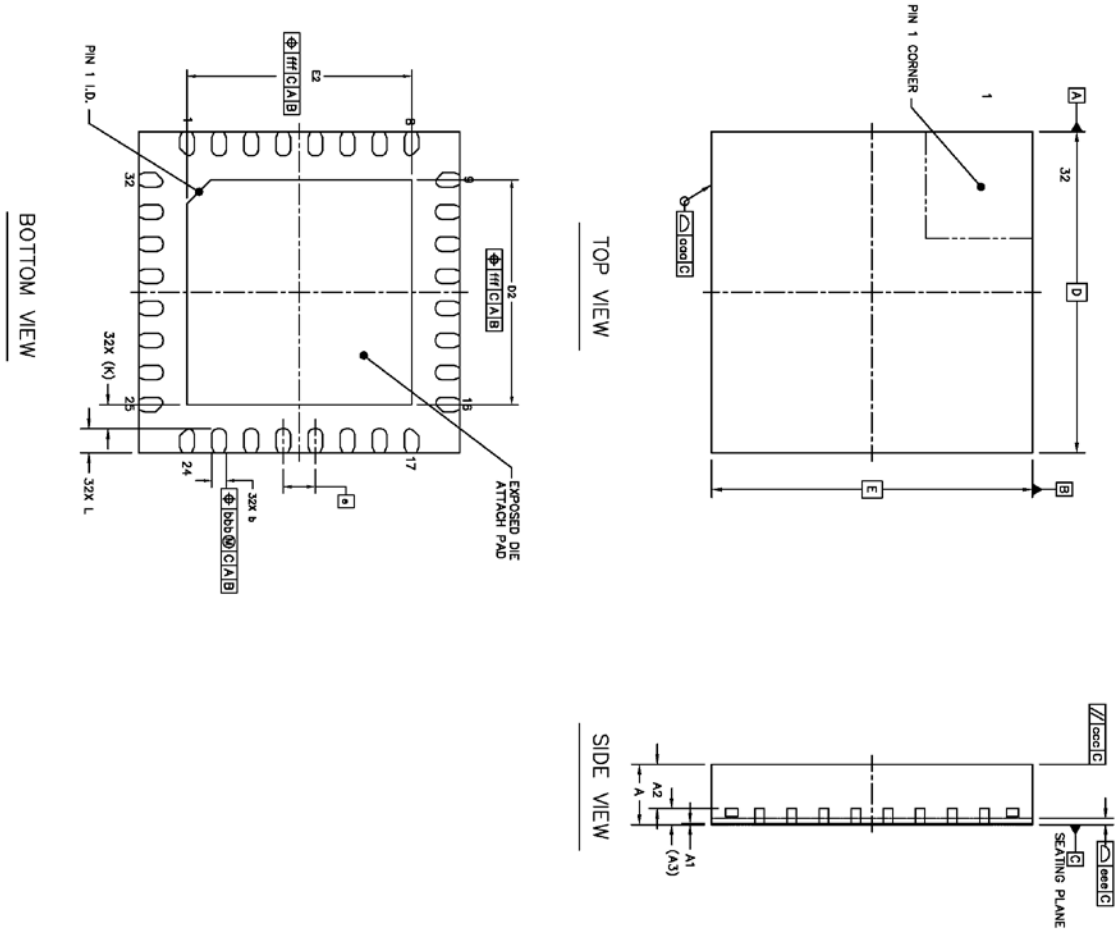
REGISTER 0XFE-CHIP ID, DEFAULT 00100110

Bit Name	Bit	Description
CHIP_ID2	7:0	CHIP ID “0010 0110”, read only

REGISTER 0XFF-CHIP ID, DEFAULT 00000000

Bit Name	Bit	Description
CHIP_VER	7:0	CHIP version, “000000”, read only

9. PACKAGE (UNIT: MM)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		4 BSC	
BODY SIZE Y	E		4 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	D2	2.7	2.8	2.9
EP SIZE Y	E2	2.7	2.8	2.9
LEAD LENGTH	L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE	K		0.3 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
LEAD OFFSET	bbb		0.1	
EXPOSED PAD OFFSET	fff		0.1	

10.CORPORATE INFORMATION

Everest Semiconductor Co., Ltd.

No. 1355 Jinjihu Drive, Suzhou Industrial Park, Jiangsu, P.R. China, Zip Code 215021

苏州工业园区金鸡湖大道 1355 号国际科技园, 邮编 215021

Email: info@everest-semi.com

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