



STN4488L

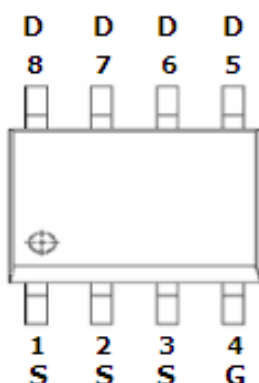


N Channel Enhancement Mode MOSFET
20.0A

DESCRIPTION

STN4488L is the N-Channel logic enhancement mode power field effect transistors which are produced using high cell density DMOS trench technology. It is suitable for the power management applications in the portable or battery powered system.

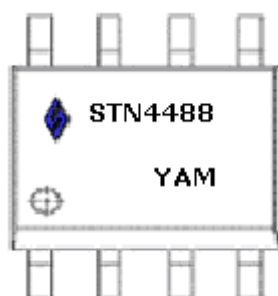
PIN CONFIGURATION SOP-8



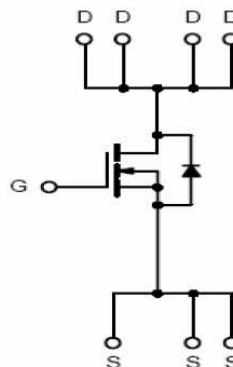
FEATURE

- 30V/20A, $R_{DS(ON)} = 3.8m\Omega$ (Typ.) @VGS = 10V
- 30V/18A, $R_{DS(ON)} = 5.2m\Omega$ @VGS = 4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

PART MARKING SOP-8



Y: Year Code
A: Week Code
M: Process Code





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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	10 Sec	Steady state	Unit
Drain-Source Voltage		V _{DSS}	30		V
Gate-Source Voltage		V _{GSS}	±20		V
Continuous Drain Current (T _J =150°C)	T _A =25°C	I _D	20	15	A
	T _A =70°C		17	12	
Pulsed Drain Current		I _{DM}	80		A
Continuous Source Current (Diode Conduction)		I _S	3.0		A
Power Dissipation	T _A =25°C	P _D	3.1	1.7	W
	T _A =70°C		20	1.1	
Operation Junction Temperature		T _J	-55/150		°C
Storage Temperature Range		T _{STG}	-55/150		°C
Thermal Resistance-Junction to Ambient		R _{θJA}	Typ	Max	°C/W
			59	75	



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ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 10	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$ $T_J=55^\circ C$			1	uA
					5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=5V, V_{GS}=10V$	80			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$ $T_J=125^\circ C$		3.8	4.6	mΩ
		$V_{GS}=4.5V, I_D=18A$		5.3	6.5	
Forward Tran Conductance	g_{fs}	$V_{DS}=10V, I_D=20A$		72		S
Diode Forward Voltage	V_{SD}	$I_S=8.0A, V_{GS}=0V$			1.0	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=10V$ $I_D=20A$		84	112	nC
Gate-Source Charge	Q_{gs}			12		
Gate-Drain Charge	Q_{gd}			21		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		5450	6800	pF
Output Capacitance	C_{oss}			760		
Reverse TransferCapacitance	C_{rss}			540		
Turn-On Time	$t_{d(on)}$	$V_{DS}=15V, R_L=0.75\Omega$ $I_D=1A, V_G=10V$ $R_G=3.0\Omega$		13		nS
	t_r			9.8		
Turn-Off Time	$t_{d(off)}$			49		
	t_f			16		

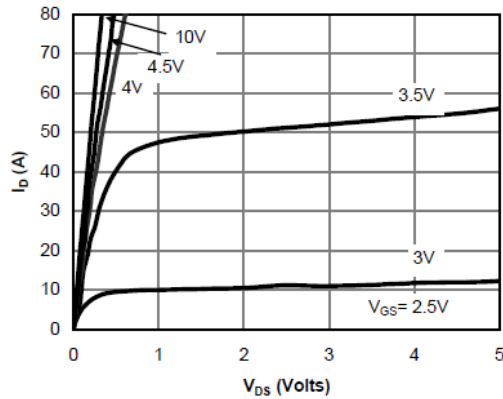
TYPICAL CHARACTERISTICS


Figure 1: On-Region Characteristics

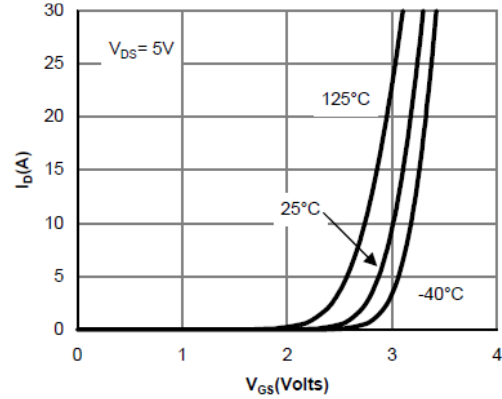


Figure 2: Transfer Characteristics

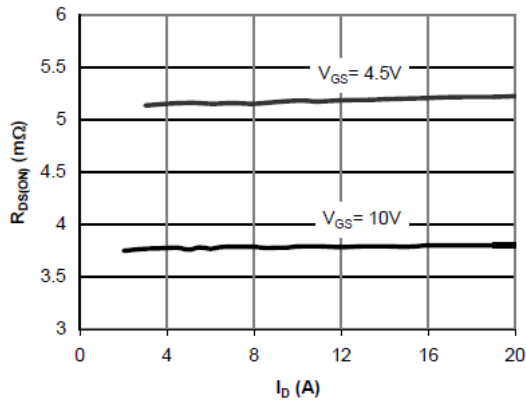


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

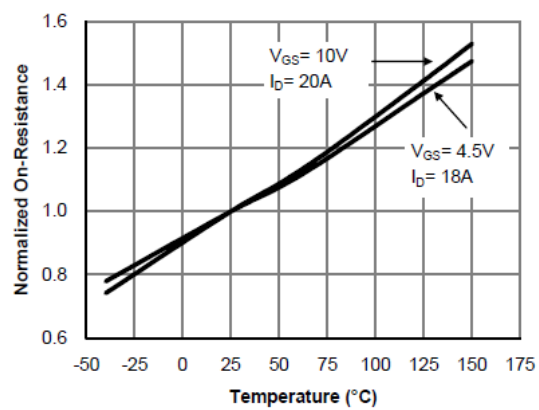


Figure 4: On-Resistance vs. Junction Temperature

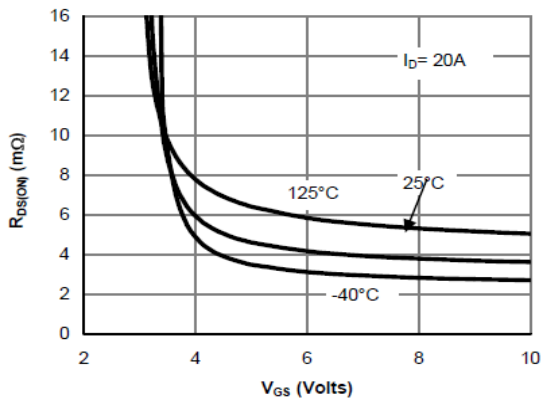


Figure 5: On-Resistance vs. Gate-Source Voltage

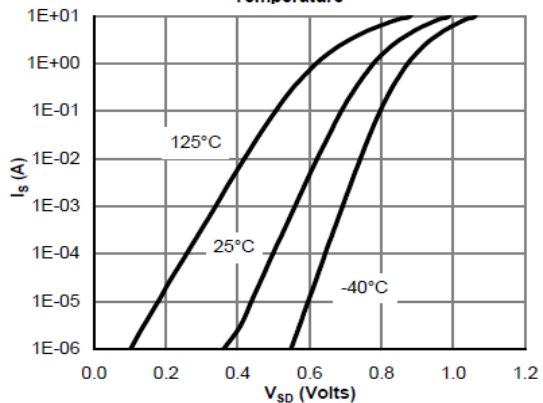
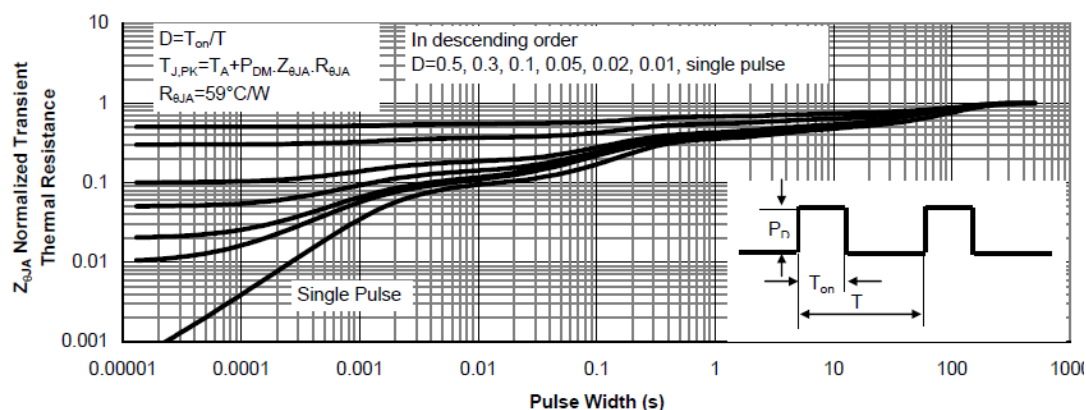
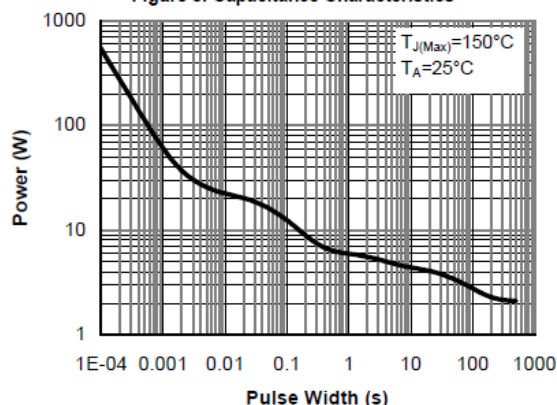
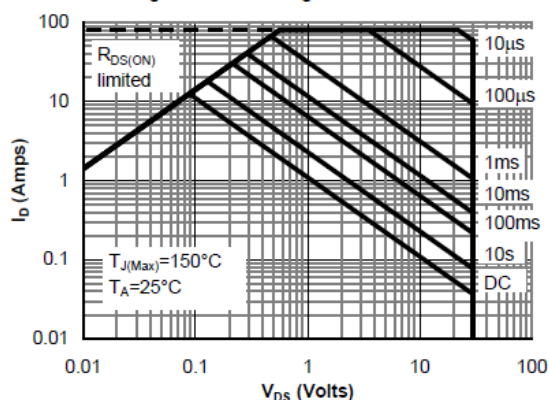
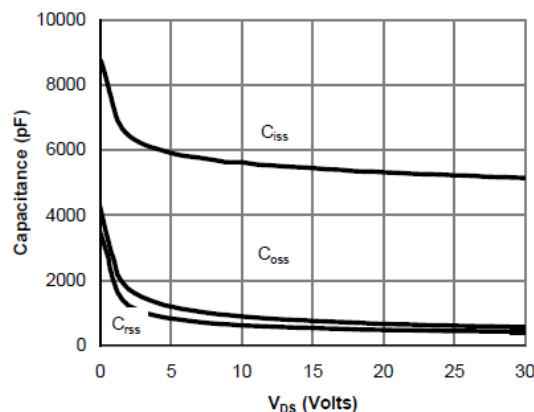
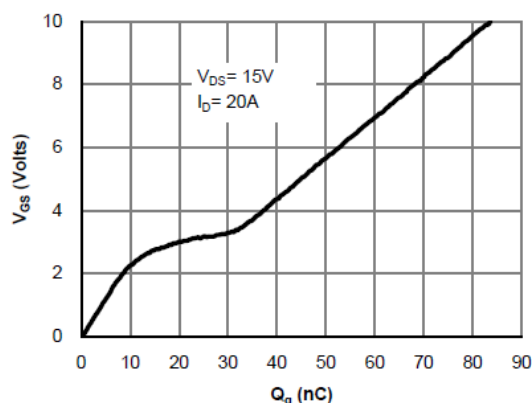
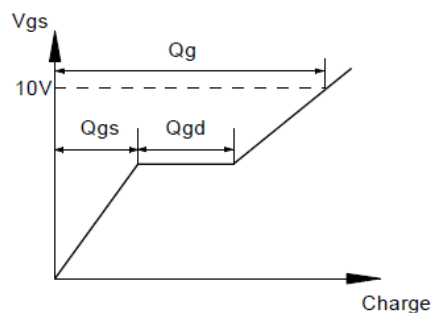
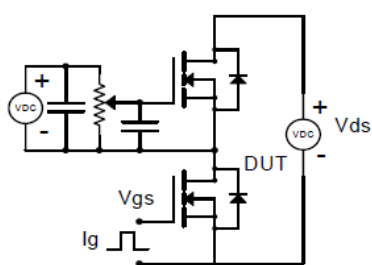


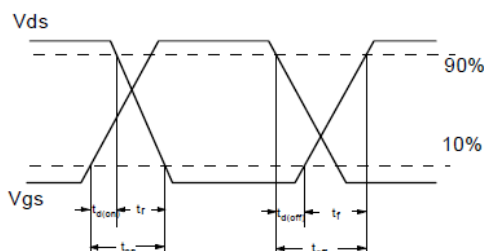
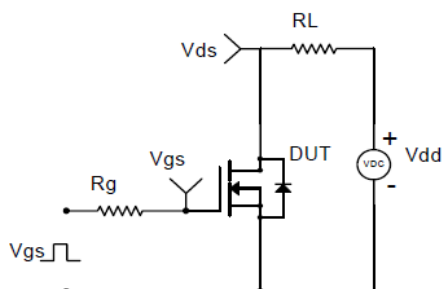
Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS


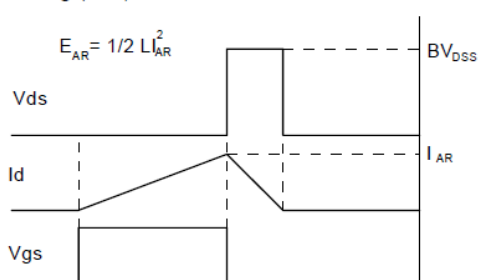
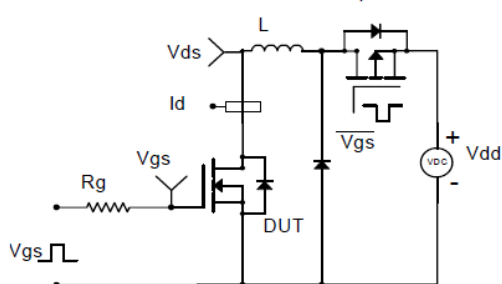
Gate Charge Test Circuit & Waveform



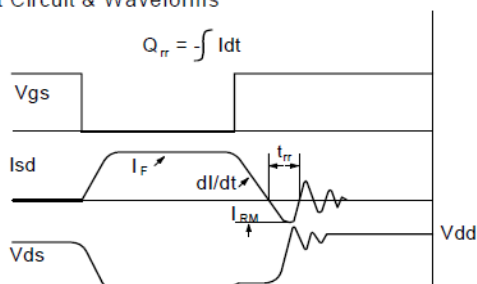
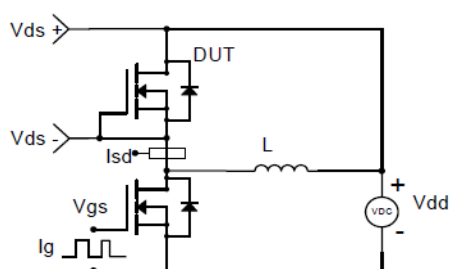
Resistive Switching Test Circuit & Waveforms

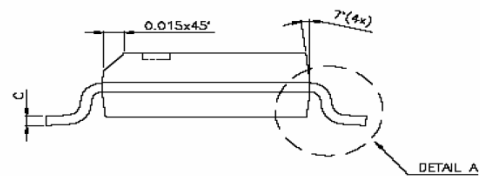
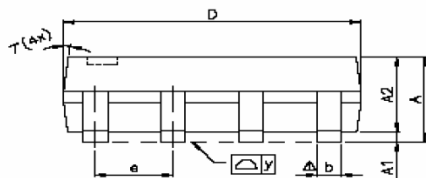
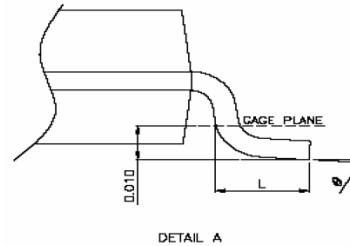
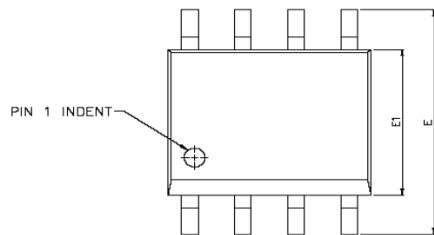


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



SOP-8 PACKAGE OUTLINE


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δy	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°