



Pin Assignments

ZXLD1370

60V HIGH ACCURACY BUCK/BOOST/BUCK-BOOST LED DRIVER-CONTROLLER WITH AEC-Q100

Description

The ZXLD1370 is an LED driver controller IC for driving external MOSFETs to drive high current LEDs. It is a multi-topology controller that efficiently controls the current through series connected LEDs. The multi-topology enables it to operate in buck, boost and buckboost configurations.

The 60V capability, coupled with its multi-topology capability, enables it to be used in a wide range of applications and drive in excess of 15 LEDs in series.

The ZXLD1370 is a modified hysteretic controller using a patent pending control scheme providing high output current accuracy in all three modes of operation. High accuracy dimming is achieved through DC control and high frequency PWM control.

The ZXLD1370 uses two pins for fault diagnosis. A flag output highlights a fault, while the multi-level status pin gives further information on the exact fault.

Features

- 0.5% Typical Output Current Accuracy
- 6V to 60V Operating Voltage Range
- LED Driver Supports Buck, Boost and Buck-Boost Configurations
- Wide Dynamic Range Dimming
- 20:1 DC Dimming
- 1000:1 Dimming Range at 500Hz
- Up to 1MHz Switching
- High Temperature Control of LED Current Using TADJ
- Available in Automotive Grade with AEC-Q100 and TS16949
 Certification
- Available in "Green" Molding Compound (No Br, Sb) with Lead Free Finish/ RoHS Compliant
 - Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
 - Halogen and Antimony Free. "Green" Device (Note 3)
- An Automotive-Compliant Part is Available Under Separate Data Sheet (ZXLD1370Q)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.

See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.









Typical Applications Circuit



Functional Block Diagram





Pin Descriptions

ADJ 1 Adjust Input (for DC Output Current Control) Connect to REF to set 10% output current. ADJ 1 1 Drive with dc voltage (125mV 2.5V) to adjust output current from 10% to 20% of set value. The ADJ pin has an internal clamp that limits the internal node to less than 3V. This provides some fielded schould they get overdriven. TADJ 3 1 Temperature Adjust Input for LED Thermal Current Control Connect to REF to disable thermal current to this pin to reduce output current above a preset temperature threshold. SHP 4 I/O Shaping Capacitor for Feedback Control Loop Connect to REF to disable thermal current Loop STATUS 5 O Pin sint 4.5V (noninal) during normal operation. Pin sint 4.5V (noninal) during normal operation. Pin sint 4.5V (noninal) during normal operation. STATUS 5 O Pin sint 4.5V (noninal) during normal operation. STATUS 5 O Pin sint during normal operation. VRC 8 — Not Connected Internally - recommend connection to pin 7. (PGND), to maximize PCB copper for thermal dissipation. NC 8 — Not Connected Internally - recommend connection pin 10 (GATE) to permit wide copper trace to gate of MOSFET. GATE 0 Gate Drive Cuputo to Steven MMOS	Pin Name	Pin	Type (Note 4)	Function
The ADJ pin has an internal clamp that limits the internal node to less than 3V. This provides some fallsafe should they get overdriven. REF 2 O Internal 1.25V Reference Voltage Output TADJ 3 I Temperature Adjust Input for LED Thermal Current Control Connect to REF to disable thermal compensation function (see section on Thermal Control). SHP 4 I/O Shaping Capacitor for Feedback Control Loop Connect 100pF ±20% capacitor for Internal to privide loop compensation. STATUS 5 O Pin is at 4.5V (norminal) during normal operation. Pin is at 4.5V (norminal) during normal operation. Pin is at 4.5V (norminal) during normal operation. Pin sit these to a lower voltage to indicate specific operation warnings or fault conditions (see section on STATUS output). Status Divoltage is low during shutdown mode. SGND 6 P Signal Ground - Connect to 0V PGND 7 P Power Ground - Connect to 0V and pin 8 to maximize copper area. N/C 8 — Not Connected Internally – recommend connection to pin 10 (GATE) to permit wide copper trace to gate to driMOSFET. Valux 11 P O Gate Drive Output to External NMOS Transistor – connect to pin 9 Valux 11 P Imped Supply to Drive Output to External Swich Gate Driver Va				
TADJ 3 I Temperature Adjust Ipput for LED Thermal Current Control SHP 4 I/O Connect to REF to disable thermal compensation function (see section on Thermal Control). SHP 4 I/O Shaping Capacitor for Feedback Control Loop Connect to REF to disable thermal compensation function (see section on Thermal Control). Operation Status Output (Analog Output) STATUS 5 O Pin switches to a lower voltage to indicate specific operation warnings or fault conditions (see section on STATUS output). SGND 6 P Signal Ground - Connect to 0V and pin 8 to maximize copper area. N/C 8 — Not Connected Internally – recommend connection to pin 7. (PGND). to maximize PCB copper for thermal dissipation. N/C 9 — Not Connected Internally – recommend connection pin 10 (GATE) to permit wide copper trace to gate of MOSFET. GATE 10 O Gate Drive Output to External NMOS Transistor – connect to pin 9 Vaux 11 P Connect to Vin, or auxiliary supply from 6V to 15V supply to reduce internal power dissipation (refer to Application Section run rol avaliary supply from 6V to 15V supply to reduce internal power dissipation (refer to Application section). Vin 12 P Connect to Vin, or auxiliary supply from 6V to 15V supply to reduce internal p	ADJ	1	I	The ADJ pin has an internal clamp that limits the internal node to less than 3V. This provides some
TADJ 3 I Connect themistor/resistor network to this pin to reduce output current above a preset temperature threshold. Connect to REF to disable thermal compensation function (see section on Thermal Control). SHP 4 I/O Shaping Capacitor for Feedback Control Loop STATUS 5 O Operation Status Output (Analog Output) Pin is at 4.5V (nominal) during normal operation. STATUS 5 O Pin is at 4.5V (nominal) during normal operation. Pin switches to a lower voltage to indicate specific operation warnings or fault conditions (see section on STATUS output). STATUS 5 O Signal Ground - Connect to 0V Pin switches to a lower voltage to indicate specific operation warnings or fault conditions (see section on STATUS output). SGND 6 P Signal Ground - Connect to 0V Pin switches to a lower voltage is low during shutdown mode. SGND 6 P Regrame Ground - Connect to 0V and pin 8 to maximize copper area. N/C 8 — Not Connected Internally – recommend connection pin 10 (GATE) to permit wide copper trace to gate of MOSFET. GATE 10 O Gate Drive Output to External NMOS Transistor – connect to pin 9 Vaux 11 P Auxiliary Positive Supply to I	REF	2	0	Internal 1.25V Reference Voltage Output
SHP 4 I/O Connect 100pF ±20% capacitor from this pin to ground to provide loop compensation. STATUS 5 O Operation Status Output (Analog Output) Pin is at 4.5V (normial) during normal operation. STATUS 5 O Pin switches to a lower voltage to indicate specific operation warnings or fault conditions (see section on STATUS output). SGND 6 P Signal Ground - Connect to 0V PGND 7 P Power Ground - Connect to 0V and pin 8 to maximize copper area. N/C 8 — Not Connected Internally – recommend connection to pin 7. (PGND), to maximize PCB copper for thermal dissipation. N/C 9 — Not Connected Internally – recommend connection pin 10 (GATE) to permit wide copper trace to gate of MOSFET. GATE 10 O Gate Drive Output to External NMOS Transistor – connect to pin 9 VAUX 11 P Auxiliary Positive Supply to Internal Switch Gate Driver VAUX 11 P Connect of V _N , or auxiliary supply form 6V to 15V supply to reduce internal power dissipation (refer to Application Section). VIN 12 P Input Supply to Device (6V to 60V) Decouple to ground with capacitor close to de	TADJ	3	I	Connect thermistor/resistor network to this pin to reduce output current above a preset temperature threshold.
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PGND 7 P Power Ground - Connect to 0V and pin 8 to maximize copper area. N/C 8	STATUS	5	0	Pin is at 4.5V (nominal) during normal operation. Pin switches to a lower voltage to indicate specific operation warnings or fault conditions (see section on STATUS output).
N/C 8 — Not Connected Internally – recommend connection to pin 7, (PGND), to maximize PCB copper for thermal dissipation. N/C 9 — Not Connected Internally – recommend connection pin 10 (GATE) to permit wide copper trace to gate of MOSFET. GATE 10 O Gate Drive Output to External NMOS Transistor – connect to pin 9 VAUX 11 P Connect to V _{NI} or auxiliary supply from 6V to 15V supply to reduce internal power dissipation (refer to Application Section for more details). Decouple to ground with capacitor close to device (refer to Applications section). V _{IN} 12 P Input Supply to Device (6V to 60V) Decouple to ground with capacitor close to device (refer to Applications section). VIN 12 P Current Monitor Input Connect current sense resistor between this pin and V _{IN} . The nominal voltage across the resistor is 225mV. FLAG 14 O Flag Open Drain Output Pin is high impedance during normal operation. Pin switches low to indicate a fault, or warning condition. Digital PWM Output Current Control PWM 15 I Digital PWM Output Current Control Dirive with frequency higher than 100Hz to gate output 'or' and 'off' during dimming control. The device enters standby mode when PWM pin is driven with logic low level for more than 15ms nominal (refer to Application Section for more details). GI	SGND	6	Р	Signal Ground - Connect to 0V
INC 8 - Ithermal dissipation. NVC 9 - Not Connected Internally – recommend connection pin 10 (GATE) to permit wide copper trace to gate of MOSFET. GATE 10 O Gate Drive Output to External NMOS Transistor – connect to pin 9 VAUX 11 P Auxiliary Positive Supply to Internal Switch Gate Driver Connect to V _{IN} , or auxiliary supply from 6V to 15V supply to reduce internal power dissipation (refer to Application Section for more details). Decouple to ground with capacitor close to device (refer to Applications section). V _{IN} 12 P Input Supply to Device (6V to 60V) Decouple to ground with capacitor close to device (refer to Applications section). ISM 13 I Connect current sense resistor between this pin and V _{IN} . The nominal voltage across the resistor is 225mV. FLAG 14 O Flag Open Drain Output Pin is high impedance during normal operation. Pin switches low to indicate a fault, or warning condition. PWM 15 I Digital PWM Output Current Control Pin is driven either by open drain or push-pull, 3.3V or 5V logic levels. Drive with frequency higher than 100Hz to gate output 'or' and 'off during dimming control. The device enters standby mode when PWM pin is driven with logic tow level for more than 15ms nominal (refer to Application Section for more details). Gl 16 I Ga	PGND	7	Р	Power Ground - Connect to 0V and pin 8 to maximize copper area.
INC 9	N/C	8	_	
VAUX 11 P Auxiliary Positive Supply to Internal Switch Gate Driver VAUX 11 P Auxiliary Supply from 6V to 15V supply to reduce internal power dissipation (refer to Application Section for more details). Decouple to ground with capacitor close to device (refer to Applications section). VIN 12 P Input Supply to Device (6V to 60V) Decouple to ground with capacitor close to device (refer to Applications section). ISM 13 I Current Monitor Input Connect current sense resistor between this pin and V _{IN} . The nominal voltage across the resistor is 225mV. FLAG 14 O Flag Open Drain Output Pin is high impedance during normal operation. Pin switches low to indicate a fault, or warning condition. PWM 15 I Digital PWM Output Current Control Pin is driven either by open drain or push-pull, 3.3V or 5V logic levels. Drive with frequency higher than 100Hz to gate output 'on' and 'off' during dimming control. The device enters standby mode when PWM pin is driven with logic low level for more than 15ms nominal (refer to Application Section for more details). GI 16 I Gain Setting Input Used to set the device in Buck mode, Boost or Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes, connect to resistive divider from ADJ to SGND. This defines the ratio of switch current to LED current (see Application Section). The GI pin has an internal clamp that limits the internal node to less than 3V. This provides some failsafe should they get overdriven.	N/C	9	—	
VAUX11PConnect to VIN, or auxiliary supply from 6V to 15V supply to reduce internal power dissipation (refer to Application Section for more details). Decouple to ground with capacitor close to device (refer to Applications section).VIN12PInput Supply to Device (6V to 60V) Decouple to ground with capacitor close to device (refer to Applications section).ISM13ICurrent Monitor Input Connect current sense resistor between this pin and VIN. The nominal voltage across the resistor is 225mV.FLAG14OFlag Open Drain Output Pin is high impedance during normal operation. Pin is witches low to indicate a fault, or warning condition. Digital PVM Output Current Control Pin is driven either by open drain or push-pull, 3.3V or 5V logic levels. Drive with frequency higher than 100Hz to gate output 'on' and 'off' during dimming control. The device enters standby mode when PWM pin is driven with logic low level for more than 15ms nominal (refer to Application Section for more details).GI16IGain Setting Input Used to set the device in Buck mode, Boost or Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boos	GATE	10	0	Gate Drive Output to External NMOS Transistor – connect to pin 9
VIN 12 P Decouple to ground with capacitor close to device (refer to Applications section). ISM 13 I Current Monitor Input Connect current sense resistor between this pin and V _{IN} . The nominal voltage across the resistor is 225mV. FLAG 14 O Flag Open Drain Output Pin is high impedance during normal operation. Pin switches low to indicate a fault, or warning condition. PWM 15 I Digital PWM Output Current Control Pin is driven either by open drain or push-pull, 3.3V or 5V logic levels. Drive with frequency higher than 100Hz to gate output 'on' and 'off' during dimming control. The device enters standby mode when PWM pin is driven with logic low level for more than 15ms nominal (refer to Application Section for more details). GI 16 I Gain Setting Input Used to set the device in Buck mode, Boost or Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes, connect to resistive divider from ADJ to SGND. This defines the ratio of switch current to LED current (see Application Section). The GI pin has an internal clamp that limits the internal node to less than 3V. This provides some failsafe should they get overdriven.	V _{AUX}	11	Ρ	Connect to V_{IN} , or auxiliary supply from 6V to 15V supply to reduce internal power dissipation (refer to Application Section for more details).
ISM 13 I Connect current sense resistor between this pin and V _{IN} . The nominal voltage across the resistor is 225mV. FLAG 14 O Flag Open Drain Output Pin is high impedance during normal operation. Pin switches low to indicate a fault, or warning condition. PWM 15 I Digital PWM Output Current Control Pin is driven either by open drain or push-pull, 3.3V or 5V logic levels. Drive with frequency higher than 100Hz to gate output 'on' and 'off' during dimming control. The device enters standby mode when PWM pin is driven with logic low level for more than 15ms nominal (refer to Application Section for more details). GI 16 I Gain Setting Input Used to set the device in Buck mode, Boost or Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes, connect to resistive divider from ADJ to SGND. This defines the ratio of switch current to LED current (see Application Section). The GI pin has an internal clamp that limits the internal node to less than 3V. This provides some failsafe should they get overdriven.	V _{IN}	12	Р	
FLAG14OPin is high impedance during normal operation. Pin switches low to indicate a fault, or warning condition.PWM15IDigital PWM Output Current Control Pin is driven either by open drain or push-pull, 3.3V or 5V logic levels. Drive with frequency higher than 100Hz to gate output 'on' and 'off' during dimming control. The device enters standby mode when PWM pin is driven with logic low level for more than 15ms nominal (refer to Application Section for more details).GI16IGI16IGIIGain Setting Input Used to set the device in Buck mode, Boost or Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes, connect to resistive divider from ADJ to SGND. This defines the ratio of switch current to LED current (see Application Section). The GI pin has an internal clamp that limits the internal node to less than 3V. This provides some failsafe should they get overdriven.	ISM	13	I	Current Monitor Input Connect current sense resistor between this pin and V _{IN} .
PWM 15 I Pin is driven either by open drain or push-pull, 3.3V or 5V logic levels. Drive with frequency higher than 100Hz to gate output 'on' and 'off' during dimming control. The device enters standby mode when PWM pin is driven with logic low level for more than 15ms nominal (refer to Application Section for more details). GI 16 I Gain Setting Input Used to set the device in Buck mode, Boost or Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes, connect to resistive divider from ADJ to SGND. This defines the ratio of switch current to LED current (see Application Section). The GI pin has an internal clamp that limits the internal node to less than 3V. This provides some failsafe should they get overdriven.	FLAG	14	0	Pin is high impedance during normal operation.
GI 16 I Used to set the device in Buck mode, Boost or Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes, connect to resistive divider from ADJ to SGND. This defines the ratio of switch current to LED current (see Application Section). The GI pin has an internal clamp that limits the internal node to less than 3V. This provides some failsafe should they get overdriven.	PWM	15	I	Pin is driven either by open drain or push-pull, 3.3V or 5V logic levels. Drive with frequency higher than 100Hz to gate output 'on' and 'off' during dimming control. The device enters standby mode when PWM pin is driven with logic low level for more than 15ms
EP PAD P Exposed Paddle – Connect to 0V plane for electrical and thermal management.	GI	16	I	Used to set the device in Buck mode, Boost or Buck-Boost modes. Connect to ADJ in Buck mode operation. For Boost and Buck-Boost modes, connect to resistive divider from ADJ to SGND. This defines the ratio of switch current to LED current (see Application Section). The GI pin has an internal clamp that limits
	EP	PAD	P	Exposed Paddle – Connect to 0V plane for electrical and thermal management.

Note: 4. Type refers to whether or not pin is an Input, Output, Input/Output or Power Supply pin.



Symbol	Parameter	Rating	Unit
V _{IN}	Input Supply Voltage Relative to GND	-0.3 to +65	V
V _{AUX}	Auxiliary Supply Voltage Relative to GND	-0.3 to +65	V
VISM	Current Monitor Input Relative to GND	-0.3 to +65	V
V _{SENSE}	Current Monitor Sense Voltage (VIN-VISM)	-0.3 to +5	V
V _{GATE}	Gate Driver Output Voltage	-0.3 to +20	V
IGATE	Gate Driver Continuous Output Current	18	mA
V _{FLAG}	Flag Output Voltage	-0.3 to 40	V
V _{PWM} , V _{ADJ} , V _{TADJ} , V _{GI}	Other Input Pins	-0.3 to +5.5	V
TJ	Maximum Junction Temperature	150	°C
T _{ST}	Storage Temperature	-55 to +150	°C

Absolute Maximum Ratings (Note 5) (Voltages to GND, unless otherwise specified.)

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Package Thermal Data

Thermal Resistance	Package	Typical	Unit
Junction-to-Ambient, θ _{JA} (Note 6)	TSSOP-16EP	50	°C/W
Junction-to-Case, θ_{JC}	TSSOP-16EP	23	°C/W

Notes: 5. For correct operation SGND and PGND should always be connected together.

6. Measured on High Effective Thermal Conductivity Test Board" according JESD51.



Symbol Parameter Performance/Comment Mit Normal Operation 8

Symbol	Parameter	Performance/Comment	Min	Max	Unit
		Normal Operation	8		
V _{IN}	Input Supply Voltage Range	Reduced Performance Operation (Note 7)	6.3	60	V
		Normal Operation	8		
V _{AUX}	Auxiliary Supply Voltage Range (Note 8)	Reduced Performance Operation (Note 7)	6.3	60	V
VISM	Current Sense Monitor Input Range	—	6.3	60	V
VSENSE	Differential Input Voltage	V_{VIN} - V_{ISM} , with $0 \le V_{ADJ} \le 2.5$	0	450	mV
V _{ADJ}	External dc Control Voltage Applied to ADJ Pin to Adjust Output Current	DC Brightness Control Mode from 10% to 200%	0.125	2.5	V
I _{REF}	Reference External Load Current	REF Sourcing Current		1	mA
f _{MAX}	Recommended Switching Frequency Range (Note 9)	—	300	1,000	kHz
Vtadj	Temperature Adjustment (T _{ADJ}) Input Voltage Range	—	0	V _{REF}	V
4	Recommended PWM Dimming Frequency Range	To Achieve 1000:1 Resolution	100	500	Hz
f _{PWM}	Recommended FWW Dimining Frequency Range	To Achieve 500:1 Resolution	100	1,000	Hz
t _{PWMH/L}	PWM Pulse Width in Dimming Mode	PWM Input High or Low	0.002	10	ms
V _{PWMH}	PWM Pin High Level Input Voltage	—	2	5.5	V
V _{PWML}	PWM Pin Low Level Input Voltage	_	0	0.4	V
TJ	Operating Junction Temperature Range	—	-40	125	°C
GI	Gain Setting Ratio for Boost and Buck-Boost Modes	Ratio = V _{GI} /V _{ADJ}	0.20	0.50	

Notes: 7. Device starts up above 6V and as such the minimum applied supply voltage has to be above 6.5V (plus any noise margin). The ZXLD1370 will, however, continue to function when the input voltage is reduced from ≥ 8V down to 6.3V.

When operating with input voltages below 8V the output current and device parameters may deviate from their normal values; and is dependent on power MOSFET switch, load and ambient temperature conditions. To ensure best operation in Boost and Buck-Boost modes with input voltages, V_{IN}, between 6.3 and 8V a suitable boot-strap network on V_{AUX} pin is recommended.

Performance in Buck mode will be reduced at input voltages (VIN, VAUX) below 8V – a boot-strap network cannot be implemented in buck mode. And so a suitable low VT MOSFET should be selected.

8. VAUX can be driven from a voltage higher than VIN to provide higher efficiency at low VIN voltages, but to avoid false operation; a voltage should not be applied to VAUX in the absence of a voltage at VIN.

9. The device contains circuitry to control the switching frequency to approximately 400kHz. The maximum and minimum operating frequency is not tested in production.



Electrical Characteristics (Note 5) ($V_{IN} = V_{AUX} = 12V$, $T_A = +25^{\circ}C$, unless otherwise specified.)

Symbol	Parameter	Condition	s	Min	Тур	Max	Units
Supply and R	Reference Parameters						
V _{UV-}	Undervoltage Detection Threshold Normal Operation to Switch Disabled	V _{IN} or V _{AUX} Falling		5.2	5.6	6.3	V
V _{UV+}	Undervoltage Detection Threshold Switch Disabled to Normal Operation	V _{IN} or V _{AUX} Rising		5.5	6.0	6.5	V
I _{Q-IN}	Quiescent Current into VIN	PWM Pin Floating		—	1.5	3.0	mA
I _{Q-AUX}	Quiescent Current into V _{AUX}	Output Not Switching		_	150	300	μA
I _{SB-IN}	Standby Current into V _{IN}	PWM Pin Grounded		_	90	150	μA
I _{SB-AUX}	Standby Current into V _{AUX}	for more than 15ms		_	0.7	10.0	μA
V _{REF}	Internal Reference Voltage	No Load		1.237	1.250	1.263	V
	Change in Reference Voltage with Output	Sourcing 1mA		-5			mV
ΔV_{REF}	Current	Sinking 100µA		_	_	5	mv
VREF_LINE	Reference Voltage Line Regulation	$V_{IN} = V_{AUX}, 6.5V < V_{IN} =$	<60V	-60	-90	_	dB
V _{REF-TC}	Reference Temperature Coefficient	-		_	+/-50	_	ppm/°C
DC-DC Conve	erter Parameters						
V _{ADJ}	External DC control voltage applied to ADJ pin to adjust output current (Note 8)	DC Brightness Control I 10% to 200%	Vode	0.125	1.25	2.50	V
I _{ADJ}	ADJ Input Current (Note 10)	$V_{ADJ} \le 2.5V$ $V_{ADJ} = 5.0V^{\dagger}$		_	_	100 5	nA μA
V _{GI}	GI Voltage threshold for boost and buck-boost modes selection (Note 8)	V _{ADJ} = 1.25V		_		0.8	V
I _{GI}	GI Input Current (Note 10)	V _{GI} ≤ 2.5V V _{GI} = 5.0V [†]		—	—	100 5	nA μA
IPWM	PWM Input Current	V _{PWM} = 5.5V		_	36	100	μA
t PWMOFF	PWM Pulse Width (to enter shutdown state)	PWM Input Low		10	15	25	ms
T _{SDH}	Thermal Shutdown Upper Threshold (GATE output forced low)	Temperature Rising		—	150	_	°C
T _{SDL}	Thermal Shutdown Lower Threshold (GATE output re-enabled)	Temperature Falling		_	125		°C
High-Side Cu	rrent Monitor (Pin ISM)	•	1				
I _{ISM}	Input Current	@ V _{ISM} = 12V		_	11	20	μA
		Buck			218	_	
VSENSE	Current Measurement Sense Voltage		/ _{ADJ} = 1.25V		225	_	mV
		Buck-Boost (Note 11)		_			0/
V _{SENSE_ACC}	Accuracy of Nominal V _{SENSE} Threshold Voltage	V _{ADJ} = 1.25V	ŀ		±0.25	±2	%
V _{SENSE-OC}	Overcurrent Sense Threshold Voltage			300	350	375	mV

Notes: 10. The ADJ and GI pins have an internal clamp that limits the internal node to less than 3V. This provides some failsafe should those pins get overdriven. 11. Initial sense voltage in Boost and Buck-Boost modes at maximum duty cycle.



Symbol	Parameter	Conditions		Min	Тур	Max	Units
Output Para	imeters	•					•
V _{FLAGL}	FLAG Pin Low Level Output Voltage	Output sinking 1mA		_	_	0.5	V
I _{FLAGOFF}	FLAG Pin Open Drain Leakage Current	V _{FLAG} = 40V		_	_	1	μA
		Normal Operation		4.2	4.5	4.8	
		Out of Regulation (V _{SHP} (Note 13)	Out of Range)	3.3	3.6	3.9	
	STATUS Flag No-Load Output Voltage	V _{IN} Undervoltage (V _{IN} <	5.6V)	3.3	3.6	3.9	v
V _{STATUS}	(Note 12)	Switch Stalled (ton or to	_{FF} > 100µs)	3.3	3.6	3.9	v
		Overtemperature (T _J > +	-125°C)	1.5	1.8	2.1	
		Excess Sense Resistor Current (V _{SENSE} > 0.32V)		0.6	0.9	1.2	
R _{STATUS}	Output Impedance of STATUS Output	Normal Operation			10		kΩ
Driver Outp	ut (PIN GATE)						•
M	High Level Output Voltage		$V_{IN} = V_{AUX} = 12V$	9.5	11	— ,	v
V _{GATEH}			$V_{IN} = V_{AUX} = 6.5V$	4	5.5	_	v
VGATEL	Low Level Output Voltage	Sinking 1mA, (Note 15)			—	0.5	V
VGATECL	High Level GATE CLAMP Voltage	$V_{IN} = V_{AUX} = V_{ISM} = 18V$ $I_{GATE} = 1mA$		_	12.8	15.0	V
I _{GATE}	Dynamic peak current available during rise or fall of output voltage	Charging or Discharging Switch with $Q_G = 10nC$ a		_	±300	_	mA
t _{STALL}	Time to assert 'STALL' flag and warning on STATUS output (Note 16)	GATE low or high		_	100	170	μs
LED Therm	al Control Circuit (T _{ADJ}) Parameters						
V _{TADJH}	Upper Threshold Voltage	Onset of Output Current (V _{TADJ} Falling)	t Reduction	560	625	690	mV
VTADJL	Lower Threshold Voltage	Output Current Reduced Value (V _{TADJ} Falling)	d to <10% of Set	380	440	500	mV
I _{TADJ}	T _{ADJ} Pin Input Current	V _{TADJ} = 1.25V		_	_	1	μA

Electrical Characteristics (Continued) (VIN = VAUX = 12V, TA = +25°C, unless otherwise specified.)

12. In the event of more than one fault/warning condition occurring, the higher priority condition will take precedence. E.g. 'Excessive coil current' and 'Out of regulation' occurring together will produce an output of 0.9V on the STATUS pin. The voltage levels on the STATUS output assume the Notes: Internal regulator to be in regulation and V_{ADJ}<=V_{REF}. A reduction of the voltage on the STATUS pin will occur when the voltage on V_{IN} is near the minimum value of 6V.

13. Flag is asserted if V_{SHP}<2.5V or V_{SHP}>3.5V

14. GATE is switched to the supply voltage VAUX for low values of VAUX (i.e. between 6V and approximately 12V). For VAUX>12V, GATE is clamped internally to prevent it exceeding 15V. Below 12V the minimum gate pin voltage will be 2.5V below Vaux. 15. GATE is switched to PGND by an NMOS transistor

16. If tON exceeds tSTALL, the device will force GATE low to turn off the external switch and then initiate a restart cycle. During this phase, ADJ is grounded internally and the SHP pin is switched to its nominal operating voltage, before operation is allowed to resume. Restart cycles will be repeated automatically until the operating conditions are such that normal operation can be sustained. If tOFF exceeds tSTALL, the switch will remain off until normal operation is possible.



Typical Characteristics





Typical Characteristics (Continued)







Eiguro 6	Buck-Boost LED	Curront	Switching	Froquency	V
Figure 0	DUCK-DUUSI LEL	ounem,	Switching	Frequency vs.	V AD.I





Typical Characteristics (Cont.) Buck Mode - R_S = 150mΩ, L = 33µH





Typical Characteristics (Cont.) Buck Mode – $R_S = 300m\Omega$, L = 47 μ H













Typical Characteristics (Cont.) Buck-Boost Mode – R_S = 150m Ω , GI_{RATIO} = 0.23, L = 47 μ H



Application Information

The ZXLD1370 is a high accuracy hysteretic inductive buck/boost/buck-boost controller designed to be used with an external NMOS switch for current-driving single or multiple series-connected LEDs. The device can be configured to operate in buck, boost, or buck-boost modes by suitable configuration of the external components as shown in the schematics shown in the device operation description.

Device Description

a) Buck Mode - the most simple buck circuit shown in Figure 21

Control of the LED current buck mode is achieved by sensing the coil current in the sense resistor R_S, connected between the two inputs of a current monitor within the control loop block. An output from the control loop drives the input of a comparator which drives the gate of the external NMOS switch transistor Q1 via the internal Gate Driver. When the switch is on, the drain voltage of Q1 is near zero. Current flows from V_{IN}, via R_S, LED, coil and switch to ground. The current ramps up until an upper threshold value is reached (see Figure 22). At this point, GATE goes low, the switch is turned off and the drain voltage increases to VIN plus the forward voltage, VF, of the schottky diode D1. Current flows via RS, LED, coil and D1 back to VIN. When the coil current has ramped down to a lower threshold value, GATE goes high, the switch is turned on again and the cycle of events repeats, resulting in continuous oscillation. The feedback loop adjusts the NMOS switch duty cycle to stabilize the LED current in response to changes in external conditions, including input voltage and load voltage.

The average current in the sense resistor, LED and coil is equal to the average of the maximum and minimum threshold currents. The ripple current (hysteresis) is equal to the difference between the thresholds. The control loop maintains the average LED current at the set level by adjusting the switch duty cycle continuously to force the average sense resistor current to the value demanded by the voltage on the ADJ pin. This minimizes variation in output current with changes in operating conditions.

The control loop also regulates the switching frequency by varying the level of hysteresis. The hysteresis has a defined minimum (typ 5%) and a maximum (typ 30%). The frequency may deviate from nominal in some conditions. This depends upon the desired LED current, the coil inductance and the voltages at the input and the load. Loop compensation is achieved by a single external capacitor C2, connected between SHP and SGND.

The control loop sets the duty cycle so that the sense voltage is:

$$V_{\text{SENSE}} = 0.218 \left(\frac{V_{\text{ADJ}}}{V_{\text{REF}}} \right)$$

Therefore,

$$I_{LED} = \left(\frac{0.218}{R_S}\right) \left(\frac{V_{ADJ}}{V_{REF}}\right)$$
(Buck mode) Equation 1

If the ADJ pin connected to the REF pin, this simplifies to:

$$I_{LED} = \left(\frac{0.218}{R_s}\right) \left(\frac{V_{ADJ}}{V_{REF}}\right) (Buck mode)$$



Figure 21 Buck Configuration







or

Application Information (Continued)

b) Boost and Buck-Boost Modes - the most simple boost/buck-boost circuit shown in Figure 23

Control in Boost and Buck-Boost mode is achieved by sensing the coil current in the series resistor R_S , connected between the two inputs of a current monitor within the control loop block. An output from the control loop drives the input of a comparator which drives the gate of the external NMOS switch transistor Q1 via the internal Gate Driver. When the switch is on, the drain voltage of Q1 is near zero. Current flows from V_{IN} , via R_S , coil and switch to ground. This current ramps up until an upper threshold value is reached (see Figure 24). At this point GATE goes low, the switch is turned off and the drain voltage increases to either:

- the load voltage VLEDS plus the forward voltage of D1 in Boost configuration,
- the load voltage VLEDS plus the forward voltage of D1 plus V_{IN} in Buck-Boost configuration.

Current flows via R_S , coil, D1 and LED back to V_{IN} (Buck-boost mode), or GND (Boost mode). When the coil current has ramped down to a lower threshold value, GATE goes high, the switch is turned on again and the cycle of events repeats, resulting in continuous oscillation. The feedback loop adjusts the NMOS switch duty cycle to stabilize the LED current in response to changes in external conditions, including input voltage and load voltage. Loop compensation is achieved by a single external capacitor C2, G connected between SHP and SGND. Note that in reality, a load capacitor C_{OUT} is used, so that the LED current waveform shown is smoothed.

The average current in the sense resistor and coil, I_{RS} , is equal to the average of the maximum and minimum threshold currents and the ripple current (hysteresis) is equal to the difference between the thresholds.

The average current in the LED, I_{LED} , is always less than I_{RS} . The feedback control loop adjusts the switch duty cycle, D, to achieve a set point at the sense resistor. This controls I_{RS} . During the interval t_{OFF} , the coil current flows through D1 and the LED load. During t_{ON} , the coil current flows through Q1, not the LEDs. Therefore the set point is modified by D using a gating function to control I_{LED} indirectly. In order to compensate internally for the effect of the gating function, a control factor, GI_ADJ is used. GI_ADJ is set by a pair of external resistors, R_{GI1} and R_{GI2} (Figure 23). This allows the sense voltage to be adjusted to an optimum level for power efficiency without significant error in the LED controlled current.

$$GI_ADJ = \left(\frac{RGI}{RGII + RGI2}\right)$$

Equation 2 (Boost and Buck-Boost modes)

The control loop sets the duty cycle so that the sense resistor current is:

$$R_{S} = \left(\frac{0.225}{R_{S}}\right) \left(\frac{GI_{ADJ}}{1-D}\right) \left(\frac{V_{ADJ}}{V_{REF}}\right)$$

Equation 3 (Boost and Buck-Boost modes)

 ${\sf I}_{\sf RS}$ equals the coil current. The coil is connected only to the switch and the schottky diode. The schottky diode passes the LED current.









Therefore the average LED current is the coil current multiplied by the schottky diode duty cycle, 1-D.

$$I_{LED} = I_{RS} (1-D) = \left(\frac{0.225}{R_S}\right) GI_ADJ \left(\frac{V_{ADJ}}{V_{REF}}\right)$$

(Boost and Buck-Boost)

Equation 4

This shows that the LED current depends on the ADJ pin voltage, the reference voltage and 3 resistor values (R_S, R_{Gl1} and R_{Gl2}). It is independent of the input and output voltages.

(Boost and Buck-Boost)

If the ADJ pin is connected to the REF pin, this simplifies to:

$$I_{LED} = \left(\frac{0.225}{Rs}\right) GI_ADJ$$

Now ILED is dependent only on the 3 resistor values.

Considering power dissipation and accuracy, it is useful to know how the mean sense voltage varies with input voltage and other parameters.

$V_{RS} = I_{RS} = 0.225 \left(\frac{GI_ADJ}{1-D} \right) \left(\frac{V_{ADJ}}{V_{REF}} \right)$	(Boost and Buck-Boost)	Equation 5
---	------------------------	------------

This shows that the sense voltage varies with duty cycle in Boost and Buck-Boost configurations.

Application Circuit Design

External component selection is driven by the characteristics of the load and the input supply, since this will determine the kind of topology being used for the system. Component selection begins with the current setting procedure, the inductor/frequency setting and the MOSFET selection. Finally after selecting the freewheeling diode and the output capacitor (if needed), the application section will cover the PWM dimming and thermal feedback. The full procedure is greatly accelerated by the web Calculator spreadsheet, which includes fully automated component selection, and is available on the Diodes website. However the full calculation is also given here.

Some components depend upon the switching frequency and the duty cycle. The switching frequency is regulated by the ZXLD1370 to a large extent, depending upon conditions. This is discussed in a later paragraph dealing with coil selection.

Duty Cycle Calculation and Topology Selection

The duty cycle is a function of the input and output voltages. Approximately, the MOSFET switching duty cycle is:



Because D must always be a positive number less than 1, these equations show that:

V _{OUT} < V _{IN}	for Buck (voltage step-down)
$V_{OUT} > V_{IN}$	for Boost (voltage step-up)
V_{OUT} > or = or < V_{IN}	for Buck-Boost (voltage step-down or step-up)

This allows us to select the topology for the required voltage range.



More exact equations are used in the web Calculator. These are:

$$D_{BUCK} = \frac{V_{OUT} + V_F + I_{OUT} (R_S + R_{COIL})}{V_{IN} + V_F - V_{DSON}}$$
 for Buck

$$D_{BOOST} = \frac{V_{OUT} - V_{IN} + I_{IN} (R_S + R_{COIL}) + V_F}{V_{OUT} + V_F - V_{DSON}}$$
 for Boost

$$D_{BB} = \frac{V_{OUT} + V_F + (I_{IN} + I_{OUT}) (R_S + R_{COIL})}{V_{OUT} + V_{IN} + V_F - V_{DSON}}$$
 for Buck-Boost
Where V_F = schottky diode forward voltage, estimated for the expected coil current, I_{COIL}
 V_{DSON} = MOSFET drain source voltage in the ON condition (dependent on R_{DSON} and drain current = I_{COIL})

R_{COIL} = DC winding resistance of L1

The additional terms are relatively small, so the exact equations will only make a significant difference at lower operating voltages at the input and output, i.e. low input voltage or a small number of LEDs connected in series. The estimates of V_F and V_{DSON} depend on the coil current. The mean coil current, I_{COIL} depends upon the topology and upon the mean terminal currents as follows:

		I _{LED}	for Buck	
ICOIL	= -	l I _{IN}	for Boost	Equation 8
			for Buck-Boost	

 I_{LED} is the target LED current and is already known. I_{IN} will be calculated with some accuracy later, but can be estimated now from the electrical power efficiency. If the expected efficiency is roughly 90%, the output power P_{OUT} is 90% of the input power, P_{IN} , and the coil current is estimated as follows.

Where N is the number of LEDs connected in series, and VLED is the forward voltage drop of a single LED at ILED.

So	$I_{\rm IN} \approx \frac{I_{\rm LED} N V_{\rm LED}}{0.9 V_{\rm IN}}$	Equation 9
----	---	------------

Equation 9 can now be used to find I_{COIL} in Equation 8, which can then be used to estimate the small terms in Equation 7. This completes the calculation of Duty Cycle and the selection of Buck, Boost or Buck-Boost topology.

An initial estimate of duty cycle is required before we can choose a coil. In Equation 7, the following approximations are recommended:

VF	= 0.5V
I _{IN} (Rs+R _{COIL})	= 0.5V
I _{OUT} (R _S +R _{COIL})	= 0.5V
V _{DSON}	= 0.1V
$(I_{IN}+I_{OUT})(R_S+R_{COIL})$	= 1.1V

Then Equation 7 becomes:





Application Information (Cont.)

Setting the LED current

The LED current requirement determines the choice of the sense resistor R_S. This also depends on the voltage on the ADJ pin and the voltage on the GI pin, according to the topology required.

The ADJ pin may be connected directly to the internal 1.25V reference (V_{REF}) to define the nominal 100% LED current. The ADJ pin can also be driven with an external DC voltage between 125mV and 2.5V to adjust the LED current proportionally between 10% and 200% of the nominal value.

For a divider ratio GI_ADJ greater than 0.65V, the ZXLD1370 operates in Buck mode when $V_{ADJ} = 1.25V$. If GI_ADJ is less than 0.65V (typical), the device operates in Boost or Buck-Boost mode, according to the load connection. This 0.65V threshold varies in proportion to V_{ADJ} , i.e., the Buck mode threshold voltage is 0.65 V_{ADJ} /1.25V.

ADJ and GI are high impedance inputs within their normal operating voltage ranges. An internal 2.6V clamp protects the device against excessive input voltage and limits the maximum output current to approximately 4% above the maximum current set by V_{REF} if the maximum input voltage is exceeded.

Equation 10

Buck Topology

In Buck mode, GI is connected to ADJ as in Figure 25. The LED current depends only upon R_S, V_{ADJ} and V_{REF} . From **Equation 1** above,

 $R_{SBUCK} = \left(\frac{0.218}{I_{LED}}\right) \left(\frac{V_{ADJ}}{V_{REF}}\right)$

If ADJ is directly connected to VREF, this becomes:

$$R_{SBUCK} = \left(\frac{0.218}{I_{LED}}\right)$$



Figure 25 Setting LED Current in Buck Configuration

Boost and Buck-Boost Topology

For Boost and Buck-boost topologies, the LED current depends upon the resistors, R_{S} , R_{GI1} , and R_{GI2} as in **Equations 4** and **2** above. There is more than one degree of freedom. That is to say, there is not a unique solution. From **Equation 4**,

$$R_{SBOOSTBB} = \left(\frac{0.225}{I_{LED}}\right) GI_{ADJ} \left(\frac{V_{ADJ}}{V_{REF}}\right)$$
 Equation 11

If ADJ is connected to REF, this becomes

$$\mathsf{R}_{\mathsf{SBOOSTBB}} = \left(\frac{0.225}{\mathsf{I}_{\mathsf{LED}}}\right) \mathsf{GI}_{\mathsf{ADJ}}$$

GI_ADJ is given by Equation 2, repeated here for convenience:

$$GI_ADJ = \left(\frac{RGI}{RGI + RGI2}\right)$$

Note that from considerations of ZXLD1370 input bias current, the recommended limits for RGI1 are:

 $22k\Omega < R_{GI1} < 100k\Omega$

Equation 12

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Figure 26 Setting LED Current in Boost and Buck-Boost Configuration



The additional degree of freedom allows us to select GI_ADJ within limits but this may affect overall performance a little. As mentioned above, the working voltage range at the GI pin is restricted. The permitted range of GI_ADJ in Boost or Buck-Boost configuration is:

The mean voltage across the sense resistor is:

 $V_{RS} = I_{COIL} R_{S}$

Note that if GI_ADJ is made larger, these equations show that R_S is increased and V_{RS} is increased. Therefore, for the same coil current, the dissipation in R_S is increased. So, in some cases, it is better to minimize GI_ADJ. However, consider **Equation 5**. If ADJ is connected to REF, this becomes

$$V_{RS} = 0.225 \left(\frac{GI_ADJ}{1-D} \right)$$

This shows that V_{RS} becomes smaller than 225mV if GI_ADJ < 1 - D. If also D is small, V_{RS} can become too small. For example if D = 0.2, and GI_ADJ is the minimum value of 0.2, then V_{RS} becomes $0.225^* 0.2 / 0.8 = 56.25 \text{ mV}$. This will increase the LED current error due to small offsets in the system, such as mV drop in the copper printed wiring circuit, or offset uncertainty in the ZXLD1370. If now, GI_ADJ is increased to 0.4 or 0.5, V_{RS} is increased to a value greater than 100mV. This will give small enough I_{LED} error for most practical purposes. Satisfactory operation will be obtained if V_{RS} is more than about 80mV. This means GI_ADJ should be greater than (1-D_{MIN}) * 80/225 = (1- D_{MIN}) * 0.355.

There is also a maximum limit on V_{RS} which gives a maximum limit for GI_ADJ. If V_{RS} exceeds approximately 300mV, or 133% of 225mV, the STATUS output may indicate an overcurrent condition. This will happen for larger D_{MAX} .

Therefore, together with the requirement of Equation 13, the recommended range for GI_ADJ is:

$$0.355 (1-D_{MIN}) < GI_ADJ < 1.33 (1-D_{MAX})$$

An optimum compromise for GI_ADJ is suggested, i.e.

$$GI_ADJ_{AUTO} = 1 - D_{MAX}$$

This value is used for the "Automatic" setting of the web Calculator. If $1-D_{MAX}$ is less than 0.2, then GI_ADJ is set to 0.2. If $1-D_{MAX}$ is greater than 0.5 then GI_ADJ is set to 0.5.

Once GI_ADJ has been selected, a value of R_{GI1} can be selected from Equation 12. Then R_{GI2} is calculated as follows, rearranging Equation 2:

$$R_{GI2} = R_{GI1} \left(\frac{1 - GI _ ADJ}{GI _ ADJ} \right)$$

For example to drive 12 LEDS at a current of 350mA from a 12V supply requires Boost configuration. Each LED has a forward voltage of 3.2V at 350mA, so $V_{OUT} = 3.2^{*}12 = 38.4V$. From **Equation 6**, the duty cycle is approximately

$$\frac{\left(V_{OUT} - V_{IN}\right)}{V_{OUT}} = \left(\frac{38.4 - 12}{38.4}\right) = 0.6875$$

From **Equation 16**, we set GI_ADJ to 1 - D = 0.3125.

IF $R_{Gl1} = 33k\Omega$, then from **Equation 17**,

$$R_{GI2} = 33x \left(\frac{1 - 0.3125}{0.3125}\right) = 72.6k\Omega$$

Let us choose the preferred value R_{Gl2} = 75k Ω . Now GI_ADJ is adjusted to the new value, using Equation 2.

$$GI_ADJ = \left(\frac{RGI}{RGI1 + RGI2}\right) = \frac{33k}{33k + 75k} = 0.305$$

ZXLD1370

Equation 14



Equation 16

Equation 17

Equation 15



Now we calculate R_S from Equation 11. Assume ADJ is connected to REF.

$$R_{SBOOSTBB} = \left(\frac{0.225}{I_{LED}}\right) x GI_ADJx \left(\frac{V_{ADJ}}{V_{REF}}\right) = \frac{0.225}{0.35} x 0.305 = 0.196\Omega$$

A preferred value of $R_{SBOOSTBB} = 0.2\Omega$ will give the desired LED current with an error of 2% due to the preferred value selection.

Table 1 shows typical resistor values used to determine the GI_ADJ ratio with E24 series resistors.

GI Ratio	R _{GI1}	R _{G2}
0.2	30kΩ	120kΩ
0.25	33kΩ	100kΩ
0.3	39kΩ	91kΩ
0.35	30kΩ	56kΩ
0.4	100kΩ	150kΩ
0.45	51kΩ	62kΩ
0.5	30kΩ	30kΩ

This completes the LED current setting.

Inductor Selection and Frequency Control

The selection of the inductor coil, L1, requires knowledge of the switching frequency and current ripple, and depends on the duty cycle to some extent. In the hysteretic converter, the frequency depends upon the input and output voltages and the switching thresholds of the current monitor. The peak-to-peak coil current is adjusted by the ZXLD1370 to control the frequency to a fixed value. This is done by controlling the switching thresholds within particular limits. This effectively much reduces the overall frequency range for a given input voltage range. Where the input voltage range is not excessive, the frequency is regulated to approximately 330kHz in Buck configuration, and 300kHz in Boost and Buck-Boost configurations. This is helpful in terms of EMC and other system requirements.

For larger input voltage variation, or when the choice of coil inductance is not optimum, the switching frequency may depart from the regulated value, but the regulation of LED current remains successful. If desired, the frequency can to some extent be increased by using a smaller inductor, or decreased using a larger inductor. The web Calculator will evaluate the frequency across the input voltage range and the effect of this upon power efficiency and junction temperatures.

Determination of the input voltage range for which the frequency is regulated may be required. This calculation is very involved, and is not given here. However the performance in this respect can be evaluated within the web Calculator for the chosen inductance.

The inductance is given as follows in terms of peak-to-peak ripple current in the coil, ΔI_L and the MOSFET on time, ton.

$$L1 = -\begin{cases} \{V_{IN} - V_{LED} - I_{OUT} (R_{DSON} + R_{COIL} + R_{S})\} \frac{t_{ON}}{\Delta I_{L}} & \text{for Buck} \\ \{V_{IN} - I_{IN} (R_{DSON} + R_{COIL} + R_{S})\} \frac{t_{ON}}{\Delta I_{L}} & \text{for Boost} & \text{Equation 18} \\ \{V_{IN} - (I_{IN} + I_{OUT}) (R_{DSON} + R_{COIL} + R_{S})\} \frac{t_{ON}}{\Delta I_{L}} & \text{for Buck-Boost} \end{cases}$$

Therefore In order to calculate L1, we need to find I_{IN} , t_{ON} , and ΔI_L . The effects of the resistances are small and will be estimated.

I_{IN} is estimated from **Equation 9**.

ton is related to switching frequency, f, and duty cycle, D, as follows:

 $t_{ON} = \frac{D}{f}$

Equation 19



Application Information (Cont.)

As the regulated frequency is known, and we have already found D from **Equation 7** or the approximation **Equation 7b**, this allows calculation of t_{ON}.

The ZXLD1370 sets the ripple current, ΔI_L is monitored by the ZXLD1370 which sets this to be between nominally 10% and 30% of the mean coil current, I_{COIL} , which is found from **Equation 8**. The device adjusts the ripple current within this range in order to regulate the switching frequency. We therefore need to use a value of 20% of I_{COIL} to find an inductance which is optimized for the input voltage range. The range of ripple current control is also modulated by other circuit parameters as follows.

$$\Delta I_{LMAX} = \left\{ 0.03 + 0.12 \left(\frac{V_{ADJ}}{V_{REF}} \right) \right\} \frac{1 - D}{GI_ADJ} ICOIL$$

$$\Delta I_{LMIN} = \left\{ 0.01 + 0.04 \left(\frac{V_{ADJ}}{V_{REF}} \right) \right\} \frac{1 - D}{GI_ADJ} ICOIL$$

$$\Delta I_{LMID} = \left\{ 0.02 + 0.08 \left(\frac{V_{ADJ}}{V_{REF}} \right) \right\} \frac{1 - D}{GI_ADJ} ICOIL$$
Equation 20

If ADJ is connected to REF, this simplifies to:

$$\Delta I_{LMAX} = 0.15 \frac{1-D}{GI_ADJ}I_{COIL}$$

$$\Delta I_{LMIN} = 0.05 \frac{1-D}{GI_ADJ}I_{COIL}$$
Equation 20a
$$\Delta I_{LMID} = 0.1 \frac{1-D}{GI_ADJ}I_{COIL}$$

Where ΔI_{LMID} is the value we must use in **Equation 18**. We have now established the inductance value.

The chosen coil should have a saturation current higher than the peak sensed current. This saturation current is the DC current for which the inductance has decreased by 10% compared to the low current value.

Assuming $\pm 10\%$ ripple current, we can find this peak current from **Equation 8**, adjusted for ripple current:

	Γ	1.1 I _{LED}	for Buck
I _{COILPEAK} =	1	1.1 I _{INMAX}	for Boost
	L	1.1 I _{INMAX} + I _{I ED}	for Buck-Boost

Equation 21

Where I_{INMAX} is the value of I_{IN} at minimum V_{IN} .

The mean current rating is also a factor, but normally the saturation current is the limiting factor.

The following websites may be useful in finding suitable components:

www.coilcraft.com www.niccomp.com www.wuerth-elektronik.de



MOSFET Selection

The ZXLD1370 requires an external NMOS FET as the main power switch with a voltage rating at least 15% higher than the maximum circuit voltage to ensure safe operation during the overshoot and ringing of the switch node. The current rating is recommended to be at least 10% higher than the average transistor current. The power rating is then verified by calculating the resistive and switching power losses.

 $P = P_{RESISTIVE} + P_{SWITCHING}$

Resistive Power Losses

The resistive power losses are calculated using the RMS transistor current and the MOSFET on-resistance. Calculate the current for the different topologies as follows:

Buck Mode

 $I_{MOSFET-MAX} = D_{MAX} \times I_{LED}$

When operating at low V_{IN} in Buck mode a MOSFET with a suitably low V_T must be chosen to ensure that the MOSFET is properly enhanced. This is of most importance in Buck mode where a Bootstrap cannot be implemented.

Boost and Buck-Boost Mode

$$I_{MOSFET-MAX} = \frac{D_{MAX}}{1 - D_{MAX}} \times i_{LED}$$

When operating at low V_{IN} in Boost or Buck-Boost modes, a Bootstrap circuit (see Figure 37) to V_{AUX} is recommended to fully enhance the external MOSFET. If a Bootstrap circuit is not implemented, then a MOSFET with a suitably low V_T must be chosen to ensure that the MOSFET is properly enhanced.

The approximate RMS current in the MOSFET will be:

Buck Mode

$$I_{MOSFET-RMS} = I_{LED} \sqrt{D}$$

Boost and Buck-Boost Mode

$$I_{\text{MOSFET}-\text{RMS}} = \frac{\sqrt{D}}{1-D} X I_{\text{LED}}$$

The resistive power dissipation of the MOSFET is:

Switching Power Losses

Calculating the switching MOSFET's switching loss depends on many factors that influence both turn-on and turn-off. Using a first order rough approximation, the switching power dissipation of the MOSFET is:

$$P_{SWITCHING} = \frac{C_{RSS} \times V^2_{IN} \times f_{sw} \times I_{LOAD}}{I_{GATF}}$$

Where

C_{RSS} is the MOSFET's reverse-transfer capacitance (a data sheet parameter),

f_{SW} is the switching frequency,

IGATE is the MOSFET gate-driver's sink/source current at the MOSFET's turn-on threshold.



Matching the MOSFET with the controller is primarily based on the rise and fall time of the gate voltage. The best rise/fall time in the application is based on many requirements, such as EMI (conducted and radiated), switching losses, lead/circuit inductance, switching frequency, etc. How fast a MOSFET can be turned on and off is related to how fast the gate capacitance of the MOSFET can be charged and discharged. The relationship between C (and the relative total gate charge Q_G), turn-on/turn-off time and the MOSFET driver current rating can be written as:

$$\begin{split} dt &= \frac{dV \cdot C}{I} = \frac{Qg}{I} \\ \text{where} \\ dt &= \text{turn-on/turn-off time} \\ dV &= \text{gate voltage} \\ C &= \text{gate capacitance} = Q_G/V \\ I &= \text{drive current} - \text{constant current source (for the given voltage value)} \end{split}$$

Here the constant current source "I" usually is approximated with the peak drive current at a given driver input voltage.

(Example 1)

Using the DMN6068 MOSFET ($V_{DS(MAX)} = 60V$, $I_{D(MAX)} = 8.5A$):

 \rightarrow Q_G = 10.3nC at V_{GS} = 10V

ZXLD1370 IPEAK = I GATE = 300mA

$$dt = \frac{Q_g}{I_{PEAK}} = \frac{10.3nC}{300mA} = 35ns$$

Assuming that cumulatively the rise time and fall time can account for a maximum of 10% of the period, the maximum frequency allowed in this condition is:

 $t_{PERIOD} = 20^{*} dt$ \rightarrow $f = 1/t_{PERIOD} = 1.43 MHz$

This frequency is well above the max frequency the device can handle, therefore the DNM6068 can be used with the ZXLD1370 in the whole spectrum of frequencies recommended for the device (from 300kHz to 1MHz).

(Example 2)

Using the ZXMN6A09K ($V_{DS(MAX)} = 60V$, $I_{D(MAX)} = 12.2A$):

$$\rightarrow$$
 Q_G = 29nC at V_{GS} = 10V

ZXLD1370 I_{PEAK} = 300mA

$$dt = \frac{Q_g}{I_{PEAK}} = \frac{29nC}{300mA} = 97ns$$

Assuming that cumulatively the rise time and fall time can account for a maximum of 10% of the period, the maximum frequency allowed in this condition is:

 $t_{PERIOD} = 20^{*}dt$ \rightarrow $f = 1/t_{PERIOD} = 515 kHz$

This frequency is within the recommended frequency range the device can handle, therefore the ZXMN6A09K is recommended to be used with the ZXLD1370 for frequencies from 300kHz to 500kHz.

The recommended total gate charge for the MOSFET used in conjunction with the ZXLD1370 is less than 30nC.



Junction Temperature Estimation

Finally, the ZXLD1370 junction temperature can be estimated using the following equations:

Total supply current of ZXLD1370:

 $I_{QTOT} \approx I_Q + f \cdot Q_G$

Where I_Q = total quiescent current I_{Q-IN} + I_{Q-AUX}

Power consumed by ZXLD1370:

 $\mathsf{P}_{\mathsf{IC}} = \mathsf{V}_{\mathsf{IN}} \bullet (\mathsf{I}_{\mathsf{Q}} + \mathsf{f} \bullet \mathsf{Qg})$

Or in case of separate voltage supply, with $V_{AUX} < 15V$:

 $P_{IC} = V_{IN} \bullet I_{Q-IN} + V_{AUX} \bullet (I_{Q-AUX} + f \bullet Qg)$

 $T_{J} = T_{A} + P_{IC} \cdot \theta_{JA} = T_{A} + P_{IC} \cdot (\theta_{JC} + \theta_{CA})$

Where the total quiescent current I_{QTOT} consists of the static supply current (I_Q) and the current required to charge and discharge the gate of the power MOSFET. Moreover, the part of thermal resistance between case and ambient depends on the PCB characteristics.



Figure 27 Power Derating Curve for ZXLD1370 Mounted on Test Board According to JESD51



Diodes Selection

For maximum efficiency and performance, the rectifier (D1) should be a fast low capacitance Schottky diode* with low reverse leakage at the maximum operating voltage and temperature. The Schottky diode also provides better efficiency than silicon PN diodes, due to a combination of lower forward voltage and reduced recovery time.

It is important to select parts with a peak current rating above the peak coil current and a continuous current rating higher than the maximum output load current. In particular, it is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode.

The higher forward voltage and overshoot due to reverse recovery time in silicon diodes will increase the peak voltage on the Drain of the external MOSFET. If a silicon diode is used, care should be taken to ensure that the total voltage appearing on the Drain of the external MOSFET, including supply ripple, does not exceed the specified maximum value.

*A suitable Schottky diode would be PDS3100 (Diodes Incorporated).

Output Capacitor

An output capacitor may be required to limit interference or for specific EMC purposes. For boost and buck-boost regulators, the output capacitor provides energy to the load when the freewheeling diode is reverse biased during the first switching subinterval. An output capacitor in a buck topology will simply reduce the LED current ripple below the inductor current ripple. In other words, this capacitor changes the current waveform through the LED(s) from a triangular ramp to a more sinusoidal version without altering the mean current value.

In all cases, the output capacitor is chosen to provide a desired current ripple of the LED current (usually recommended to be less than 40% of the average LED current).

Buck

$$C_{OUTPUT} = \frac{\Delta I_{L-PP}}{8x f_{SW} x r_{LED} x \Delta I_{LED-PP}}$$

Boost and Buck-Boost

$$C_{OUTPUT} = \frac{DxI_{LED-PP}}{f_{SW} xr_{LED} x\Delta I_{LED-PP}}$$

Where:

- ΔI_{L-PP} is the ripple of the inductor current, usually ±20% of the average sensed current
- ΔI_{LED-PP} is the ripple of the LED current, it should be <40% of the LEDs average current
- f_{SW} is the switching frequency (From graphs and calculator)
- r_{LED} is the dynamic resistance of the LEDs string (n times the dynamic resistance of the single LED from the datasheet of the LED manufacturer).

The output capacitor should be chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. The minimum RMS current for the output capacitor is calculated as follows:

Buck

$$I_{COUTPUT-RMS} = \frac{I_{LED-PP}}{\sqrt{12}}$$

Boost and Buck-Boost

$$I_{COUTPUT-RMS} = I_{LED} \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

Ceramic capacitors with X7R dielectric are the best choice due to their high ripple current rating, long lifetime, and performance over the voltage and temperature ranges.



Input Capacitor

The input capacitor can be calculated knowing the input voltage ripple $\Delta V_{\text{IN-PP}}$ as follows:

Buck

$$C_{IN} = \frac{D x (1 - D) x I_{LED}}{f_{SW} x \Delta V_{IN-PP}}$$
 Use D = 0.5 as worst case

Boost

$$C_{IN} = \frac{\Delta I_{L-PP}}{8 x f_{SW} x \Delta V_{IN-PP}}$$

Buck-Boost

$$C_{IN} = \frac{D \times I_{LED}}{f_{SW} \times \Delta V_{IN-PP}}$$
 Use D = D_{MAX} as worst case

The minimum RMS current for the output capacitor is calculated as follows:

Buck

$I_{CIN-RMS} = I_{LED} x \sqrt{Dx(1-D)}$	Use D = 0.5 as worst case
--	---------------------------

Boost

$$I_{\text{CIN-RMS}} = \frac{I_{\text{L-PP}}}{\sqrt{12}}$$

Buck-Boost

$$I_{CIN-RMS} = I_{LED} x \sqrt{\frac{D}{(1-D)}}$$

Use D = D_{MAX} as worst case



PWM Output Current Control & Dimming

The ZXLD1370 has a dedicated PWM dimming input that allows a wide dimming frequency range from 100Hz to 1kHz with up to 1000:1 resolution; however higher dimming frequencies can be used – at the expense of dimming dynamic range and accuracy.

Typically, for a PWM frequency of 1kHz, the error on the current linearity is lower than 5%; in particular the accuracy is better than 1% for PWM from 5% to 100%. This is shown in the graph below:



Figure 28 LED Current Linearity and Accuracy with PWM Dimming at 1kHz

For a PWM frequency of 100Hz, the error on the current linearity is lower than 2.5%; it becomes negligible for PWM greater than 5%. This is shown in the graph below:



Figure 29 LED Current Linearity and Accuracy with PWM Dimming at 100Hz

The PWM pin is designed to be driven by both 3.3V and 5V logic levels. It can be driven also by an open drain/collector transistor. In this case, the designer can either use the internal pull-up network or an external pull-up network in order to speed-up PWM transitions, as shown in the Boost and Buck-Boost section.



Application Information (Cont.)



Figure 31 PWM Dimming from MCU



LED current can be adjusted digitally, by applying a low frequency PWM logic signal to the PWM pin to turn the controller on and off. This will produce an average output current proportional to the duty cycle of the control signal. During PWM operation, the device remains powered up and only the output switch is gated by the control signal.

The PWM signal can achieve very high LED current resolution. In fact, dimming down from 100% to 0.1% at 500Hz, a minimum pulse width of 2µs can be achieved resulting in very high resolution and accuracy. While the maximum recommended pulse is for the PWM signal is 10ms (equivalent to 100Hz) (see Figure 32).

The ultimate PWM dimming ratio will be determined by the switching frequency as the minimum PWM pulse width is determined by resolving at least 1 switching cycle. The figure to the right the switching waveforms for a low duty cycle PWM dimming.

As can be seen, when the LED current restarts (blue waveform) it has to start all the way from zero to the peak level set by $V_{SENSE}/R_{S^*}1.15$. Therefore, the first pulse is always longer than the nominal switching frequency would imply.





The PWM pin can be used to put the device into standby. Taking the PWM pin low (<0.4V) for more than 25ms (typically 15ms) the device will enter its standby state and most of the internal circuitry is switched off and residual quiescent current will be typically 90 μ A. In particular, the STATUS pin will go down to GND while the FLAG and REF pins will stay at their nominal values.

When the device restarts from standby mode, a "start-up" time must be allowed for before the device resume full LED current regulation.



Application Information (Cont.)

Thermal Control of LED Current

For thermal control of the LEDs, the ZXLD1370 monitors the voltage on the TADJ pin and reduces output current if the voltage on this pin falls below 625mV. An external NTC thermistor and resistor can therefore be connected as shown below to set the voltage on the TADJ pin to 625mV at the required temperature threshold. This will give 100% LED current below the threshold temperature and a falling current above it as shown in the graph. The temperature threshold can be altered by adjusting the value of R_{TH} and/or the thermistor to suit the requirements of the chosen LED.

The Thermal Control feature can be disabled by connecting TADJ directly to REF.

Here is a simple procedure to design the thermal feedback circuit:

- 1) Select the temperature threshold T_{THRESHOLD} at which the current must start to decrease
- 2) Select the Thermistor TH1 (both resistive value at +25°C and beta)
- 3) Select the value of the resistor R_{TH} as $R_{TH} = TH$ at $T_{THRESHOLD}$



Thermal network response in Buck configuration with: Rth = 1.8k\Omega and TH1=10k\Omega (beta =3900)

Figure 34 Thermal Feedback Network

The thermistor resistance, R_T, at a temperature of T degrees Kelvin is given by:

$$R_{T} = R_{R} e^{B\left(\frac{1}{T} - \frac{1}{T_{R}}\right)}$$

Where:

 R_{R} is the thermistor resistance at the reference temperature, T_{R}

 T_R is the reference temperature, in Kelvin, normally 273 + 25 = 298K (+25°C) B is the "beta" value of the thermistor.

For example,

1) Temperature threshold $T_{THRESHOLD} = 273 + 70 = 343K (+70°C)$

- 2) TH1 = 10kΩ at +25°C and B = 3900 \rightarrow R_T = 1.8kΩ @ +70°C
- 3) $R_{TH} = R_T \text{ at } T_{THRESHOLD} = 1.8 k\Omega$

Overtemperature Shutdown

The ZXLD1370 incorporates an overtemperature shutdown circuit to protect against damage caused by excessive die temperature. A warning signal is generated on the STATUS output when die temperature exceeds +125°C nominal and the output is disabled when die temperature exceeds +150°C nominal. Normal operation resumes when the device cools back down to +125°C.



FLAG/STATUS Outputs

The FLAG/STATUS outputs provide a warning of extreme operating or fault conditions. FLAG is an open-drain logic output, which is normally off, but switches low to indicate that a warning, or fault condition exists. STATUS is a DAC output, which is normally high (4.5V), but switches to a lower voltage to indicate the nature of the warning/fault.

Conditions monitored, the method of detection and the nominal STATUS output voltage are given in the following table:

Та	hl	е	2
ıa	D	C.	~

Warning/Fault Condition	Severity (Note 17)	Monitored Parameters	FLAG	Nominal STATUS Voltage
Normal Operation	_	—	Н	4.5
	1	V _{AUX} <5.6V	L	4.5
Supply Undervoltage	2	V _{IN} <5.6V	L	3.6
Output Current Out of Regulation (Note 18)	2	V _{SHP} outside normal voltage range	L	3.6
Driver Stalled with Switch 'On', or 'Off' (Note 19)	2	t _{ON} , or t _{OFF} >100µs	L	3.6
Device Temperature Above Maximum Recommended Operating Value	3	T _J >+125°C	L	1.8
Sense Resistor Current I _{RS} Above Specified Maximum	4	V _{SENSE} >0.32V	L	0.9

Notes: 17. Severity 1 denotes lowest severity.

18. This warning will be indicated if the output power demand is higher than the available input power; the loop may not be able to maintain regulation.

19. This warning will be indicated if the gate pin stays at the same level for greater than 100µs (e.g., the output transistor cannot pass enough current to reach the upper switching threshold).



Figure 35 Status Levels

In the event of more than one fault/warning condition occurring, the higher severity condition will take precedence. E.g., 'Excessive Coil Current' and 'Out of Regulation' occurring together will produce an output of 0.9V on the STATUS pin.

If V_{ADJ}>1.7V, V_{SENSE} may be greater than the excess coil current threshold in normal operation and an error will be reported. Hence, STATUS and FLAG are only guaranteed for V_{ADJ}<=V_{REF}.



Application Information (Cont.)

Diagnostic signals should be ignored during the device startup for 100μ s. The device start up sequence will be initiated both during the first power on of the device or after the PWM signal is kept low for more than 15ms, initiating the standby state of the device.

In particular, during the first 100μ s the diagnostic is signaling an overcurrent then an out-of-regulation status. These two events are due to the charging of the inductor and are not true fault conditions.



Figure 36 Diagnostic During Start-Up

Boosting V_{AUX} Supply Voltage in Boost and Buck-Boost Mode

When the input voltage is lower than 8V, the gate voltage will also be lower 8V. This means that depending on the characteristics of the external MOSFET, the gate voltage may not be enough to fully enhance the power MOSFET. This boosting technique is particularly important when the output MOSFET is operating at full current, since the boost circuit allows the gate voltage to be higher than 12V. This guarantees that the MOSFET is fully enhanced reducing both the power dissipation and the risk of thermal runaway of the MOSFET itself. An extra diode D2 and decoupling capacitor C3 can be used, as shown below in Figure 37, to generate a boosted voltage at V_{AUX} when the input supply voltage at V_{IN} is below 8V. This enables the device to operate with full output current when V_{IN} is at the minimum value of 6V. In the case of a low voltage threshold MOSFET, the bootstrap circuit is generally not required.



Figure 37 Bootstrap Circuit for Boost and Buck-Boost Low Voltage Operations

The resistor R2 can be used to limit the current in the bootstrap circuit in order to reduce the impact of the circuit itself on the LED accuracy. The impact on the LED current is usually a decrease of maximum 5% compared to the nominal current value set by the sense resistor.

The Zener diode D3 is used to limit the voltage on the V_{AUX} pin to less than 60V.

Due to the increased number of components and the loss of current accuracy, the bootstrap circuit is recommended only when the system has to operate continuously in conditions of low input voltage (between 6 and 8V) and high load current. Other circumstances such as low input voltage at low load current, or transient low input voltage at high current should be evaluated keeping account of the external MOSFET power dissipation.



Overvoltage Protection

The ZXLD1370 is inherently protected against open-circuit load when used in Buck configuration. However, care has to be taken with opencircuit load conditions in Buck-Boost or Boost configurations. This is because in these configurations there is no internal open-circuit protection mechanism for the external MOSFET. In this case an Overvoltage Protection (OVP) network should be provided externally to the MOSFET to avoid damage due to open circuit conditions. This is shown in Figure 38 below, highlighted in the dotted blue box.



The zener voltage is determined according to: $V_Z = V_{LEDMAX} + 10\%$ where V_{LEDMAX} is maximum LED chain voltage.

If the LEDA voltage exceeds V_Z the gate of MOSFET Q2 will rise turning Q2 on. This will pull the PWM pin low and switch off Q1 until the voltage on the drain of Q1 falls below V_Z . If the voltage at LEDA remains above V_Z for longer than 20ms then the ZXLD1370 will enter into a shutdown state.

Care should be taken such that the maximum gate voltage of the Q2 MOSFET is not exceeded.

Take care of the max voltage drop on the Q2 MOSFET gate.



PCB Layout Considerations

PCB layout is a fundamental activity to get the most of the device in all configurations. In the following section it is possible to find some important insight to design with the ZXLD1370 both in Buck and Buck-Boost configurations.



Figure 39 Circuit Layout

Here are some considerations useful for the PCB layout:

- In order to avoid ringing due to stray inductances, the inductor L1, the anode of D1 and the drain of Q1 should be placed as close together as possible.
- The shaping capacitor C1 is fundamental for the stability of the control loop. To this end, it should be placed no more than 5mm from the SHP pin.
- Input voltage pins, V_{IN} and V_{AUX}, need to be decoupled. It is recommended to use two ceramic capacitors of 2.2uF, X7R, 100V (C3 and C4). In addition to these capacitors, it is suggested to add two ceramic capacitors of 1uF, X7R, 100V each (C2, C8), as well as a further decoupling capacitor of 100nF close to the V_{IN}/V_{AUX} pins (C9). V_{IN} and V_{AUX} pins can be short-circuited when the device is used in buck mode, or can be driven from a separate supply.



Application Examples

Example 1: 2.8A Buck LED Driver

In this application example, the ZXLD1370 is connected as a buck LED driver. The schematic and parts list are shown below. The LED driver is able to deliver 2.8A of LED current with an input voltage range of 8V to 24V. In order to achieve high efficiency at high LED current, a Super Barrier Rectifier (SBR[®]) with a low forward voltage is used as the freewheeling rectifier.

This LED driver is suitable for applications which require high LED current such as LED projector, automatic LED lighting, etc.



Figure 40 Application Circuit: 2.8A Buck LED Driver

Ref No.	Value	Part No.	Manufacturer	
U1	60V LED Driver	ZXLD1370	Diodes Incorporated	
Q1	60V MOSFET	ZXMN6A09K	Diodes Incorporated	
D1	45V 10A SBR	SBR10U45SP5	Diodes Incorporated	
L1	33µH 4.2A	744770933	Wurth Electronik	
C1	100pF 50V	SMD 0805/0603	Generic	
C2	1uF 50V X7R	SMD1206	Generic	
C3 C4 C5	4.7µF 50V X7R	SMD1210	Generic	
R1 R2 R3	300mΩ 1%	SMD1206	Generic	
R4	400mΩ 1%	SMD1206	Generic	
R5	Ω0	SMD 0805/0603	Generic	



Application Information (Cont.)





Example 2: 400mA Boost LED Driver

In this application example, the ZXLD1370 is connected as a boost LED driver. The schematic and parts list are shown below. The LED driver is able to deliver 400mA of LED current into 12 high-brightness LEDs with an input voltage range of 16V to 32V.

The overall high efficiency of 92%+ makes it ideal for applications such as solar LED street lighting and general LED illuminations.



Figure 43 Application Circuit: 400mA Boost LED Driver

Ref No.	Value	Part No.	Manufacturer
U1	60V LED Driver	ZXLD1370	Diodes Incorporated
Q1	60V MOSFET	ZXMN6A25G	Diodes Incorporated
Q2	60V MOSFET	2N7002A	Diodes Incorporated
D1	100V 3A Schottky	PDS3100-13	Diodes Incorporated
Z1	47V 410mW Zener	BZT52C47	Diodes Incorporated
L1	68µH 2.1A	744771168	Wurth Electronik
C1	100pF 50V	SMD 0805/0603	Generic
C3 C9	4.7µF 50V X7R	SMD1210	Generic
C2	1µF 50V X7R	SMD1206	Generic
R1 R2	560mΩ 1%	SMD1206	Generic
R9 R10	33kΩ 1%	SMD 0805/0603	Generic
R12	Ω0	SMD 0805/0603	Generic
R15	2.7kΩ	SMD 0805/0603	Generic



Application Information (Cont.)



400mA Boost LED Driver Typical Performance

Example 3: 700mA Buck-Boost LED Driver

In this application example, the ZXLD1370 is connected as a Buck-Boost LED driver. The schematic and parts list are shown below. The LED driver is able to deliver 700mA of LED current into 4 high-brightness LEDs with an input voltage range of 7V to 20V.

Since the Buck-Boost LED driver handles an input voltage range from below and above the total LED voltage, the versatile input voltage range makes it ideal for automotive lighting applications.



Figure 46 Application Circuit: 700mA Buck-Boost LED Driver



Ref No.	Value	Part No.	Manufacturer
U1	60V LED Driver	ZXLD1370Q	Diodes Incorporated
Q1	60V MOSFET	ZXMN6A25G	Diodes Incorporated
Q2	60V MOSFET	2N7002A	Diodes Incorporated
D1	100V 5A Schottky	PDS5100-13	Diodes Incorporated
Z1	47V 410mW Zener	BZT52C47	Diodes Incorporated
L1	22µH 2.1A	744771122	Wurth Electronik
C1	100pF 50V	SMD 0805/0603	Generic
C3 C9	4.7µF 50V X7R	SMD1210	Generic
C2	1µF 50V X7R	SMD1206	Generic
R1 R2 R3	300mΩ 1%	SMD1206	Generic
R9	33kΩ 1%	SMD 0805/0603	Generic
R10	15kΩ 1%	SMD 0805/0603	Generic
R12	00	SMD 0805/0603	Generic
R15	2.7kΩ	SMD 0805/0603	Generic

700mA Buck-Boost LED Driver Typical Performance



Figure 47 Efficiency



Figure 48 Line Regulation



Ordering Information (Note 20)



Γ	Part Number	Packaging	Status	Part Marking	Reel Quantity	Tape Width	Reel Size
	ZXLD1370EST16TC	TSSOP-16EP	Active	ZXLD 1370 YYWW (Note 21)	2,500	16mm	13"

20. For packaging details, go to our website at http://www.diodes.com/products/packages.html. 21. YY is last two digits of year and WW is two-digit week number Notes:

Marking Information





Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.



	TSSOP-16EP					
Dim	Min	Max	Тур			
Α	-	1.20	-			
A1	0.025	0.100	-			
A2	0.80	1.05	0.90			
b	0.19	0.30	-			
С	0.09	0.20	-			
D	4.90	5.10	5.00			
E	6.20	6.60	6.40			
E1	4.30	4.50	4.40			
е	C	.65 BS(0			
L	0.45	0.75	0.60			
L1	,	1.0 REF	-			
L2	0	.65 BS(С С			
Х	-	-	2.997			
Y	-	-	2.997			
θ1	0°	8°	-			
AI	All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



TSSOP-16EP

Dimensions	Value (in mm)
С	0.650
Х	0.450
X1	3.290
X2	5.000
Y	1.450
Y1	3.290
Y2	4.450
Y3	7.350



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