

7A, 600V N-CHANNEL MOSFET

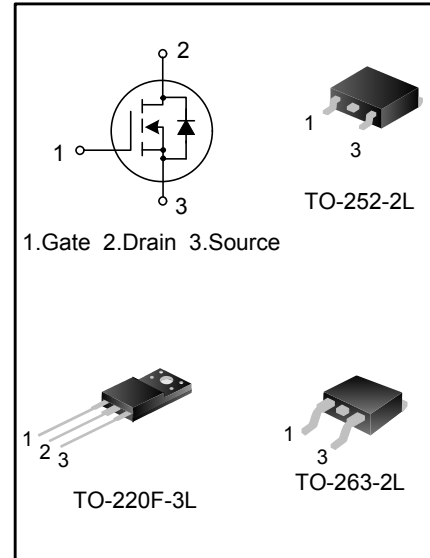
GENERAL DESCRIPTION

SVF7N60F/S/D is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ♦ 7A, 600V, $R_{DS(on)} (typ) = 0.96\Omega @ V_{GS}=10V$
- ♦ Low gate charge
- ♦ Low C_{rss}
- ♦ Fast switching
- ♦ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF7N60F	TO-220F-3L	SVF7N60F	Pb free	Tube
SVF7N60S	TO-263-2L	SVF7N60S	Halogen free	Tube
SVF7N60STR	TO-263-2L	SVF7N60S	Halogen free	Tape & Reel
SVF7N60DTR	TO-252-2L	SVF7N60D	Halogen free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Ratings			Unit
			SVF7N60F	SVF7N60S	SVF7N60D	
Drain-Source Voltage		V _{DS}	600			V
Gate-Source Voltage		V _{GS}	±30			V
Drain Current	T _C =25°C	I _D	7.0			A
	T _C =100°C		4.0			
Drain Current Pulsed		I _{DM}	28			A
Power Dissipation(T _C =25°C) -Derate above 25°C		P _D	45	122	90	W
			0.36	0.98	0.72	W/°C
Single Pulsed Avalanche Energy(Note 1)		E _{AS}	490			mJ
Operation Junction Temperature Range		T _J	-55~+150			°C
Storage Temperature Range		T _{stg}	-55~+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVF7N60F	SVF7N60S	SVF7N60D	
Thermal Resistance, Junction-to-Case	R _{θJC}	2.78	1.02	1.39	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	62.5	62.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	600	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =3.5A	--	0.96	1.2	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	592	770	1001	pF
Output Capacitance	C _{oss}		--	96	--	
Reverse Transfer Capacitance	C _{rss}		--	8.7	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =300V, I _D =7.0A, R _G =25Ω (Note 2,3)	--	15.5	--	ns
Turn-on Rise Time	t _r		--	32.7	--	
Turn-off Delay Time	t _{d(off)}		--	52.2	--	
Turn-off Fall Time	t _f		--	31.5	--	
Total Gate Charge	Q _g	V _{DS} =480V, I _D =7.0A, V _{GS} =10V (Note 2,3)	--	21.1	--	nC
Gate-Source Charge	Q _{gs}		--	4.53	--	
Gate-Drain Charge	Q _{gd}		--	10.0	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	I_{SM}		--	--	28	
Diode Forward Voltage	V_{SD}	$I_S=7.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=7.0A, V_{GS}=0V,$ $di_F/dt=100A/\mu S$	--	482	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.9	--	μC

Notes:

1. $L=30mH, I_{AS}=5.16A, V_{DD}=100V, R_G=25\Omega$, starting $T_{JB}=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycles $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

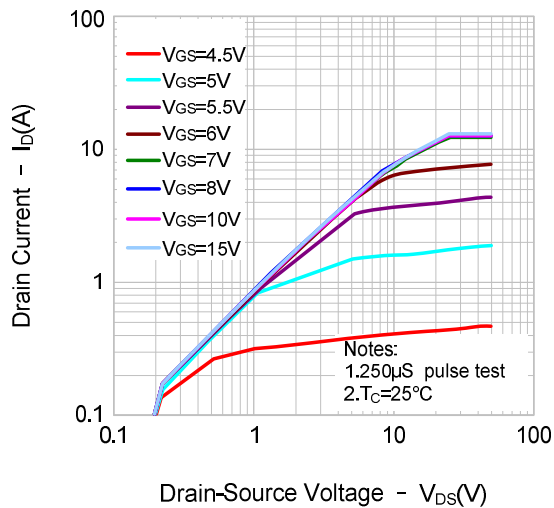


Figure 2. Transfer Characteristics

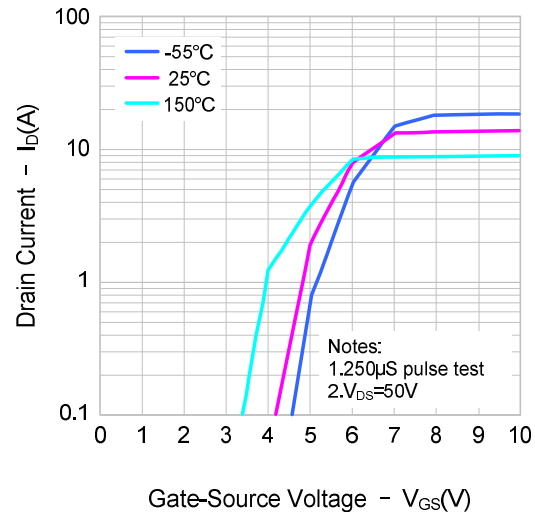


Figure 3. On-Resistance Variation vs. Drain Current

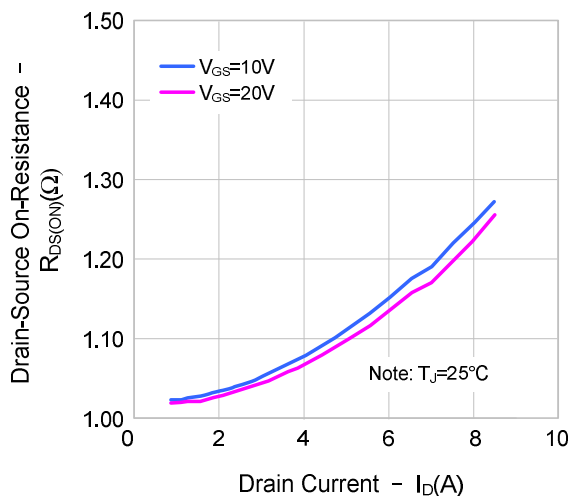
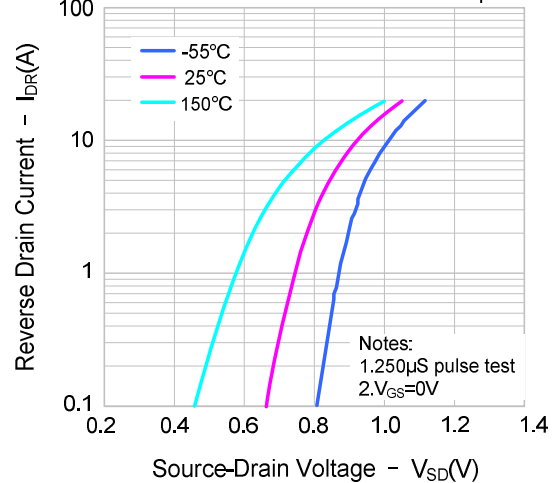


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS(continued)

Figure 5. Capacitance Characteristics

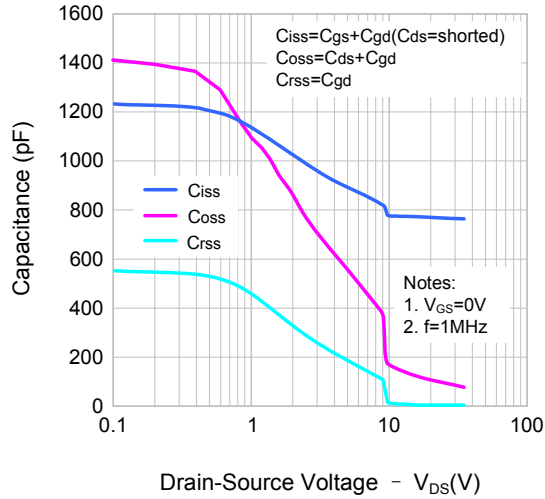


Figure 6. Gate Charge Characteristics

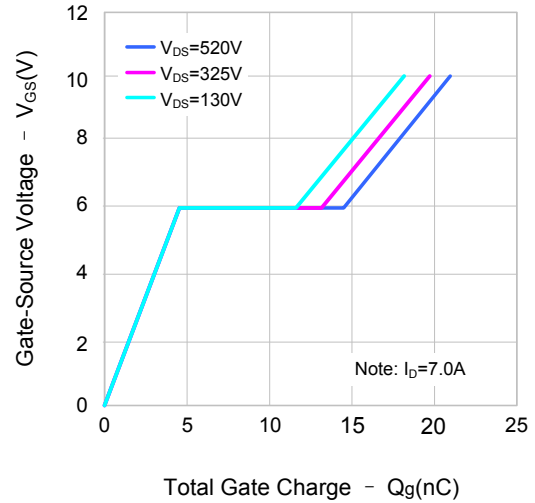


Figure 7. Breakdown Voltage Variation vs. Temperature

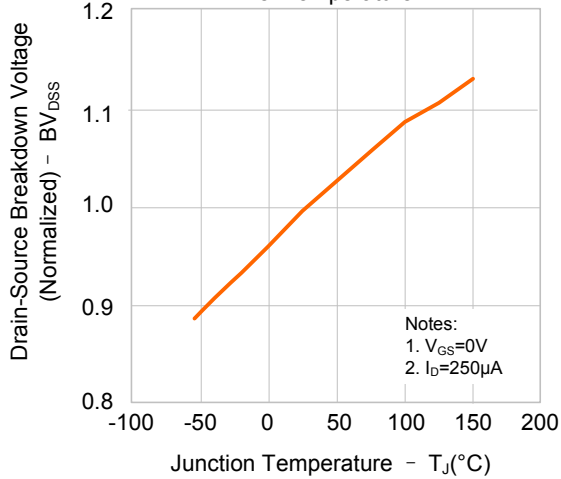


Figure 8. On-resistance vs. Temperature

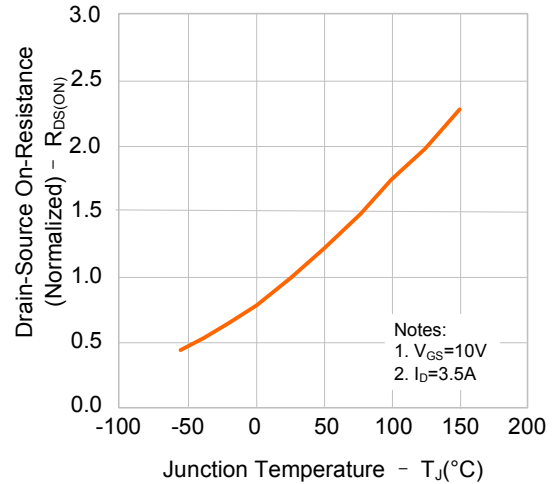


Figure 9-1. Max. Safe Operating Area(SVF7N60F)

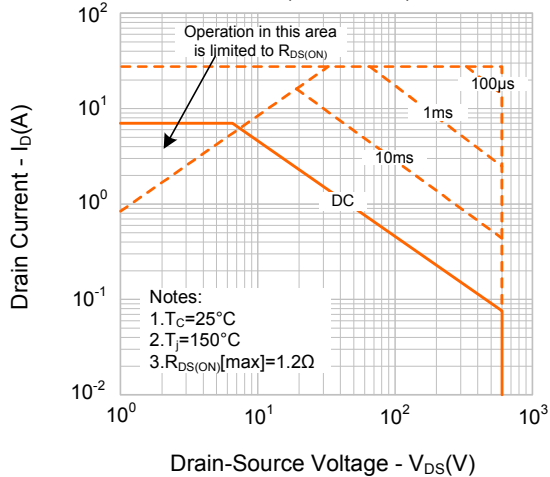
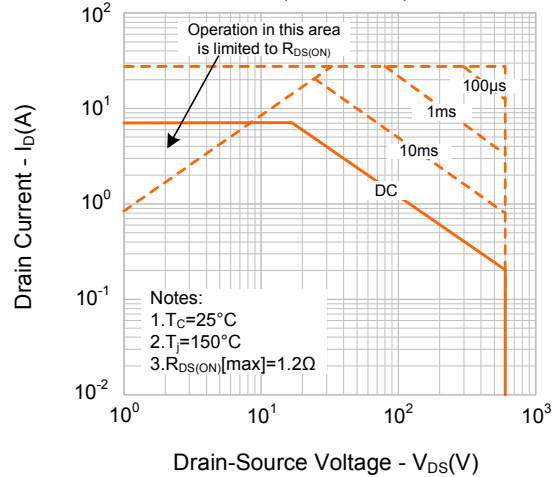
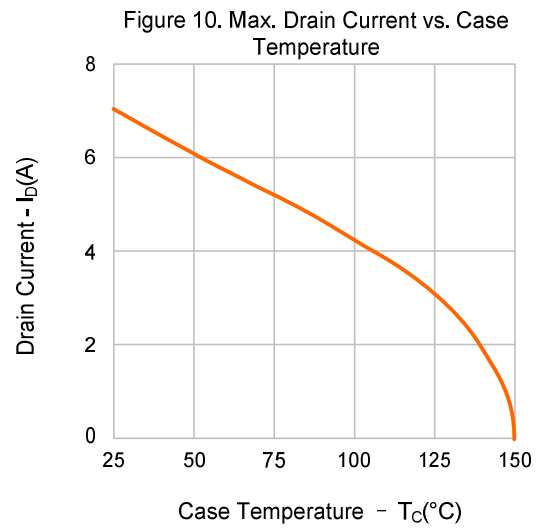
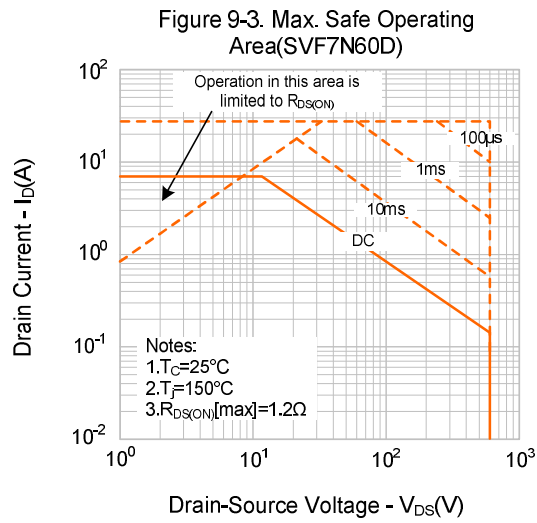


Figure 9-2. Max. Safe Operating Area(SVF7N60S)

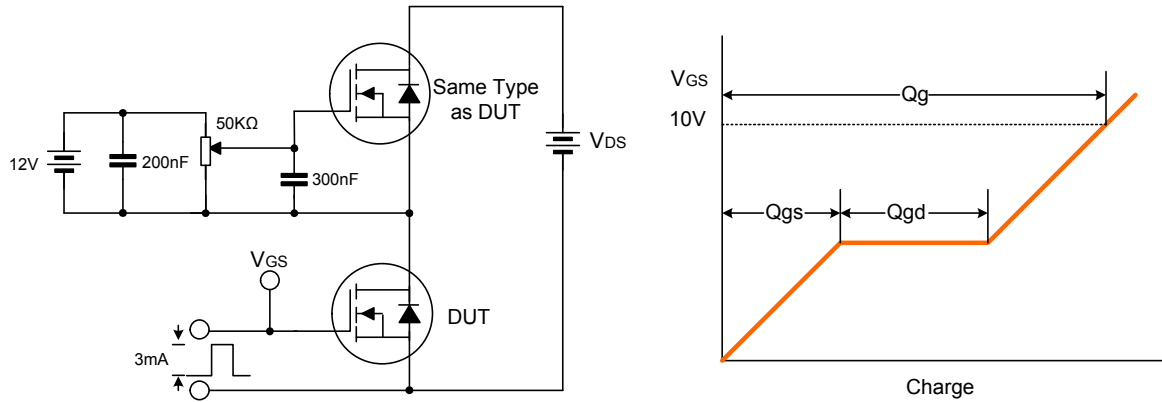


TYPICAL CHARACTERISTICS(continued)

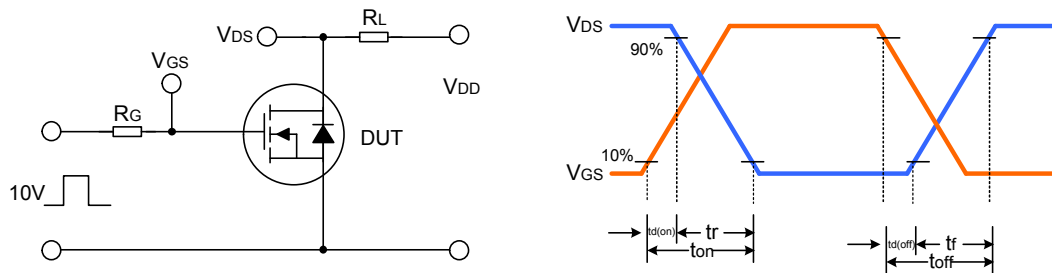


TYPICAL TEST CIRCUIT

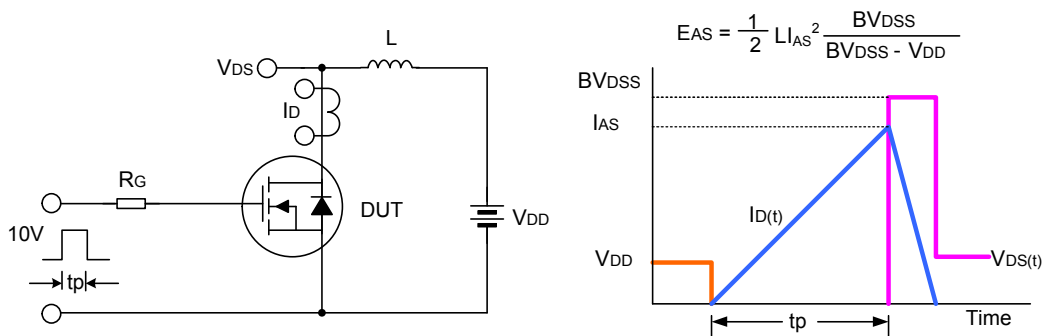
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



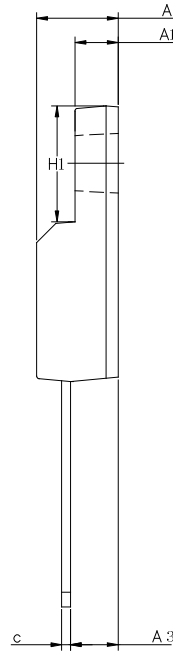
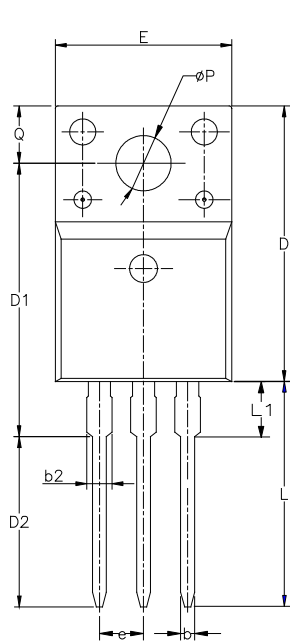
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220F-3L

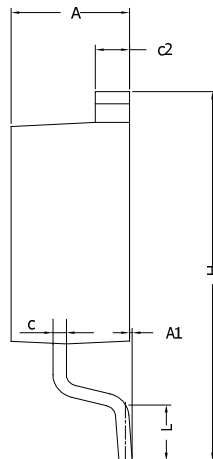
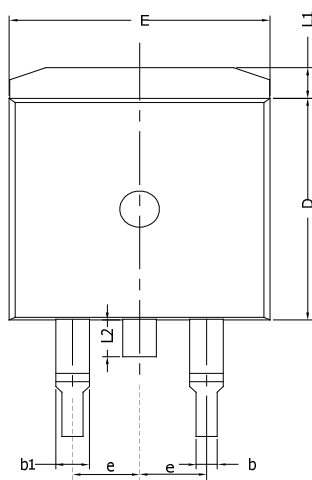
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-263-2L

UNIT: mm

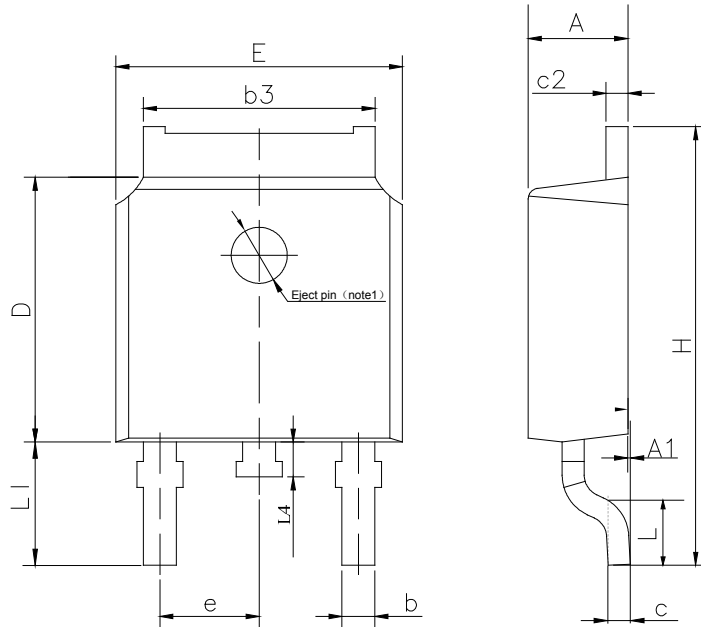


SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e	2.54BSC		
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

PACKAGE OUTLINE(continued)

TO-252-2L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

Disclaimer :

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without prior notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
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Part No.:	SVF7N60F/S/D	Document Type:	Datasheet
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Rev.: 3.2

Revision History:

1. Delete the package outline of TO-262-3L、TO-251J-3L and TO-220-3L
-

Rev.: 3.1

Revision History:

1. Update the package outline of TO-262-3L(1.1version)
 2. Add another solid figure of TO-220-3L
-

Rev.: 3.0

Revision History:

1. Update the package outline of TO-262-3L
-

Rev.: 2.9

Revision History:

1. Modify the package outline of TO-251J-3L
-

Rev.: 2.8

Revision History:

1. Modify the Electrical characteristics
-

Rev.: 2.7

Revision History:

1. Modify the General Description
-

Rev.: 2.6

Revision History:

1. Modify the Ordering information
-

Rev.: 2.5

Revision History:

1. Modify the Ordering information
 2. Modify the package outline of TO-263-2L and TO-262-3L
-

Rev.: 2.4

Revision History:

1. Modify the package information of TO-220-3L
 2. Modify the ordering information
-

Rev.: 2.3

Revision History:

1. Modify the package information of TO-220F-3L
 2. Modify the package information of TO-252-2L
-

Rev.: 2.2

Revision History:

1. Modify the thermal characteristics
-

Rev.: 2.1

Revision History:

1. Modify the package outline of TO-251J-3L

Rev.: 2.0

Revision History:

1. Modify the ordering information

Rev.: 1.9

Revision History:

1. Change the schematic diagram of MOS

Rev.: 1.8

Revision History:

1. Add the package of TO-252-2L

Rev.: 1.7

Revision History:

1. Modify "PACKAGE OUTLINE"

Rev.: 1.6

Revision History:

1. Modify "SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS"

Rev.: 1.5

Revision History:

1. Modify the typ. Value of $R_{DS(on)}$

Rev.: 1.4

Revision History:

1. Add the package of TO-262-3L

Rev.: 1.3

Revision History:

1. Update the package of TO-220-3L

Rev.: 1.2

Revision History:

1. Update the package of TO-220F-3L
2. Add the package of TO-251J-3L

Rev.: 1.1

Revision History:

1. Add the package of TO-263-2L

Rev.: 1.0

Revision History:

1. Original